

CBTL02042A; CBTL02042B

3.3 V, 2 differential channel, 2 : 1 multiplexer/demultiplexer switch for PCI Express Gen2

Rev. 1 — 10 March 2011

Product data sheet

1. General description

CBTL02042A/B is a 2 differential channel, 2-to-1 multiplexer/demultiplexer switch for PCI Express Generation 2 (Gen2), and other high-speed serial interface applications. The CBTL02042A/B can switch two differential signals to one of two locations. Using a unique design technique, NXP has minimized the impedance of the switch such that the attenuation observed through the switch is negligible, and also minimized the channel-to-channel skew as well as channel-to-channel crosstalk, as required by the high-speed serial interface. CBTL02042A/B allows expansion of existing high speed ports for extremely low power.

The device's pinouts are optimized to match different application layouts. CBTL02042A has input and output pins on the opposite of the package, and is suitable for edge connector(s) with different signal sources on the motherboard. CBTL02042B has outputs on both sides of the package, and the device can be placed between two connectors to multiplex differential signals from a controller. Please refer to [Section 8](#) for layout examples.

2. Features and benefits

- 2 bidirectional differential channel, 2 : 1 multiplexer/demultiplexer
- High-speed signal switching for PCIe Gen2 5 Gbit/s
- High bandwidth: 7 GHz at -3 dB
- Low insertion loss:
 - ◆ -0.5 dB at 100 MHz
 - ◆ -1.2 dB at 2.5 GHz
- Low intra-pair skew: 5 ps typical
- Low inter-pair skew: 35 ps maximum
- Low crosstalk: -30 dB at 2.5 GHz
- Low off-state isolation: -25 dB at 2.5 GHz
- Low return loss: -20 dB at 2.5 GHz
- V_{DD} operating range: 3.3 V \pm 10 %
- Shutdown pin (XSD) for power-saving mode
 - ◆ Standby current less than 1 μ A
- ESD tolerance:
 - ◆ 8 kV HBM
 - ◆ 1 kV CDM
- DHVQFN20 package



3. Applications

- Routing of high-speed differential signals with low signal attenuation
 - ◆ PCIe Gen2
 - ◆ DisplayPort 1.2
 - ◆ USB 3.0
 - ◆ SATA 6 Gbit/s

4. Ordering information

Table 1. Ordering information

| Type number | Package | | Version |
|--------------|----------|---|----------|
| | Name | Description | |
| CBTL02042ABQ | DHVQFN20 | plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body 2.5 × 4.5 × 0.85 mm ^[1] | SOT764-1 |
| CBTL02042BBQ | DHVQFN20 | plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body 2.5 × 4.5 × 0.85 mm ^[1] | SOT764-1 |

[1] Total height after printed-circuit board mounting = 1.0 mm maximum.

5. Functional diagram

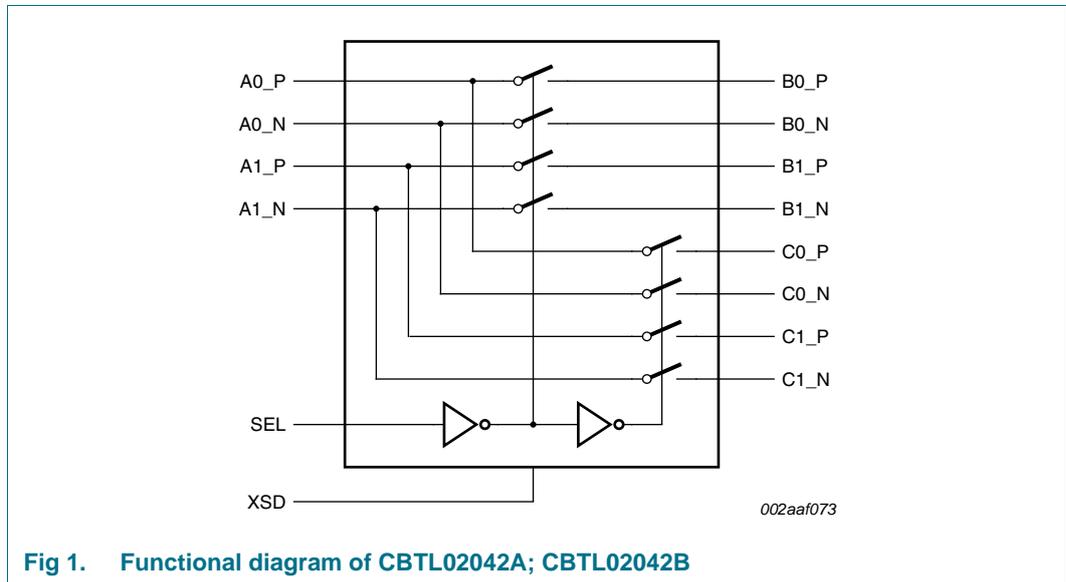
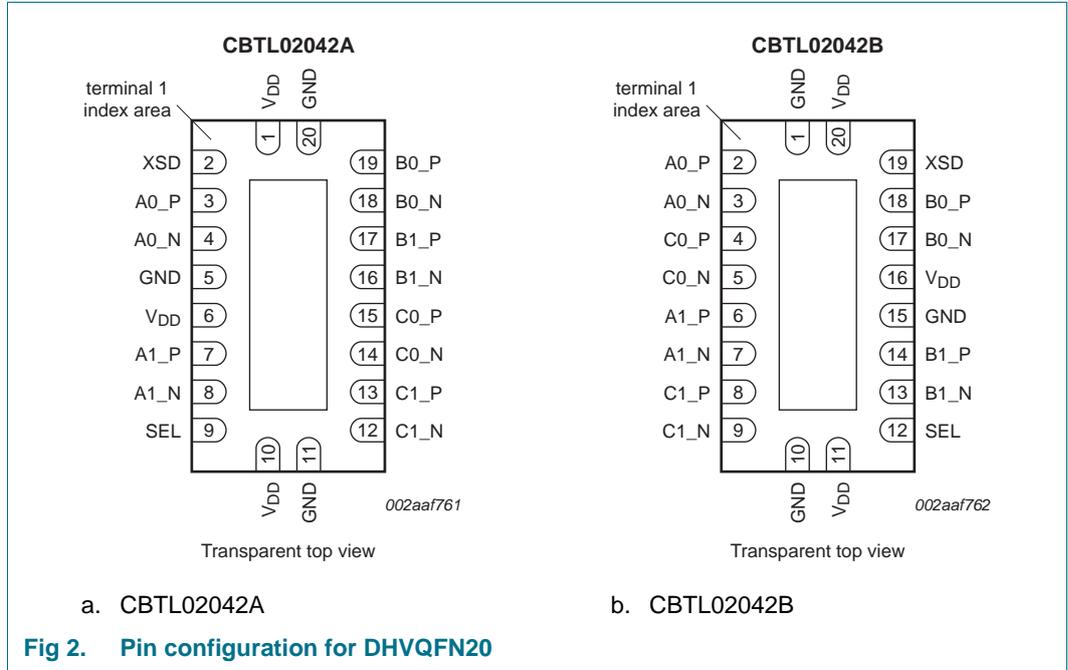


Fig 1. Functional diagram of CBTL02042A; CBTL02042B

6. Pinning information

6.1 Pinning



6.2 Pin description

Table 2. Pin description

| Symbol | Pin | | Type | Description |
|--------|------------|------------|-------------------------|--|
| | CBTL02042A | CBTL02042B | | |
| A0_P | 3 | 2 | I/O | channel 0, port A differential signal input/output |
| A0_N | 4 | 3 | I/O | |
| A1_P | 7 | 6 | I/O | channel 1, port A differential signal input/output |
| A1_N | 8 | 7 | I/O | |
| B0_P | 19 | 18 | I/O | channel 0, port B differential signal input/output |
| B0_N | 18 | 17 | I/O | |
| B1_P | 17 | 14 | I/O | channel 1, port B differential signal input/output |
| B1_N | 16 | 13 | I/O | |
| C0_P | 15 | 4 | I/O | channel 0, port C differential signal input/output |
| C0_N | 14 | 5 | I/O | |
| C1_P | 13 | 8 | I/O | channel 1, port C differential signal input/output |
| C1_N | 12 | 9 | I/O | |
| SEL | 9 | 12 | CMOS single-ended input | operation mode select SEL = LOW: A ↔ B SEL = HIGH: A ↔ C |

Table 2. Pin description ...continued

| Symbol | Pin | | Type | Description |
|--------------------|-----------------------|-----------------------|-------------------------|--|
| | CBTL02042A | CBTL02042B | | |
| XSD | 2 | 19 | CMOS single-ended input | Shutdown pin; should be driven LOW or connected to V _{SS} for normal operation. When HIGH, all paths are switched off (non-conducting high-impedance state), and supply current consumption is minimized. |
| V _{DD} | 1, 6, 10 | 11, 16, 20 | power | positive supply voltage, 3.3 V (± 10 %) |
| GND ^[1] | 5, 11, 20, center pad | 1, 10, 15, center pad | power | supply ground |

[1] DHVQFN20 package die supply ground is connected to both GND pins and exposed center pad. GND pins and the exposed center pad must be connected to supply ground for proper device operation. For enhanced thermal, electrical, and board level performance, the exposed pad needs to be soldered to the board using a corresponding thermal pad on the board and for proper heat conduction through the board, thermal vias need to be incorporated in the printed-circuit board in the thermal pad region.

7. Functional description

Refer to [Figure 1 “Functional diagram of CBTL02042A; CBTL02042B”](#).

7.1 Function selection and shutdown function

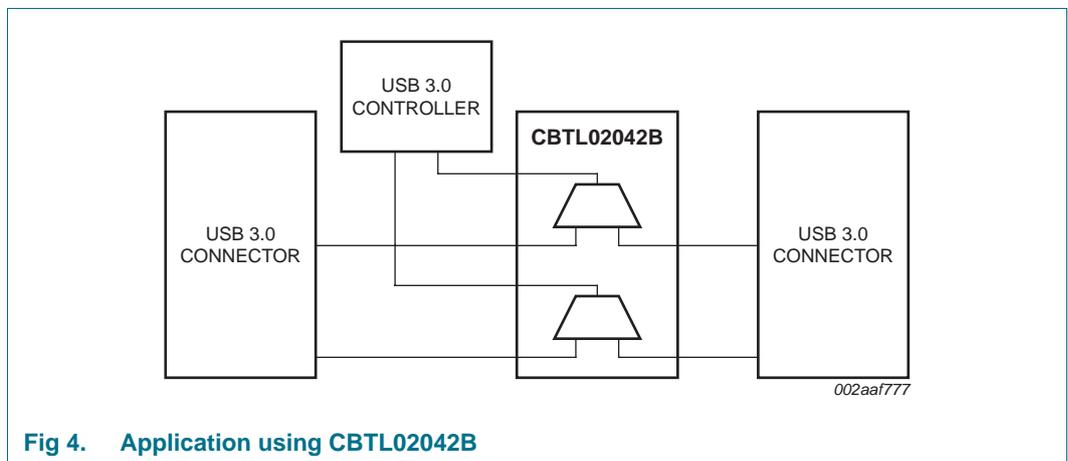
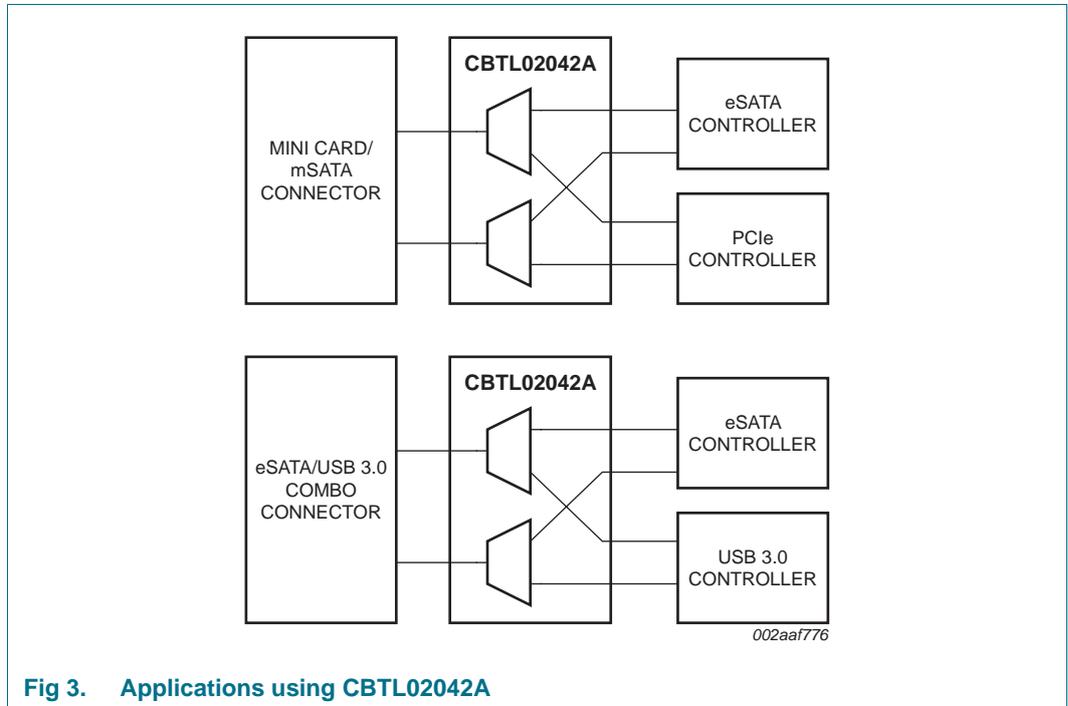
The CBTL02042A/B provides a shutdown function to minimize power consumption when the application is not active, but power to the CBTL02042A/B is provided. The XSD pin (active HIGH) places all channels in high-impedance state (non-conducting) while reducing current consumption to near-zero. When XSD pin is LOW, the device operates normally.

Table 3. Function selection

X = Don't care.

| XSD | SEL | Function |
|------|------|-------------------------------|
| HIGH | X | An, Bn and Cn pins are high-Z |
| LOW | LOW | An to Bn and vice versa |
| LOW | HIGH | An to Cn and vice versa |

8. Application design-in information



9. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

| Symbol | Parameter | Conditions | Min | Max | Unit |
|------------|---------------------------------|------------|-------|------|------|
| V_{DD} | supply voltage | | -0.3 | +4.6 | V |
| T_{case} | case temperature | | -40 | +85 | °C |
| V_{ESD} | electrostatic discharge voltage | HBM | [1] - | 8000 | V |
| | | CDM | [2] - | 1000 | V |

[1] Human Body Model: ANSI/EOS/ESD-S5.1-1994, standard for ESD sensitivity testing, Human Body Model - Component level; Electrostatic Discharge Association, Rome, NY, USA.

[2] Charged Device Model: ANSI/EOS/ESD-S5.3-1-1999, standard for ESD sensitivity testing, Charged Device Model - Component level; Electrostatic Discharge Association, Rome, NY, USA.

10. Recommended operating conditions

Table 5. Recommended operating conditions

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-----------|---------------------|-----------------------|-----|-----|----------|------|
| V_{DD} | supply voltage | | 3.0 | 3.3 | 3.6 | V |
| V_I | input voltage | | - | - | V_{DD} | V |
| T_{amb} | ambient temperature | operating in free air | -40 | - | +85 | °C |

11. Static characteristics

Table 6. Static characteristics

$V_{DD} = 3.3\text{ V} \pm 10\%$; $T_{amb} = -40\text{ °C}$ to $+85\text{ °C}$; unless otherwise specified.

| Symbol | Parameter | Conditions | Min | Typ ^[1] | Max | Unit |
|-----------|----------------------------|--|--------------|--------------------|------------------------|------|
| I_{DD} | supply current | $V_{DD} = \text{max.}; V_I = \text{GND or } V_{DD};$ XSD = LOW | - | 1.35 | 2.5 | mA |
| I_{stb} | standby current | $V_{DD} = \text{max.}; V_I = \text{GND or } V_{DD};$ XSD = HIGH | - | - | 1 | μA |
| I_{IH} | HIGH-level input current | $V_{DD} = \text{max.}; V_I = V_{DD}$ | - | - | ± 5 ^[2] | μA |
| I_{IL} | LOW-level input current | $V_{DD} = \text{max.}; V_I = \text{GND}$ | - | - | ± 5 ^[2] | μA |
| V_{IH} | HIGH-level input voltage | SEL, XSD pins | $0.65V_{DD}$ | - | - | V |
| V_{IL} | LOW-level input voltage | SEL, XSD pins | - | - | $0.35V_{DD}$ | V |
| V_I | input voltage | differential pins | - | - | 2.4 | V |
| | | SEL, XSD pins | - | - | V_{DD} | V |
| V_{IC} | common-mode input voltage | | 0 | - | 2.0 | V |
| V_{ID} | differential input voltage | peak-to-peak | - | - | 1.6 | V |

[1] Typical values are at $V_{DD} = 3.3\text{ V}$, $T_{amb} = 25\text{ °C}$, and maximum loading.

[2] Input leakage current is $\pm 50\text{ μA}$ if differential pairs are pulled to HIGH and LOW.

12. Dynamic characteristics

Table 7. Dynamic characteristics

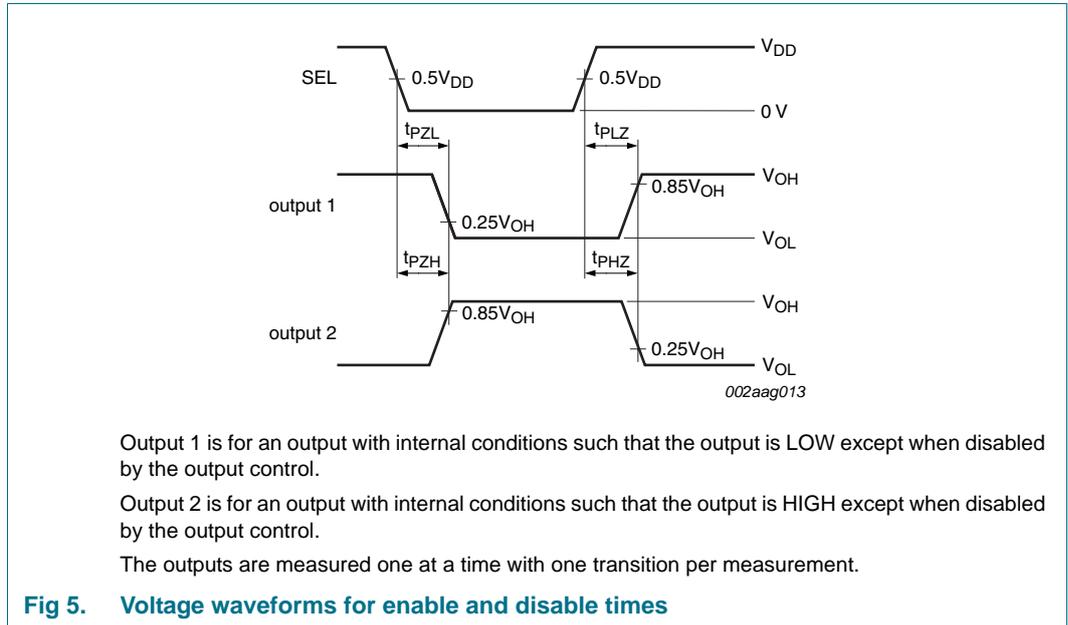
$V_{DD} = 3.3\text{ V} \pm 10\%$; $T_{amb} = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$; unless otherwise specified.

| Symbol | Parameter | Conditions | Min | Typ ^[1] | Max | Unit |
|-------------------|---------------------------------|---|-----|--------------------|-----|----------|
| DDIL | differential insertion loss | channel is OFF | | | | |
| | | f = 100 MHz | - | -50 | - | dB |
| | | f = 2.5 GHz | - | -25 | - | dB |
| | | channel is ON | | | | |
| | | f = 100 MHz | - | -0.5 | - | dB |
| | | f = 2.5 GHz | - | -1.2 | - | dB |
| DDNEXT | differential near-end crosstalk | adjacent channels are ON | | | | |
| | | f = 100 MHz | - | -50 | - | dB |
| | | f = 2.5 GHz | - | -30 | - | dB |
| B _{-3dB} | -3 dB bandwidth | | - | 7.0 | - | GHz |
| DDRL | differential return loss | f = 100 MHz | - | -25 | - | dB |
| | | f = 2.5 GHz | - | -20 | - | dB |
| R _{on} | ON-state resistance | $V_{DD} = 3.3\text{ V}$; $V_I = 2\text{ V}$; $I_I = 19\text{ mA}$ | - | 6 | - | Ω |
| t _{PD} | propagation delay | from Port A to Port B, or Port A to Port C, or vice versa | - | 80 | - | ps |

Switching characteristics

| | | | | | | |
|----------------------|-------------------------------------|--|---|---|-----|----|
| t _{startup} | start-up time | supply voltage valid or XSD going LOW to channel specified operating characteristics | - | - | 10 | ms |
| t _{PZH} | OFF-state to HIGH propagation delay | | - | - | 300 | ns |
| t _{PZL} | OFF-state to LOW propagation delay | | - | - | 70 | ns |
| t _{PHZ} | HIGH to OFF-state propagation delay | | - | - | 50 | ns |
| t _{PLZ} | LOW to OFF-state propagation delay | | - | - | 50 | ns |
| t _{sk(dif)} | differential skew time | intra-pair | - | 5 | - | ps |
| t _{sk} | skew time | inter-pair | - | - | 35 | ps |

[1] Typical values are at $V_{DD} = 3.3\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$, and maximum loading.



13. Test information

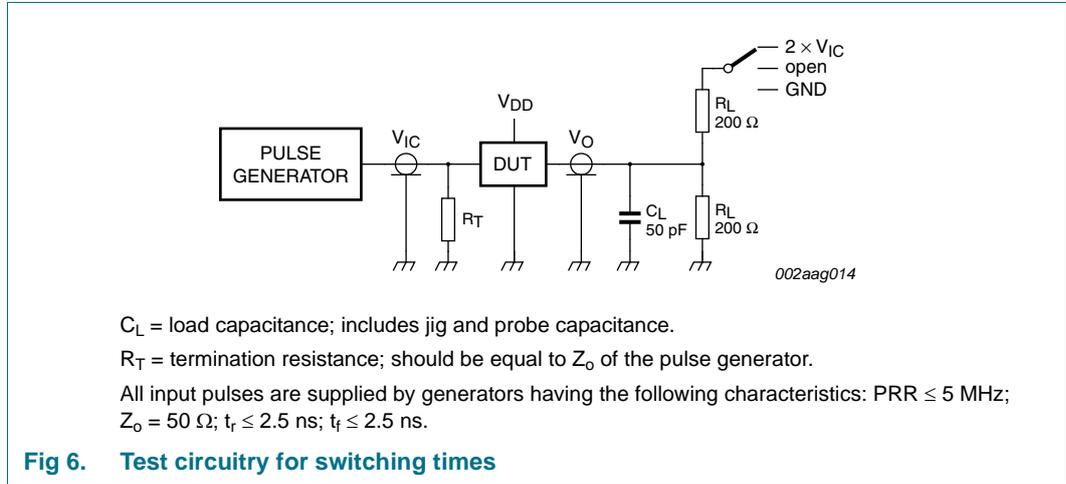


Fig 6. Test circuitry for switching times

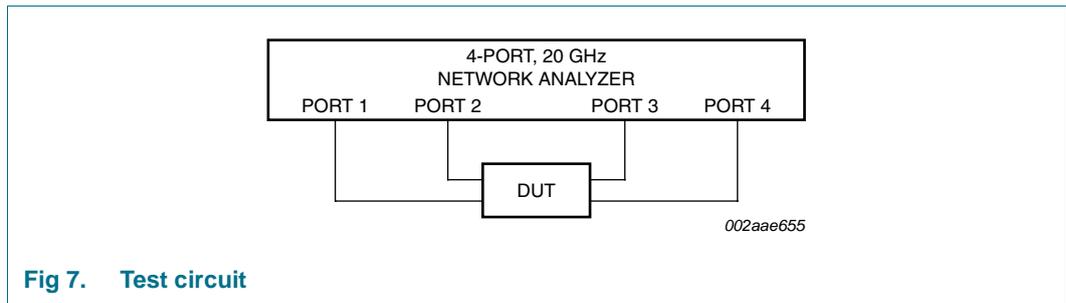


Fig 7. Test circuit

Table 8. Test data

| Test | Load | | Switch |
|--|-------|--------------|-------------------|
| | C_L | R_L | |
| t_{PLZ} , t_{PZL} (output on B side) | 50 pF | 200 Ω | $2 \times V_{IC}$ |
| t_{PHZ} , t_{PZH} (output on B side) | 50 pF | 200 Ω | GND |
| t_{PD} | - | 200 Ω | open |

14. Package outline

DHVQFN20: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body 2.5 x 4.5 x 0.85 mm

SOT764-1

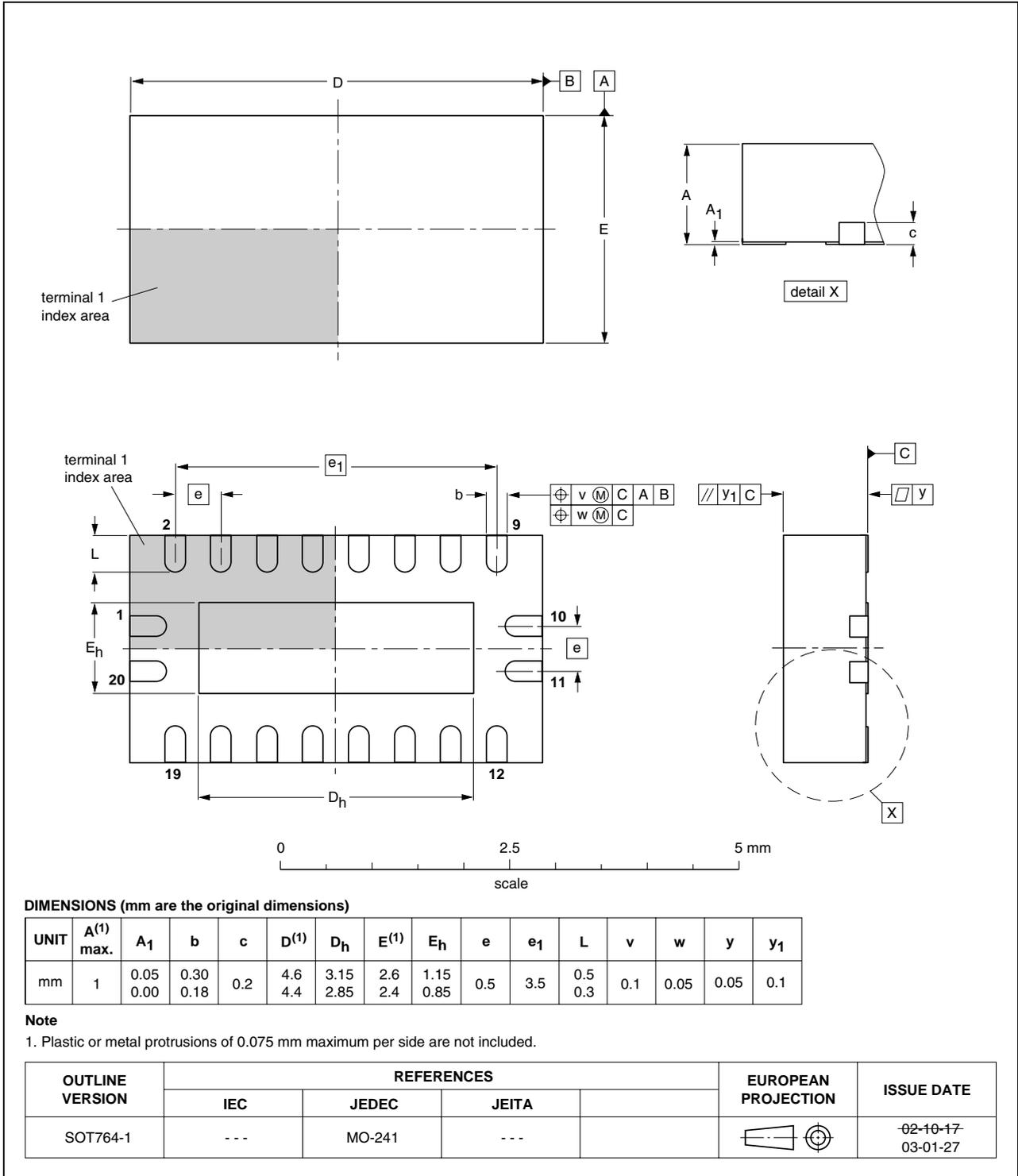


Fig 8. Package outline SOT764-1 (DHVQFN20)

15. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

15.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

15.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

15.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

15.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see [Figure 9](#)) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with [Table 9](#) and [10](#)

Table 9. SnPb eutectic process (from J-STD-020C)

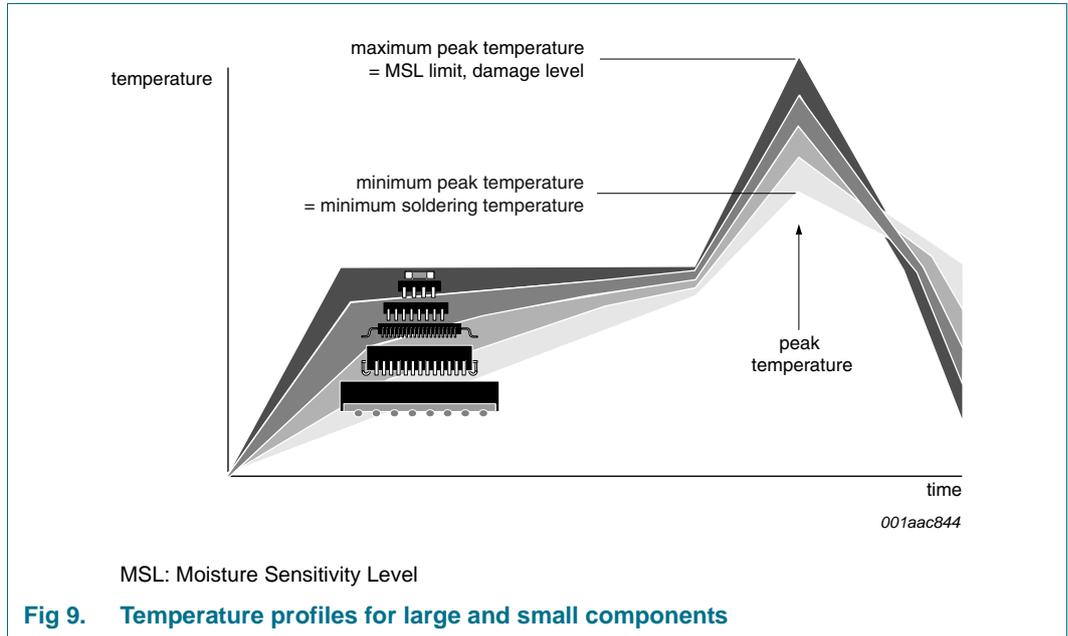
| Package thickness (mm) | Package reflow temperature (°C) | |
|------------------------|---------------------------------|-------|
| | Volume (mm ³) | |
| | < 350 | ≥ 350 |
| < 2.5 | 235 | 220 |
| ≥ 2.5 | 220 | 220 |

Table 10. Lead-free process (from J-STD-020C)

| Package thickness (mm) | Package reflow temperature (°C) | | |
|------------------------|---------------------------------|-------------|--------|
| | Volume (mm ³) | | |
| | < 350 | 350 to 2000 | > 2000 |
| < 1.6 | 260 | 260 | 260 |
| 1.6 to 2.5 | 260 | 250 | 245 |
| > 2.5 | 250 | 245 | 245 |

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see [Figure 9](#).



For further information on temperature profiles, refer to Application Note AN10365 “Surface mount reflow soldering description”.

16. Abbreviations

Table 11. Abbreviations

| Acronym | Description |
|---------|---------------------------------------|
| CDM | Charged-Device Model |
| DUT | Device Under Test |
| ESD | ElectroStatic Discharge |
| HBM | Human Body Model |
| I/O | Input/Output |
| PCI | Peripheral Component Interconnect |
| PCIe | PCI express |
| PRR | Pulse Repetition Rate |
| SATA | Serial Advanced Technology Attachment |
| USB | Universal Serial Bus |

17. Revision history

Table 12. Revision history

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---------------------------|--------------|--------------------|---------------|------------|
| CBTL02042A_CBTL02042B v.1 | 20110310 | Product data sheet | - | - |

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|-----------------------------------|-------------------------------|---|
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