

MC74VHC139

Dual 2-to-4 Decoder/ Demultiplexer

The MC74VHC139 is an advanced high speed CMOS 2-to-4 decoder/ demultiplexer fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

When the device is enabled ($\bar{E} = \text{low}$), it can be used for gating or as a data input for demultiplexing operations. When the enable input is held high, all four outputs are fixed high, independent of other inputs.

The internal circuit is composed of three stages, including a buffer output which provides high noise immunity and stable output. The inputs tolerate voltages up to 7 V, allowing the interface of 5 V systems to 3 V systems.

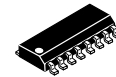
- High Speed: $t_{PD} = 5.0 \text{ ns (Typ)}$ at $V_{CC} = 5 \text{ V}$
- Low Power Dissipation: $I_{CC} = 4 \mu\text{A (Max)}$ at $T_A = 25^\circ\text{C}$
- High Noise Immunity: $V_{NIH} = V_{NIL} = 28\% V_{CC}$
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Designed for 2 V to 5.5 V Operating Range
- Low Noise: $V_{OLP} = 0.8 \text{ V (Max)}$
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300 mA
- ESD Performance: Human Body Model > 2000 V;
Machine Model > 200 V
- Chip Complexity: 100 FETs or 25 Equivalent Gates
- These Devices are Pb-Free and are RoHS Compliant



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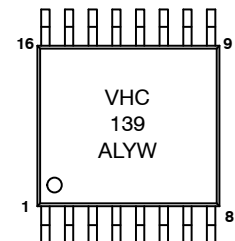
MARKING DIAGRAMS



**SOIC-16
D SUFFIX
CASE 751B**

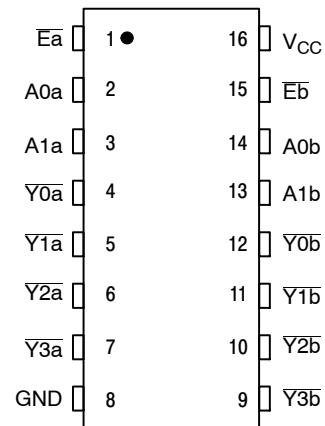


**TSSOP-16
DT SUFFIX
CASE 948F**



A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week

PIN ASSIGNMENT



ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 6 of this data sheet.

MC74VHC139

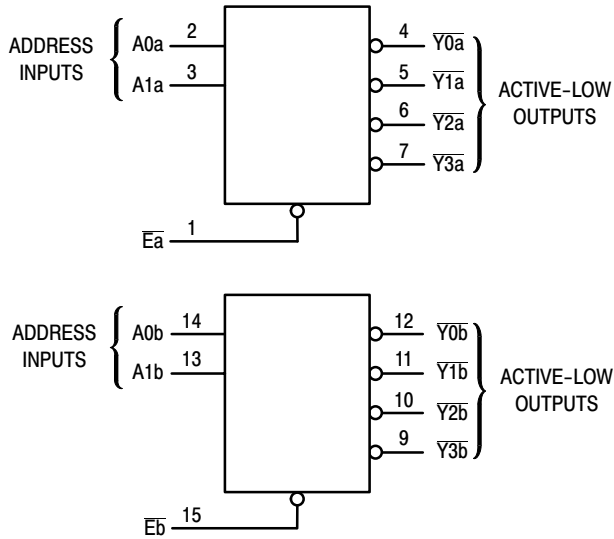


Figure 1. Logic Diagram

Table 1. FUNCTION TABLE

Inputs			Outputs			
E	A1	A0	$\overline{Y0}$	$\overline{Y1}$	$\overline{Y2}$	$\overline{Y3}$
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

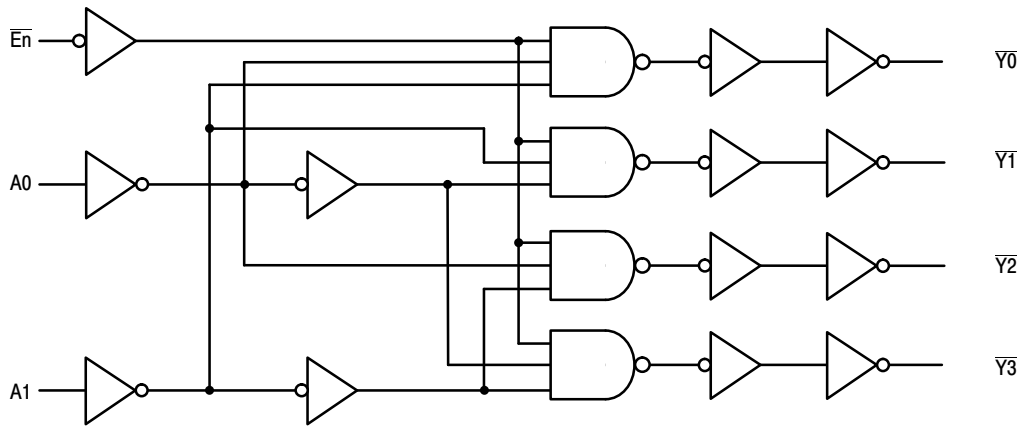


Figure 2. Expanded Logic Diagram
(1/2 of Device)

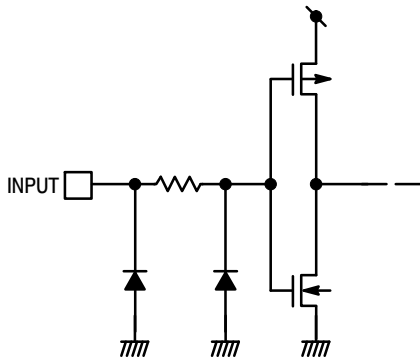


Figure 3. Input Equivalent Circuit

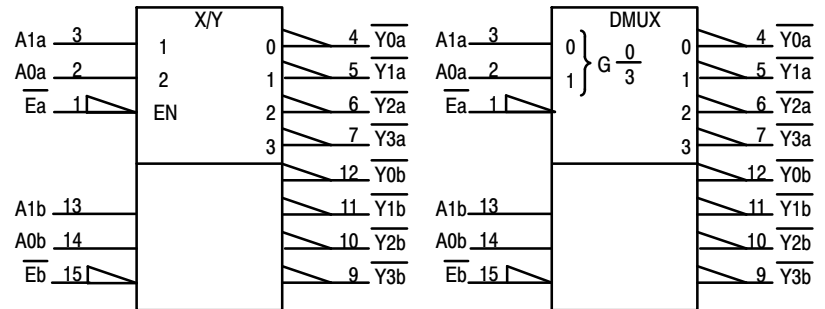
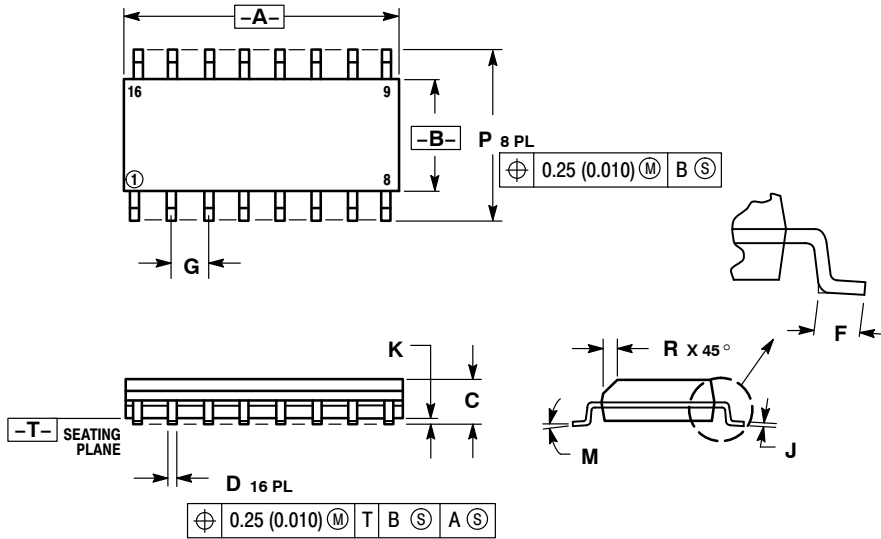


Figure 4. IEC Logic Diagram

MC74VHC139

PACKAGE DIMENSIONS

SOIC-16
CASE 751B-05
ISSUE K

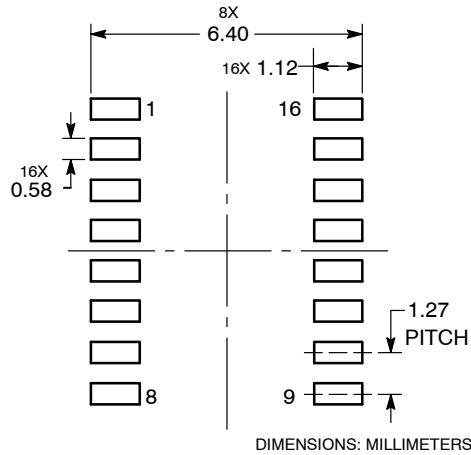


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

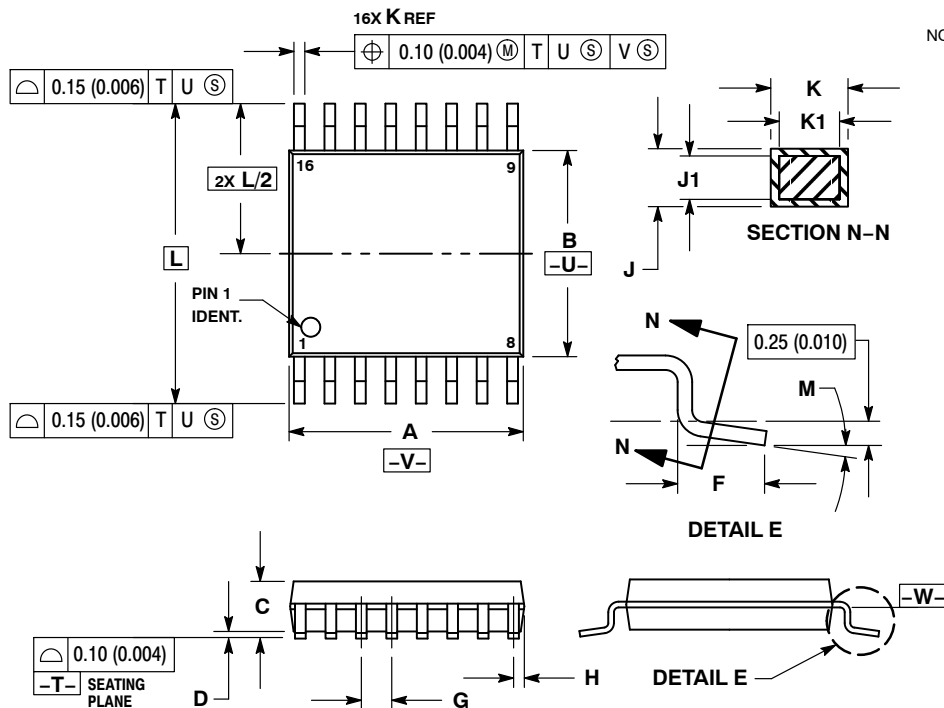
SOLDERING FOOTPRINT



MC74VHC139

PACKAGE DIMENSIONS

TSSOP-16
CASE 948F-01
ISSUE B

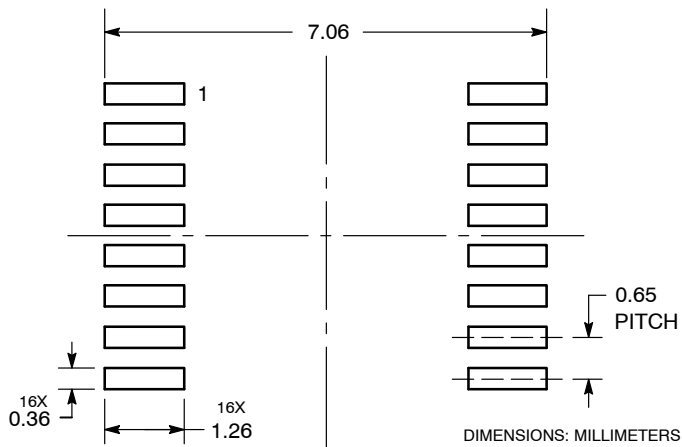


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

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