

NTMD4820N

Power MOSFET

30 V, 8 A, Dual N-Channel, SOIC-8

Features

- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Capacitance to Minimize Driver Losses
- Optimized Gate Charge to Minimize Switching Losses
- Dual SOIC-8 Surface Mount Package Saves Board Space

Applications

- Disk Drives
- DC-DC Converters
- Printers

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise stated)

Rating			Symbol	Value	Unit
Drain-to-Source Voltage			V_{DS}	30	V
Gate-to-Source Voltage			V_{GS}	± 20	V
Continuous Drain Current $R_{\theta JA}$ (Note 1)	Steady State	$T_A = 25^\circ\text{C}$	I_D	6.4	A
		$T_A = 70^\circ\text{C}$		5.1	
		$T_A = 25^\circ\text{C}$	P_D	1.28	W
		$T_A = 25^\circ\text{C}$	I_D	4.9	A
		$T_A = 70^\circ\text{C}$		3.9	
		$T_A = 25^\circ\text{C}$	P_D	0.75	W
		$T_A = 25^\circ\text{C}$	I_D	8.0	A
		$T_A = 70^\circ\text{C}$		6.4	
		$T_A = 25^\circ\text{C}$	P_D	2.0	W
		$T_A = 25^\circ\text{C}$			
Power Dissipation $R_{\theta JA}$ (Note 1)		$T_A = 25^\circ\text{C}$			
Continuous Drain Current $R_{\theta JA}$ (Note 2)		$T_A = 25^\circ\text{C}$			
Power Dissipation $R_{\theta JA}$ (Note 2)		$T_A = 25^\circ\text{C}$			
Continuous Drain Current $R_{\theta JA}$ $t < 10$ s (Note 1)		$T_A = 25^\circ\text{C}$			
Power Dissipation $R_{\theta JA}$ $t < 10$ s (Note 1)		$T_A = 25^\circ\text{C}$			
Pulsed Drain Current	$T_A = 25^\circ\text{C}$, $t_p = 10 \mu\text{s}$		I_{DM}	32	A
Operating Junction and Storage Temperature			T_J, T_{STG}	-55 to +150	$^\circ\text{C}$
Source Current (Body Diode)			I_S	2.0	A
Single Pulse Drain-to-Source Avalanche Energy $T_J = 25^\circ\text{C}$, $V_{DD} = 30$ V, $V_{GS} = 10$ V, $I_L = 11$ A _{pk} , $L = 1.0$ mH, $R_G = 25 \Omega$			EAS	60.5	mJ
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)			T_L	260	$^\circ\text{C}$

THERMAL RESISTANCE RATINGS

Rating	Symbol	Max	Unit
Junction-to-Ambient – Steady State (Note 1)	$R_{\theta JA}$	97.5	$^\circ\text{C/W}$
Junction-to-Ambient – $t \leq 10$ s (Note 1)	$R_{\theta JA}$	62	
Junction-to-FOOT (Drain)	$R_{\theta JF}$	40	
Junction-to-Ambient – Steady State (Note 2)	$R_{\theta JA}$	167.5	

1. Surface-mounted on FR4 board using 1 inch sq pad size, 1 oz Cu.
2. Surface-mounted on FR4 board using the minimum recommended pad size.

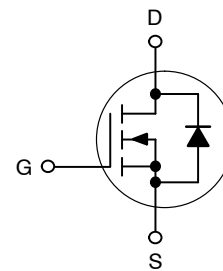


ON Semiconductor®

<http://onsemi.com>

$V_{(BR)DSS}$	$R_{DS(on)}$ Max	I_D Max
30 V	20 m Ω @ 10 V	8 A
	27 m Ω @ 4.5 V	

N-Channel



MARKING DIAGRAM & PIN ASSIGNMENT



4820N = Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb-Free Package

ORDERING INFORMATION

Device	Package	Shipping†
NTMD4820NR2G	SOIC-8 (Pb-Free)	2500/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

NTMD4820N

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)jk

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0 V, I _D = 250 μA	30			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V _{(BR)DSS} /T _J			26		mV/°C
Zero Gate Voltage Drain Current	I _{DSS}	V _{GS} = 0 V, V _{DS} = 24 V			1.0	μA
		T _J = 25°C				
		T _J = 100°C			10	
Gate-to-Source Leakage Current	I _{GSS}	V _{DS} = 0 V, V _{GS} = ±20 V			±100	nA

ON CHARACTERISTICS (Note 3)

Gate Threshold Voltage	V _{GS(TH)}	V _{GS} = V _{DS} , I _D = 250 μA	1.5		3.0	V
Negative Threshold Temperature Coefficient	V _{GS(TH)} /T _J			5.0		mV/°C
Drain-to-Source On Resistance	R _{DS(on)}	V _{GS} = 10 V, I _D = 7.5 A		15	20	mΩ
		V _{GS} = 4.5 V, I _D = 6.5 A		20	27	
Forward Transconductance	g _{FS}	V _{DS} = 1.5 V, I _D = 7.5 A		21		S

CHARGES, CAPACITANCES AND GATE RESISTANCE

Input Capacitance	C _{ISS}	V _{GS} = 0 V, f = 1.0 MHz, V _{DS} = 15 V		940		pF
Output Capacitance	C _{OSS}			225		
Reverse Transfer Capacitance	C _{RSS}			125		
Total Gate Charge	Q _{G(TOT)}	V _{GS} = 4.5 V, V _{DS} = 15 V, I _D = 7.5 A		7.7		nC
Threshold Gate Charge	Q _{G(TH)}			1.1		
Gate-to-Source Charge	Q _{GS}			3.3		
Gate-to-Drain Charge	Q _{GD}			3.2		
Total Gate Charge	Q _{G(TOT)}	V _{GS} = 10 V, V _{DS} = 15 V, I _D = 7.5 A		15.2		nC

SWITCHING CHARACTERISTICS (Note 4)

Turn-On Delay Time	t _{d(ON)}	V _{GS} = 10 V, V _{DD} = 15 V, I _D = 1.0 A, R _G = 6.0 Ω		9.4		ns
Rise Time	t _r			4.0		
Turn-Off Delay Time	t _{d(OFF)}			21		
Fall Time	t _f			6.5		

DRAIN-TO-SOURCE CHARACTERISTICS

Forward Diode Voltage	V _{SD}	V _{GS} = 0 V, I _D = 2.0 A	T _J = 25°C		0.75	1.0	V
			T _J = 125°C		0.59		
Reverse Recovery Time	t _{RR}	V _{GS} = 0 V, dI _S /dt = 100 A/μs, I _S = 2.0 A		17.8			ns
Charge Time	T _a			8.3			
Discharge Time	T _b			9.5			
Reverse Recovery Time	Q _{RR}			8.0			nC

PACKAGE PARASITIC VALUES

Source Inductance	L _S	T _A = 25°C		0.66		nH
Drain Inductance	L _D			0.20		nH
Gate Inductance	L _G			1.50		nH
Gate Resistance	R _G			1.5	3.0	Ω

3. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.

4. Switching characteristics are independent of operating junction temperatures.

TYPICAL PERFORMANCE CURVES

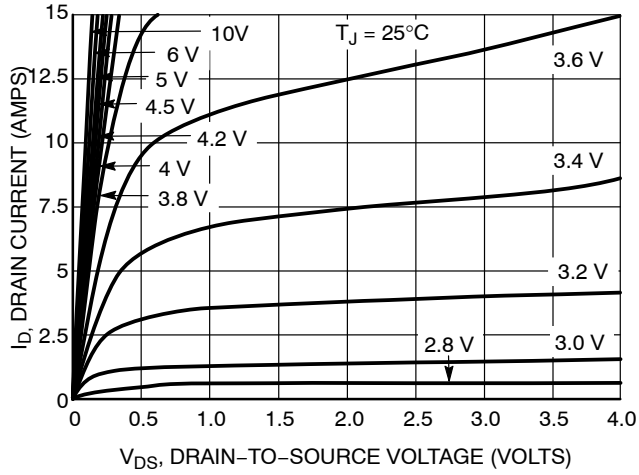


Figure 1. On-Region Characteristics

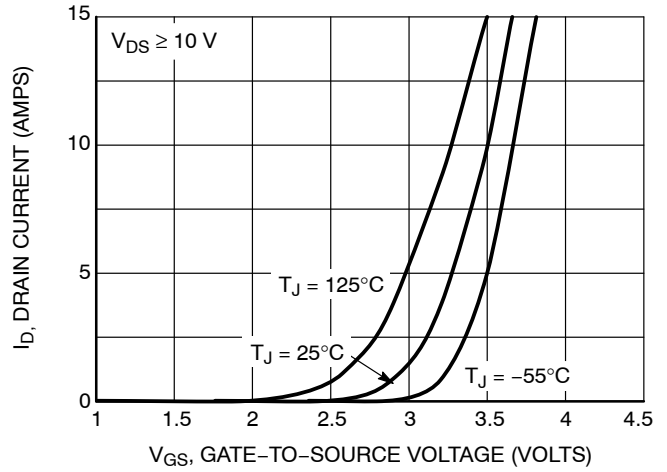


Figure 2. Transfer Characteristics

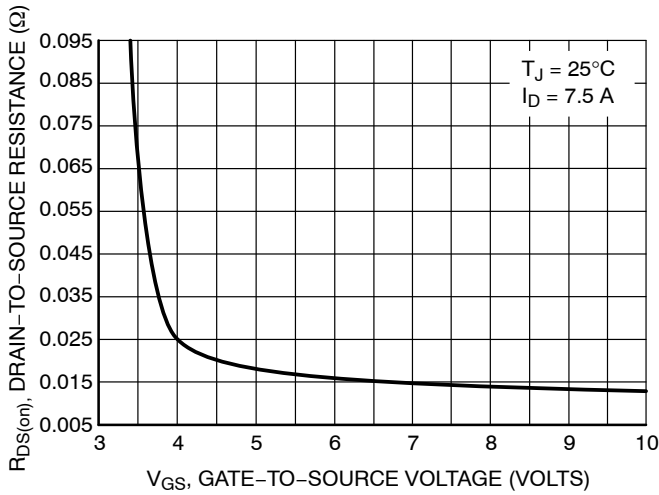


Figure 3. On-Resistance vs. Gate-to-Source Voltage

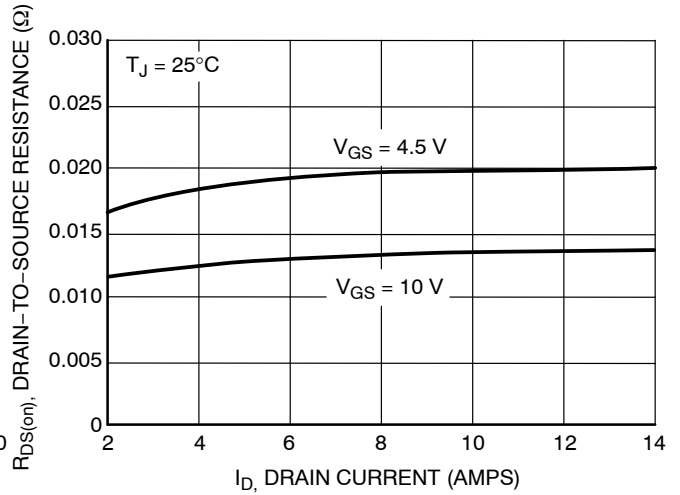


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

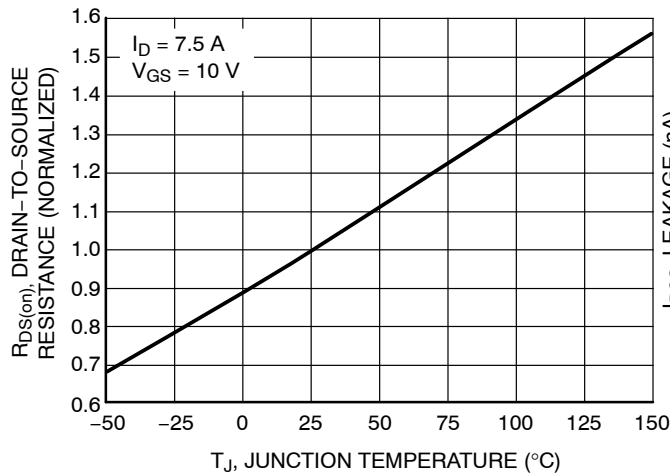


Figure 5. On-Resistance Variation with Temperature

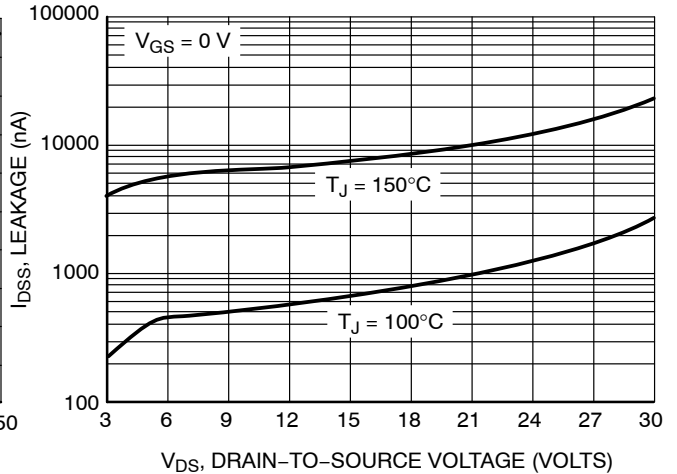


Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL PERFORMANCE CURVES

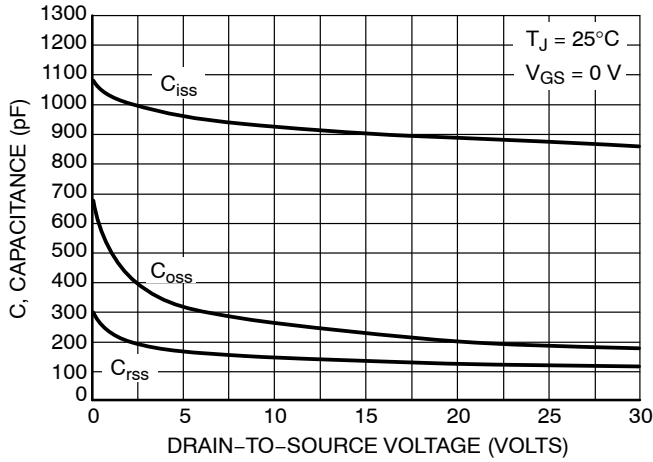


Figure 7. Capacitance Variation

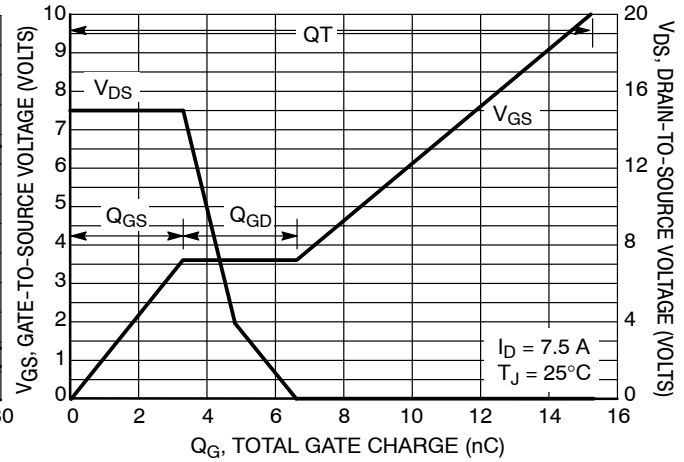


Figure 8. Gate-To-Source and Drain-To-Source Voltage vs. Total Charge

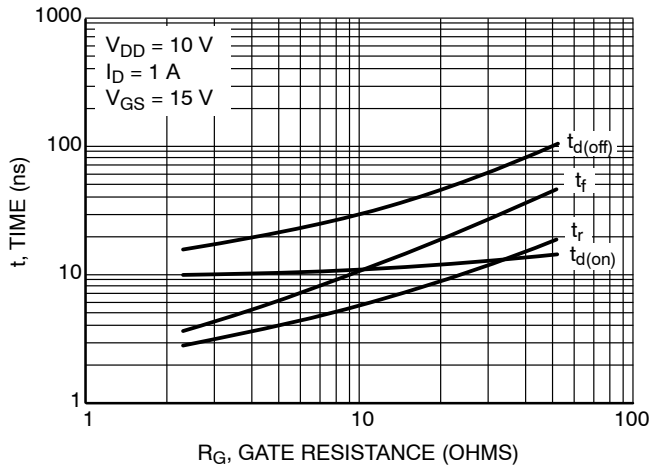


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

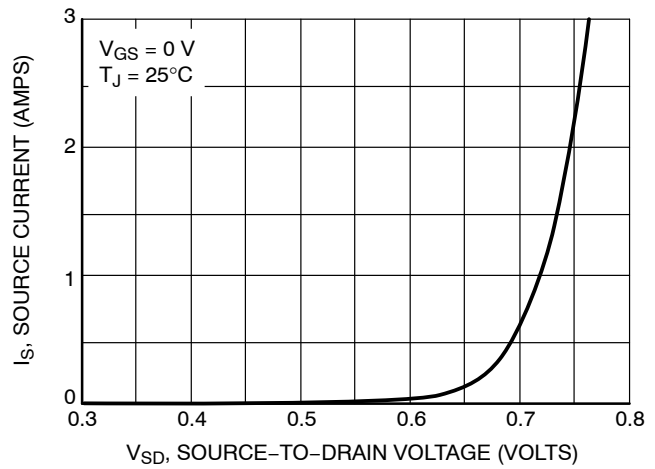


Figure 10. Diode Forward Voltage vs. Current

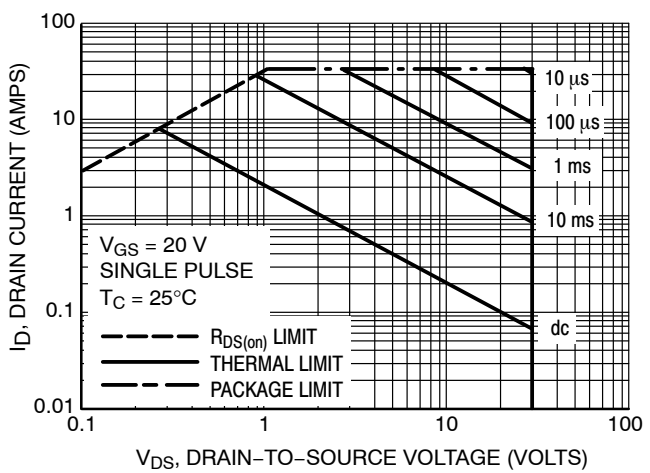


Figure 11. Maximum Rated Forward Biased Safe Operating Area

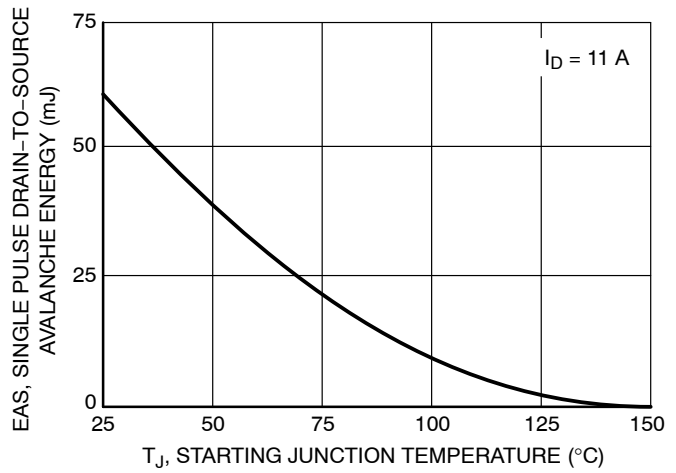
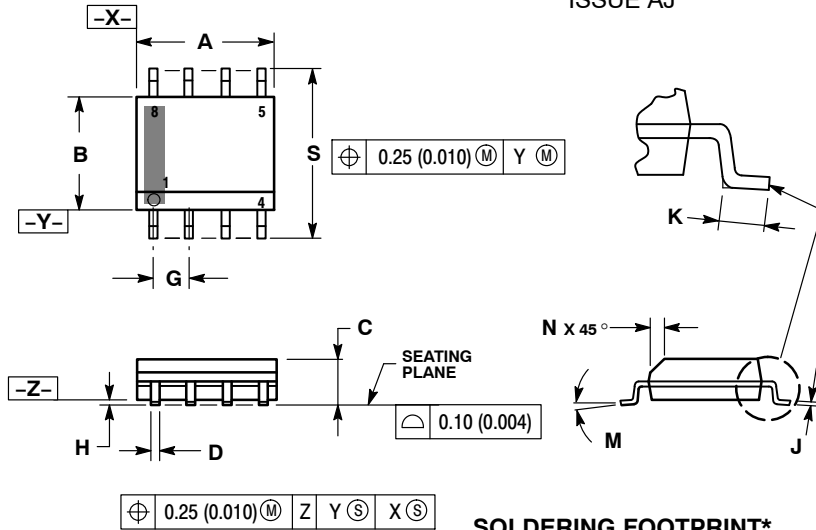


Figure 12. Maximum Avalanche Energy vs. Starting Junction Temperature

NTMD4820N

PACKAGE DIMENSIONS

SOIC-8 NB CASE 751-07 ISSUE AJ

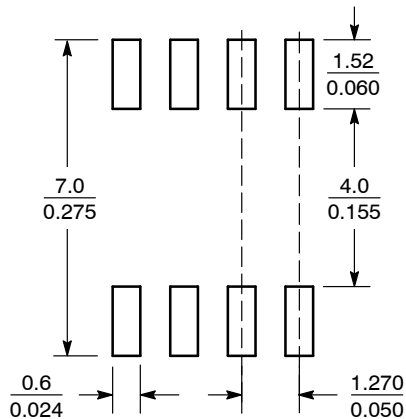


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

SOLDERING FOOTPRINT*



SCALE 6:1 (mm/inches)

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

STYLE 11:

- PIN 1. SOURCE 1
- GATE 1
- SOURCE 2
- GATE 2
- DRAIN 2
- DRAIN 2
- DRAIN 1
- DRAIN 1

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