MC10H640

68030/040 PECL to TTL Clock Driver

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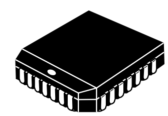


PLLC−28
FN SUFFIX
CASE 776−02

Description

The MC10H640 generates the necessary clocks for the 68030, 68040 and similar microprocessors. It is guaranteed to meet the clock specifications required by the 68030 and 68040 in terms of part-to-part skew, within-part skew and also duty cycle skew.

The user has a choice of using either TTL or PECL (ECL referenced to +5.0 V) for the input clock. TTL clocks are typically used in present MPU systems. However, as clock speeds increase to 50 MHz and beyond, the inherent superiority of ECL (particularly differential ECL) as a means of clock signal distribution becomes increasingly evident. The H640 also uses differential PECL internally to achieve its superior skew characteristic.

The H640 includes divide-by-two and divide-by-four stages, both to achieve the necessary duty cycle skew and to generate MPU clocks as required. A typical 50 MHz processor application would use an input clock running at 100 MHz, thus obtaining output clocks at 50 MHz and 25 MHz (see Logic Diagram).

Features

- Generates Clocks for 68030/040
- Meets 030/040 Skew Requirements
- TTL or PECL Input Clock
- Extra TTL and PECL Power/Ground Pins
- Asynchronous Reset
- Single +5.0 V Supply
- This Device is Pb-Free, Halogen Free and is RoHS Compliant

Function

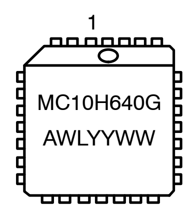
Reset (R): LOW on RESET forces all Q outputs LOW and all $\overline{Q}$ outputs HIGH.

Power-Up: The device is designed to have the POS edges of the ÷ 2 and ÷ 4 outputs synchronized at power up.

Select (SEL): LOW selects the ECL input source (DE/$\overline{DE}$). HIGH selects the TTL input source (DT).

The H640 also contains circuitry to force a stable state of the ECL input differential pair, should both sides be left open. In this case, the DE side of the input is pulled LOW, and $\overline{DE}$ goes HIGH.

MARKING DIAGRAM*



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb-Free Package

*For additional marking information, refer to Application Note AND8002/D.

ORDERING INFORMATION

Device	Package	Shipping
MC10H640FNG	PLLC−28 (Pb-Free)	37 Units / Tube

August, 2016 − Rev. 9

Publication Order Number:
MC10H640/D

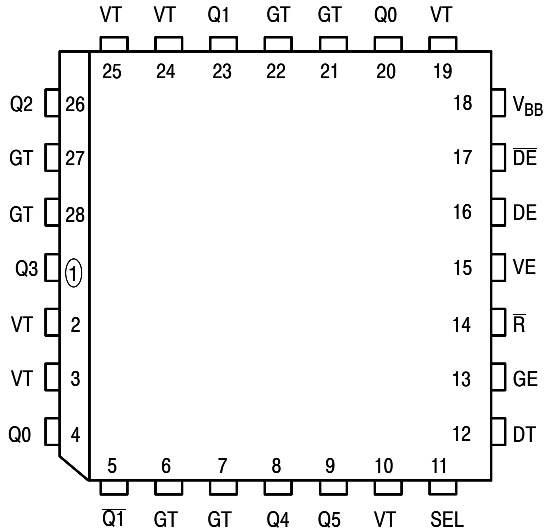


Figure 1. Pinout: PLCC−28
(Top View)

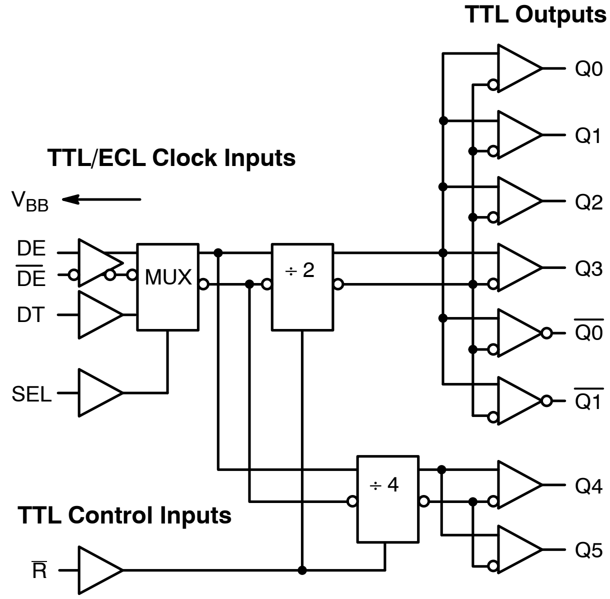


Figure 2. Logic Diagram

Table 1. PIN DESCRIPTION

PIN	FUNCTION
GT	TTL Ground (0 V)
VT	TTL V_{CC} (+5.0 V)
VE	ECL V_{CC} (+5.0 V)
GE	ECL Ground (0 V)
DE, $\overline{DE}$	ECL Signal Input (positive ECL)
V_{BB}	V_{BB} Reference Output
DT	TTL Signal Input
Qn, $\overline{Qn}$	Signal Outputs (TTL)
SEL	Input Select (TTL)
$\overline{R}$	Reset (TTL)

Table 2. DC CHARACTERISTICS ($V_T = V_E = 5.0$ V ±5%)

Symbol	Characteristic		Condition	0°C		25°C		85°C		Unit
				Min	Max	Min	Max	Min	Max	
I_{EE}	Power Supply Current	ECL	VE Pin		57		57		57	mA
I_{CCH}		TTL	Total all VT pins		30		30		30	mA
I_{CCL}					30		30		30	mA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

Table 3. 10H PECL DC CHARACTERISTICS ($V_T = V_E = 5.0\ V \pm 5\%$)

Symbol	Characteristic	Condition	0°C		25°C		85°C		Unit
			Min	Max	Min	Max	Min	Max	
I_{INH}	Input HIGH Current			255		175		175	μA
I_{INL}	Input LOW Current		0.5		0.5		0.5		
$V_{IH}1$	Input HIGH Voltage	$V_E = 5.0\ V$	3.83	4.16	3.87	4.19	3.94	4.28	V
$V_{IL}1$	Input LOW Voltage		3.05	3.52	3.05	3.52	3.05	3.555	
$V_{BB}1$	Output Reference Voltage		3.62	3.73	3.65	3.75	3.69	3.81	V

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

1. PECL levels are referenced to V_{CC} and will vary 1:1 with the power supply. The values shown are for $V_{CC} = 5.0V$.

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Table 4. TTL DC CHARACTERISTICS ($V_T = V_E = 5.0\ V \pm 5\%$)

Symbol	Characteristic	Condition	0°C		25°C		85°C		Unit
			Min	Max	Min	Max	Min	Max	
V_{IH}	Input HIGH Voltage		2.0		2.0		2.0		V
V_{IL}	Input LOW Voltage			0.8		0.8		0.8	
I_{IH}	Input HIGH Current	$V_{IN} = 2.7\ V$		20		20		20	μA
		$V_{IN} = 7.0\ V$		100		100		100	
I_{IL}	Input LOW Current	$V_{IN} = 0.5\ V$		−0.6		−0.6		−0.6	mA
V_{OH}	Output HIGH Voltage	$I_{OH} = -3.0\ mA$	2.5		2.5		2.5		V
		$I_{OH} = -15\ mA$	2.0		2.0		2.0		
V_{OL}	Output LOW Voltage	$I_{OL} = 24\ mA$		0.5		0.5		0.5	V
V_{IK}	Input Clamp Voltage	$I_{IN} = -18\ mA$		−1.2		−1.2		−1.2	V
I_{OS}	Output Short Circuit Current	$V_{OUT} = 0\ V$	−100	−225	−100	−225	−100	−225	mA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

Table 5. AC CHARACTERISTICS ($V_T = V_E$ = 5.0 V ±5%)

Symbol	Characteristic		Condition	0°C Min	0°C Max	25°C Min	25°C Max	85°C Min	85°C Max	Unit
t_{PLH}	Propagation Delay ECL D to Output	Q0 – Q3	CL = 25 pF	4.0	6.0	4.0	6.0	4.2	6.2	ns
t_{PLH}	Propagation Delay TTL D to Output		CL = 25 pF	4.0	6.0	4.0	6.0	4.3	6.3	ns
tskwd*	Within-Device Skew		CL = 25 pF		0.5		0.5		0.5	ns
t_{PLH}	Propagation Delay ECL D to Output	$\overline{Q0}$, $\overline{Q1}$	CL = 25 pF	4.0	6.0	4.0	6.0	4.2	6.2	ns
t_{PLH}	Propagation Delay TTL D to Output		CL = 25 pF	4.0	6.0	4.0	6.0	4.3	6.3	ns
t_{PLH}	Propagation Delay ECL D to Output	Q4, Q5	CL = 25 pF	4.0	6.0	4.0	6.0	4.2	6.2	ns
t_{PLH}	Propagation Delay TTL D to Output		CL = 25 pF	4.0	6.0	4.0	6.0	4.3	6.3	ns
t_{PD}	Propagation Delay R to Output	All Outputs	CL = 25 pF	4.3	6.3	4.3	6.3	5.0	7.0	ns
t_R t_F	Output Rise/Fall Time 0.8 V to 2.0 V	All Outputs	CL = 25 pF		2.5 2.5		2.5 2.5		2.5 2.5	ns
f_{max}	Maximum Input Frequency		CL = 25 pF	135		135		135		MHz
t_{pw}	Minimum Pulse Width			1.50		1.50		1.50		ns
t_{rr}	Reset Recovery Time			1.25		1.25		1.25		ns

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

1. Within-Device Skew defined as identical transitions on similar paths through a device.

Table 6. V_{CC} and C_L RANGES TO MEET DUTY CYCLE REQUIREMENTS
(0°C ≤ T_A ≤ 85°C Output Duty Cycle Measured Relative to 1.5 V)

Symbol	Characteristic		Condition	Min	Nom	Max	Unit
	Range of V_{CC} and CL to meet minimum pulse width (HIGH or LOW) = 11.5 ns at f_{out} ≤ 40 MHz	V_{CC} CL	Q0 – Q3 $\overline{Q0}$ – $\overline{Q1}$	4.75 10	5.0	5.25 50	V pF
	Range of V_{CC} and CL to meet minimum pulse width (HIGH or LOW) = 9.5 ns at 40 < f_{out} ≤ 50 MHz	V_{CC} CL	Q0 – Q3	4.875 15	5.0	5.125 27	V pF

10H640
DUTY CYCLE CONTROL

To maintain a duty cycle of ±5% at 50MHz, limit the load capacitance and/or power supply variation as shown in Figures 3 and 4. Figure 5 shows typical TPD versus load. Figure 6 shows reset recovery time. Figure 7 shows output states after power up. Best duty cycle control is obtained with a single μP load and minimum line length.

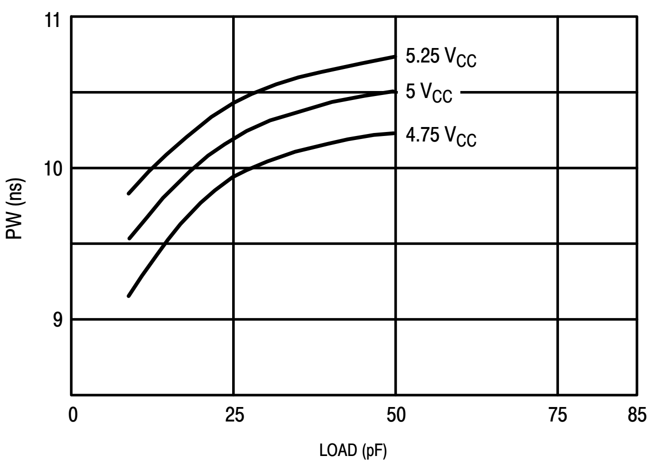


Figure 3. Positive Pulse Width at 25°C Ambient and 50 MHz Out

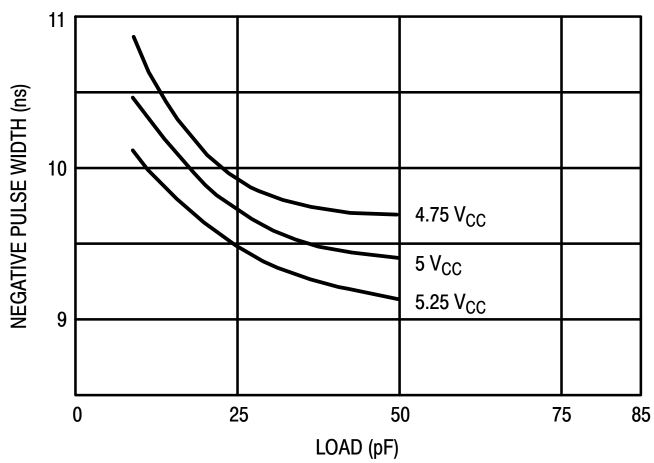


Figure 4. Negative Pulse Width at 25°C Ambient and 50 MHz Out

Resource Reference of Application Notes

AN1405/D	–	ECL Clock Distribution Techniques
AN1406/D	–	Designing with PECL (ECL at +5.0 V)
AN1503/D	–	ECLinPS™ I/O SPiCE Modeling Kit
AN1504/D	–	Metastability and the ECLinPS Family
AN1568/D	–	Interfacing Between LVDS and ECL
AN1672/D	–	The ECL Translator Guide
AND8001/D	–	Odd Number Counters Design
AND8002/D	–	Marking and Date Codes
AND8020/D	–	Termination of ECL Logic Devices
AND8066/D	–	Interfacing with ECLinPS
AND8090/D	–	AC Characteristics of ECL Devices

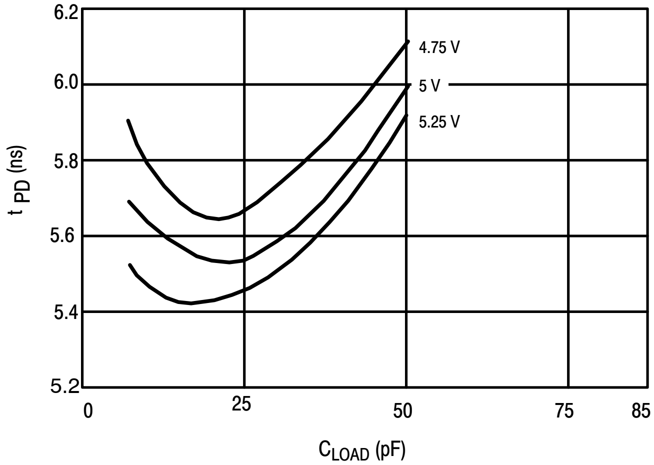


Figure 5. t_{PD} versus Load Typical at T_A = 25°C

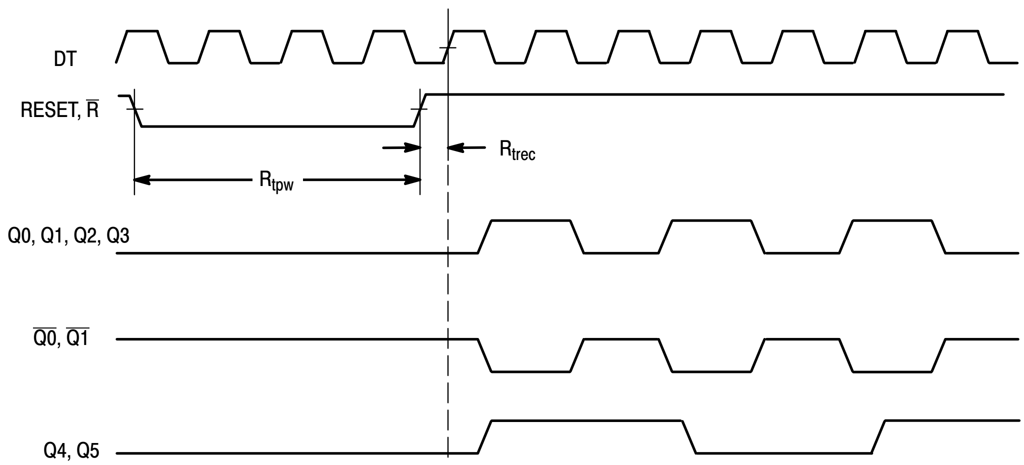
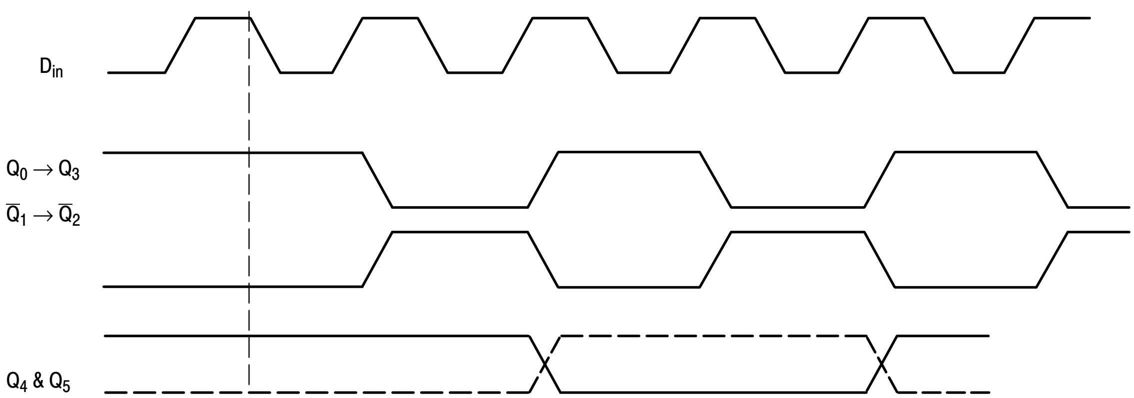


Figure 6. MC10H640 Clock Phase and Reset Recovery Time After Reset Pulse

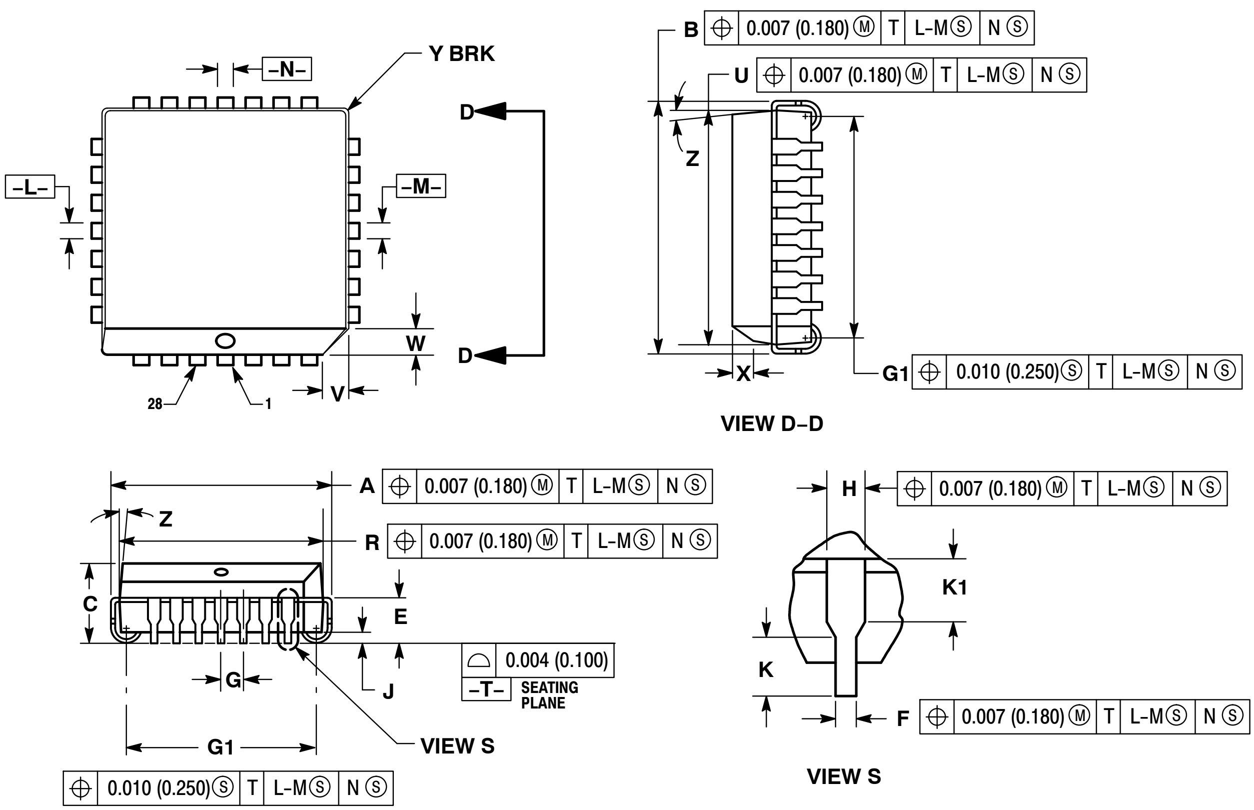


AFTER POWER UP
OUTPUTS Q_4 & Q_5 WILL SYNC WITH POSITIVE EDGES OF D_{in} & $Q_0 \rightarrow Q_3$ & NEGATIVE EDGES OF $\overline{Q}_0$ & $\overline{Q}_1$

Figure 7. Output Timing Diagram

PACKAGE DIMENSIONS

28 LEAD PLLC
FN SUFFIX
CASE 776−02
ISSUE F



NOTES:
1. DATUMS -L-, -M-, AND -N- DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
2. DIMENSION G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
3. DIMENSIONS R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
5. CONTROLLING DIMENSION: INCH.
6. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
7. DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.485	0.495	12.32	12.57
B	0.485	0.495	12.32	12.57
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.021	0.33	0.53
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	---	0.51	---
K	0.025	---	0.64	---
R	0.450	0.456	11.43	11.58
U	0.450	0.456	11.43	11.58
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	---	0.020	---	0.50
Z	2°	10°	2°	10°
G1	0.410	0.430	10.42	10.92
K1	0.040	---	1.02	---

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
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