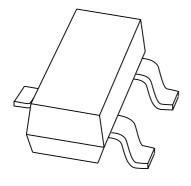
DISCRETE SEMICONDUCTORS

DATA SHEET



PBSS4130T 30 V, 1 A NPN low V_{CEsat} (BISS) transistor

Product specification

2003 Nov 27





30 V, 1 A NPN low V_{CEsat} (BISS) transistor

PBSS4130T

FEATURES

- Low collector-emitter saturation voltage V_{CEsat}
- High collector current capability I_C and I_{CM}
- · High efficiency leading to less heat generation
- Reduced printed-circuit board requirements
- Cost effective alternative to MOSFETs in specific applications.

APPLICATIONS

- · Power management
 - DC/DC conversion
 - Supply line switching
 - Battery charger
 - LCD backlighting.
- · Peripheral driver
 - Driver in low supply voltage applications (e.g. lamps and LEDs)
 - Inductive load drivers (e.g. relays, buzzers and motors).

DESCRIPTION

NPN BISS transistor in a SOT23 plastic package providing ultra low V_{CEsat} and R_{CEsat} parameters. PNP complement: PBSS5130T.

MARKING

TYPE NUMBER	MARKING CODE(1)
PBSS4130T	*3C

Note

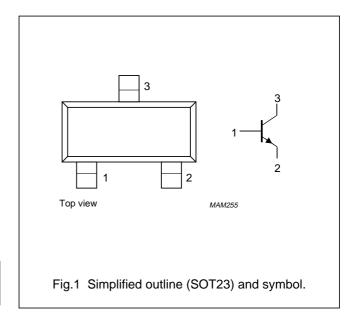
- 1. * = p: made in Hong Kong.
 - * = t: made in Malaysia.
 - * = W: made in China.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V _{CEO}	collector-emitter voltage	30	٧
I _C	collector current (DC)	1	Α
I _{CM}	peak collector current	3	Α
R _{CEsat}	equivalent on-resistance	220	mΩ

PINNING

PIN	DESCRIPTION
1	base
2	emitter
3	collector



ORDERING INFORMATION

TYPE NUMBER	PACKAGE					
TIPE NOMBER	NAME	NAME DESCRIPTION VERSIO				
PBSS4130T	_	plastic surface mounted package; 3 leads	SOT23			

30 V, 1 A NPN low V_{CEsat} (BISS) transistor

PBSS4130T

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V _{CBO}	collector-base voltage	open emitter	_	40	V
V _{CEO}	collector-emitter voltage	open base	_	30	V
V _{EBO}	emitter-base voltage	open collector	_	5	V
I _C	collector current (DC)		_	1	Α
I _{CM}	peak collector current		_	3	А
I _{BM}	peak base current		_	300	mA
P _{tot}	total power dissipation	T _{amb} ≤ 25 °C; note 1	_	300	mW
		T _{amb} ≤ 25 °C; note 2	_	480	mW
T _{stg}	storage temperature		-65	+150	°C
Tj	junction temperature		_	150	°C
T _{amb}	operating ambient temperature		-65	+150	°C

Notes

- 1. Device mounted on a FR4 printed-circuit board, single-sided copper, tinplated, standard footprint.
- 2. Device mounted on a FR4 printed-circuit board, single-sided copper, tinplated, mounting pad for collector 1 cm².

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
R _{th j-a}	thermal resistance from junction to ambient	in free air; note 1	417	K/W
		in free air; note 2	260	K/W

Notes

- 1. Device mounted on a FR4 printed-circuit board, single-sided copper, tinplated, standard footprint.
- 2. Device mounted on a FR4 printed-circuit board, single-sided copper, tinplated, mounting pad for collector 1 cm².

30 V, 1 A NPN low V_{CEsat} (BISS) transistor

PBSS4130T

CHARACTERISTICS

 T_{amb} = 25 $^{\circ}C$ unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I _{CBO}	collector-base cut-off current	V _{CB} = 30 V; I _E = 0	_	_	100	nA
		V _{CB} = 30 V; I _E = 0; T _j = 150 °C	_	_	50	μΑ
I _{EBO}	emitter-base cut-off current	V _{EB} = 4 V; I _C = 0	_	_	100	nA
h _{FE}	DC current gain	V _{CE} = 2 V; I _C = 100 mA	350	470	_	
		V _{CE} = 2 V; I _C = 500 mA	300	450	-	
		V _{CE} = 2 V; I _C = 1 A	300	420	-	
V _{CEsat}	collector-emitter saturation voltage	I _C = 100 mA; I _B = 1 mA	_	_	90	mV
		I _C = 500 mA; I _B = 50 mA	_	_	120	mV
		I _C = 750 mA; I _B = 15 mA	_	_	220	mV
		I _C = 1 A; I _B = 50 mA; note 1	_	_	270	mV
R _{CEsat}	equivalent on-resistance	$I_C = 500 \text{ mA}$; $I_B = 50 \text{ mA}$; note 1	_	_	240	mΩ
V _{BEsat}	base-emitter saturation voltage	I _C = 1 A; I _B = 100 mA; note 1	_	_	1.1	V
V _{BEon}	base-emitter turn-on voltage V _{CE} = 2 V; I _C = 100 mA		_	_	0.75	V
f⊤	transition frequency	I _C = 100 mA; V _{CE} = 10 V; f = 100 MHz	100	_	_	MHz
C _c	collector capacitance	$V_{CB} = 10 \text{ V}; I_E = I_e = 0; f = 1 \text{ MHz}$	_	_	20	pF

Note

1. Pulse test: $t_p \le 300 \ \mu s; \ \delta \le 0.02.$

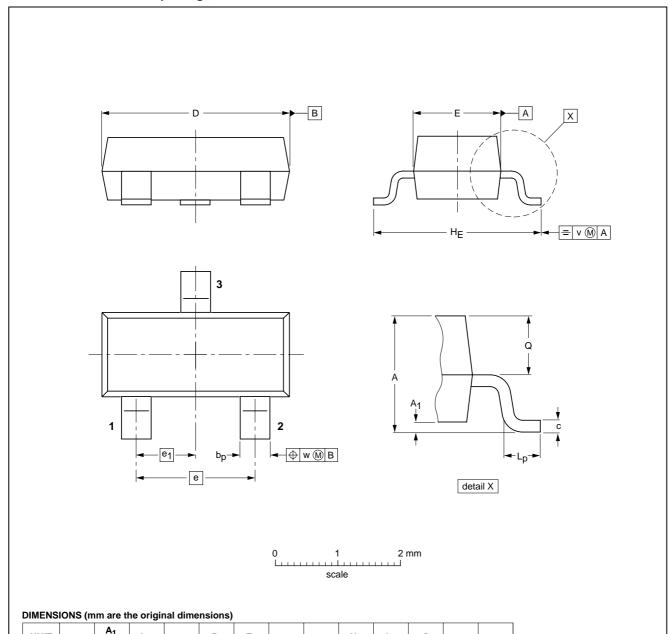
30 V, 1 A NPN low V_{CEsat} (BISS) transistor

PBSS4130T

PACKAGE OUTLINE

Plastic surface mounted package; 3 leads

SOT23



UNIT	A	max.	bp	С	D	E	е	e ₁	HE	L _p	Q	v	w
mm	1.1 0.9	0.1	0.48 0.38	0.15 0.09	3.0 2.8	1.4 1.2	1.9	0.95	2.5 2.1	0.45 0.15	0.55 0.45	0.2	0.1

OUTLINE		REFER	EUROPEAN	ICCUE DATE		
VERSION	IEC	JEDEC	EIAJ		PROJECTION	ISSUE DATE
SOT23		TO-236AB				-97-02-28 99-09-13

30 V, 1 A NPN low V_{CEsat} (BISS) transistor

PBSS4130T

DATA SHEET STATUS

LEVEL	DATA SHEET STATUS ⁽¹⁾	PRODUCT STATUS(2)(3)	DEFINITION
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

Notes

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- 3. For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

DEFINITIONS

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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