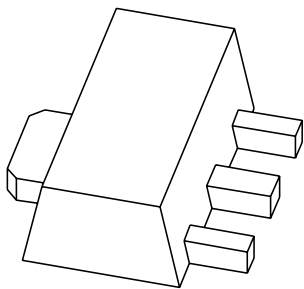


DATA SHEET



PBSS5520X

20 V, 5 A

PNP low V_{CEsat} (BISS) transistor

Product data sheet
Supersedes data of 2004 Jun 23

2004 Nov 08

20 V, 5 A PNP low V_{CEsat} (BISS) transistor

PBSS5520X

FEATURES

- High h_{FE} and low V_{CEsat} at high current operation
- High collector current I_C : 5 A
- High efficiency leading to less heat generation.

APPLICATIONS

- Medium power peripheral drivers (e.g. fans and motors)
- Strobe flash units for digital still cameras and mobile phones
- Power switch for LAN and ADSL systems
- Medium power DC-to-DC conversion
- Battery chargers
- Supply line switching.

DESCRIPTION

PNP low V_{CEsat} (BISS) transistor in a SOT89 (SC-62) plastic package.
NPN complement: PBSS4520X.

MARKING

TYPE NUMBER	MARKING CODE ⁽¹⁾
PBSS5520X	*1K

Note

- * = p: made in Hong Kong.
* = t: made in Malaysia.
* = W: made in China.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{CEO}	collector-emitter voltage	-20	V
I_C	collector current (DC)	-5	A
I_{CM}	peak collector current	-10	A
R_{CEsat}	equivalent on-resistance	54	mΩ

PINNING

PIN	DESCRIPTION
1	emitter
2	collector
3	base

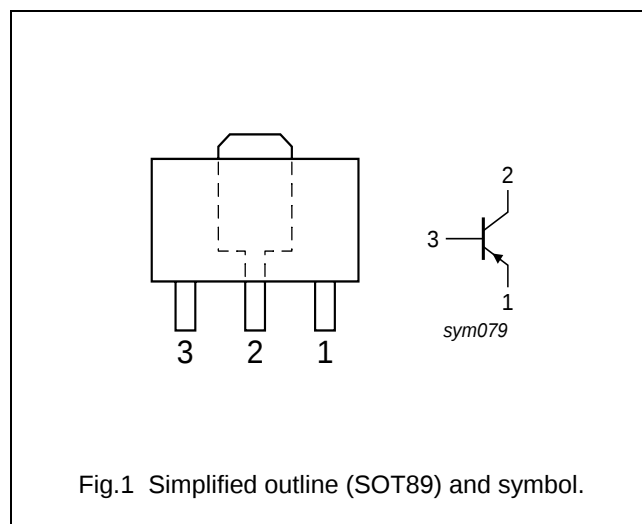


Fig.1 Simplified outline (SOT89) and symbol.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PBSS5520X	SC-62	plastic surface mounted package; collector pad for good heat transfer; 3 leads	SOT89

20 V, 5 A
PNP low V_{CEsat} (BISS) transistor

PBSS5520X

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

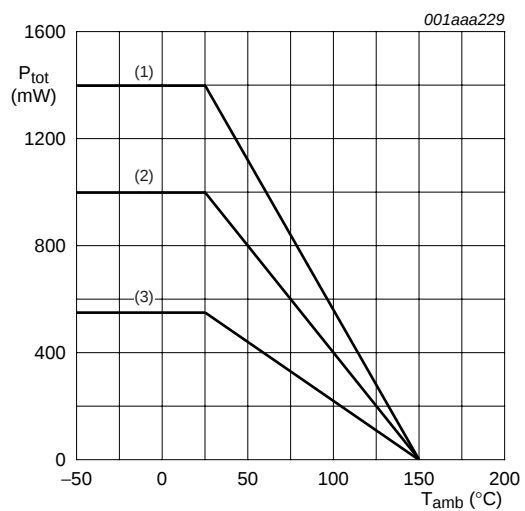
SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CBO}	collector-base voltage	open emitter	–	–20	V
V_{CEO}	collector-emitter voltage	open base	–	–20	V
V_{EBO}	emitter-base voltage	open collector	–	–5	V
I_C	collector current (DC)		–	–5	A
I_{CM}	peak collector current	$t_p \leq 1$ ms	–	–10	A
I_{CRP}	repetitive peak collector current	notes 1 and 2	–	–6.5	A
I_B	base current (DC)		–	–1	A
I_{BM}	peak base current	$t_p \leq 1$ ms	–	–2	A
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C			
		notes 1 and 2	–	2.5	W
		note 2	–	0.55	W
		note 3	–	1	W
		note 4	–	1.4	W
		note 5	–	1.6	W
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature		–	150	°C
T_{amb}	ambient temperature		–65	+150	°C

Notes

1. Operated under pulsed conditions; pulse width $t_p \leq 10$ ms; duty cycle $\delta \leq 0.2$.
2. Device mounted on a printed-circuit board, single-sided copper, tin-plated, standard footprint.
3. Device mounted on a printed-circuit board, single-sided copper, tin-plated, mounting pad for collector 1 cm².
4. Device mounted on a printed-circuit board, single-sided copper, tin-plated, mounting pad for collector 6 cm².
5. Device mounted on a 7 cm² ceramic printed-circuit board, 1 cm² single-sided copper, tin-plated.

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- (1) FR4 PCB; 6 cm² mounting pad for collector.
(2) FR4 PCB; 1 cm² mounting pad for collector.
(3) FR4 PCB; standard footprint.

Fig.2 Power derating curves.

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PNP low V_{CEsat} (BISS) transistor

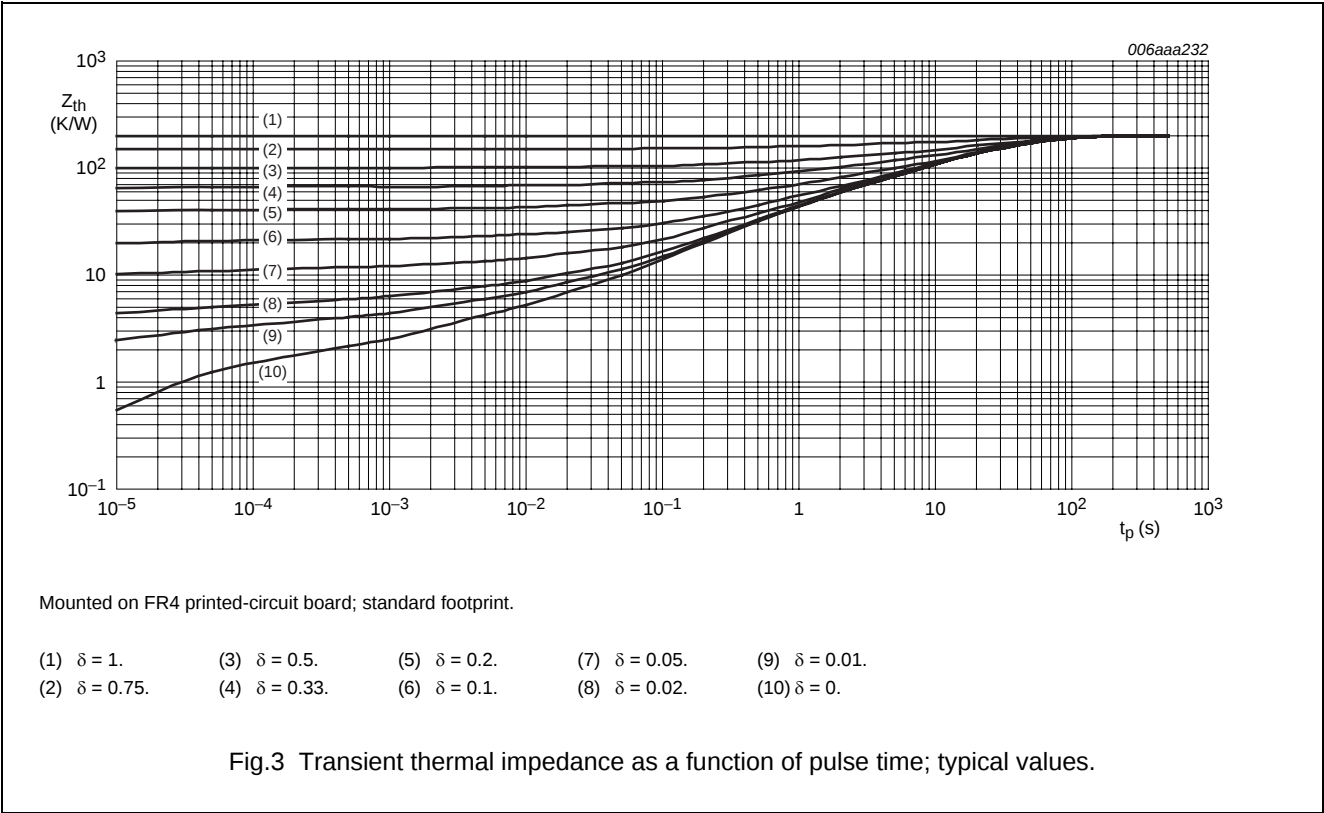
PBSS5520X

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air		
		notes 1 and 2	50	K/W
		note 2	225	K/W
		note 3	125	K/W
		note 4	90	K/W
		note 5	80	K/W
$R_{th(j-s)}$	thermal resistance from junction to soldering point		16	K/W

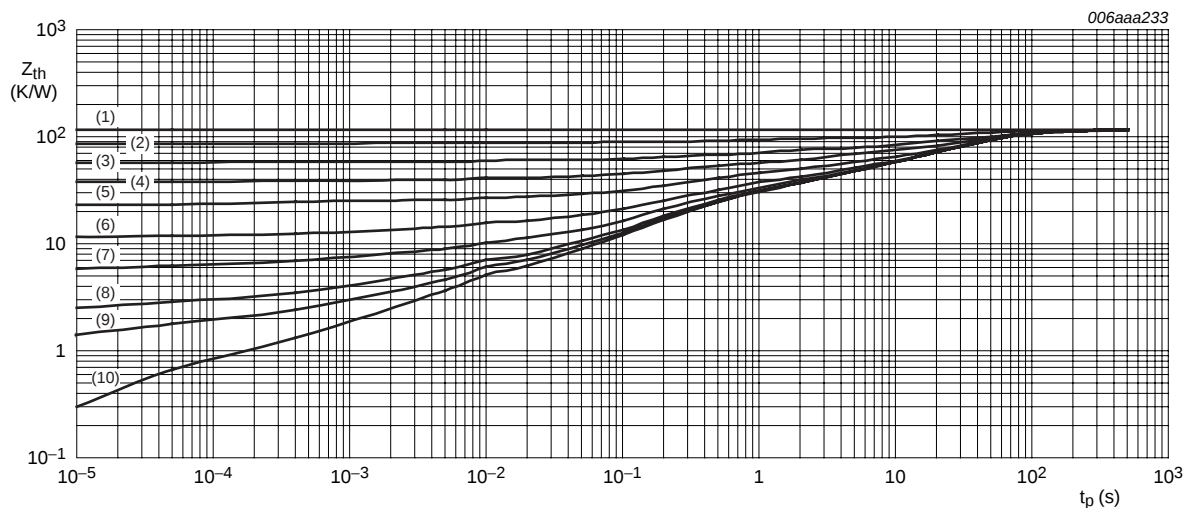
Notes

1. Operated under pulsed conditions; pulse width $t_p \leq 10$ ms; duty cycle $\delta \leq 0.2$.
2. Device mounted on a printed-circuit board, single-sided copper, tin-plated, standard footprint.
3. Device mounted on a printed-circuit board, single-sided copper, tin-plated, mounting pad for collector 1 cm².
4. Device mounted on a printed-circuit board, single-sided copper, tin-plated, mounting pad for collector 6 cm².
5. Device mounted on a 7 cm² ceramic printed-circuit board, 1 cm² single-sided copper, tin-plated.



20 V, 5 A
PNP low V_{CEsat} (BISS) transistor

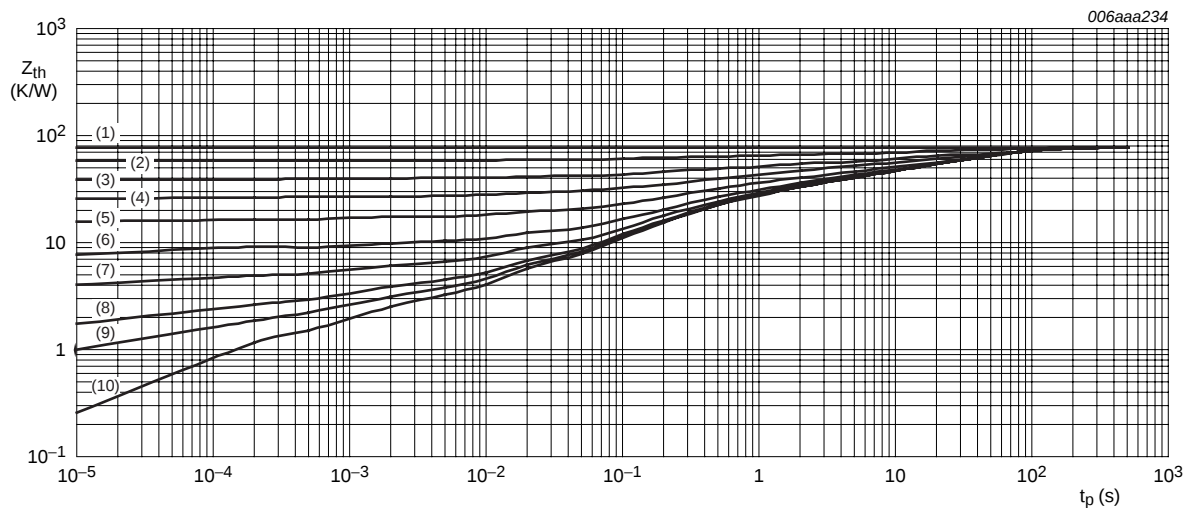
PBSS5520X



Mounted on FR4 printed-circuit board; mounting pad for collector 1 cm².

- | | | | | |
|----------------------|----------------------|---------------------|----------------------|----------------------|
| (1) $\delta = 1.$ | (3) $\delta = 0.5.$ | (5) $\delta = 0.2.$ | (7) $\delta = 0.05.$ | (9) $\delta = 0.01.$ |
| (2) $\delta = 0.75.$ | (4) $\delta = 0.33.$ | (6) $\delta = 0.1.$ | (8) $\delta = 0.02.$ | (10) $\delta = 0.$ |

Fig.4 Transient thermal impedance as a function of pulse time; typical values.



Mounted on FR4 printed-circuit board; mounting pad for collector 6 cm².

- | | | | | |
|----------------------|----------------------|---------------------|----------------------|----------------------|
| (1) $\delta = 1.$ | (3) $\delta = 0.5.$ | (5) $\delta = 0.2.$ | (7) $\delta = 0.05.$ | (9) $\delta = 0.01.$ |
| (2) $\delta = 0.75.$ | (4) $\delta = 0.33.$ | (6) $\delta = 0.1.$ | (8) $\delta = 0.02.$ | (10) $\delta = 0.$ |

Fig.5 Transient thermal impedance as a function of pulse time; typical values.

20 V, 5 A
PNP low V_{CEsat} (BISS) transistor

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CHARACTERISTICS $T_{amb} = 25\text{ }^{\circ}\text{C}$ unless otherwise specified.

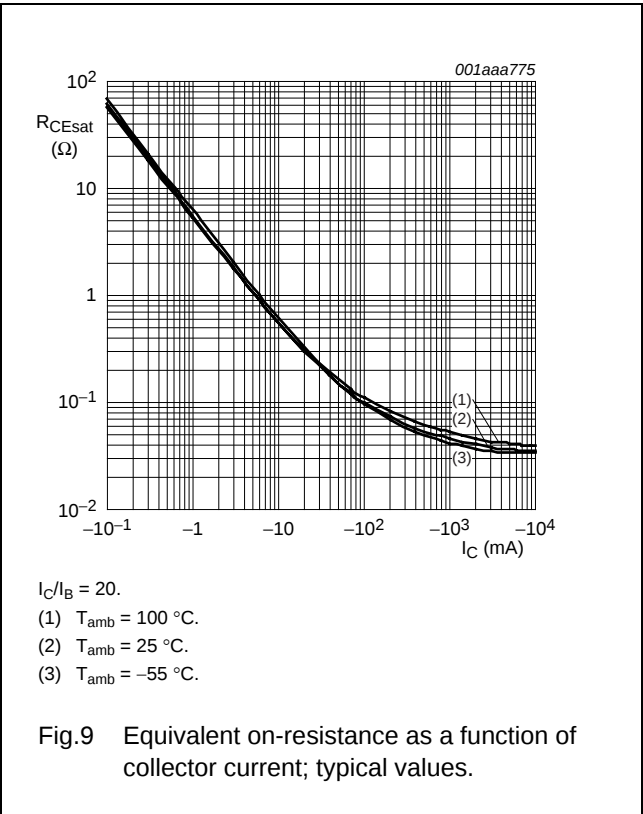
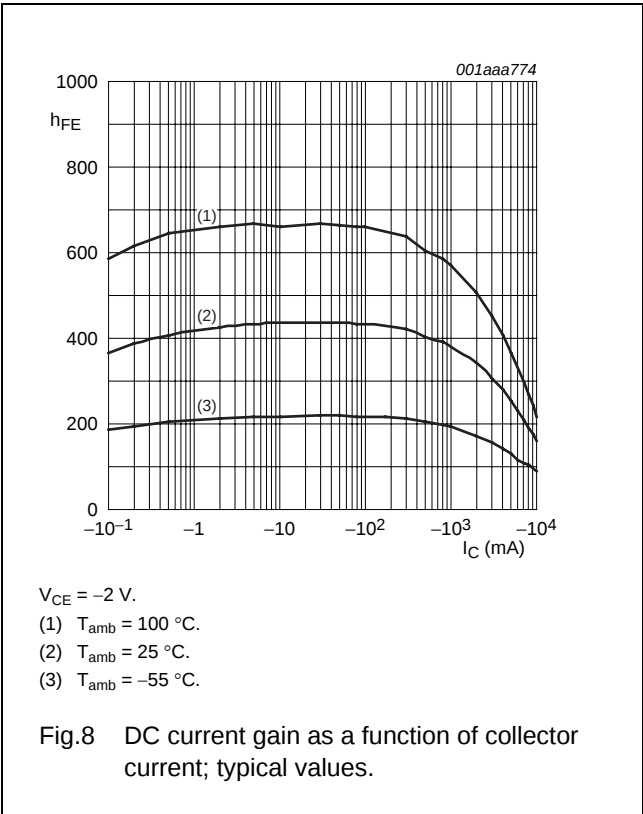
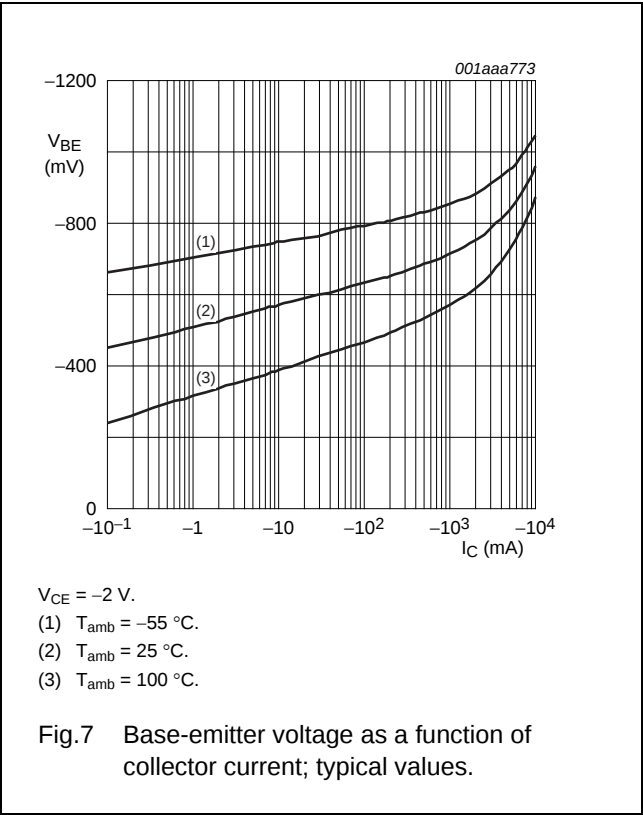
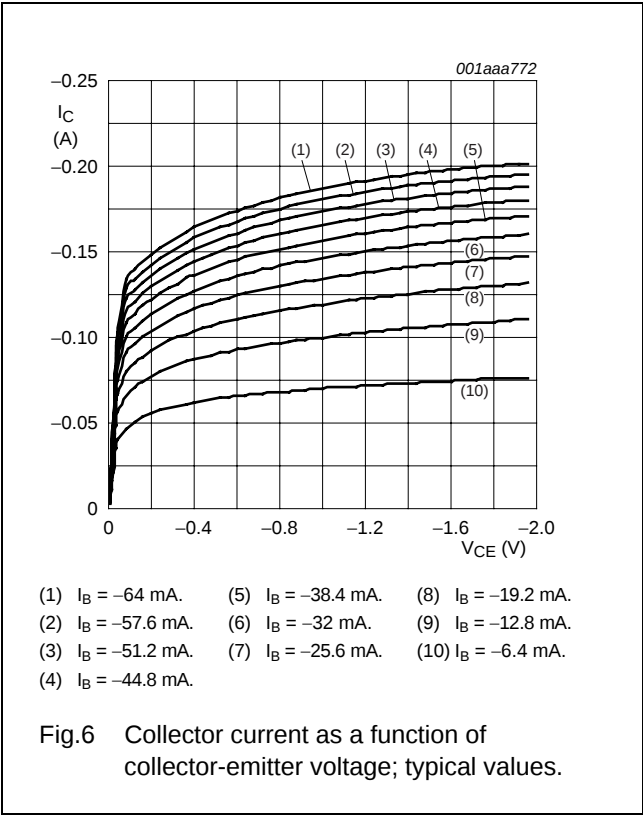
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{CBO}	collector-base cut-off current	$V_{CB} = -20\text{ V}; I_E = 0\text{ A}$	–	–	–100	nA
		$V_{CB} = -20\text{ V}; I_E = 0\text{ A}; T_J = 150\text{ }^{\circ}\text{C}$	–	–	–50	μA
I_{EBO}	emitter-base cut-off current	$V_{EB} = -5\text{ V}; I_C = 0\text{ A}$	–	–	–100	nA
I_{CES}	collector-emitter cut-off current	$V_{CE} = -20\text{ V}; V_{BE} = 0\text{ V}$	–	–	–100	nA
h_{FE}	DC current gain	$V_{CE} = -2\text{ V}$				
		$I_C = -0.5\text{ A}; \text{note 1}$	300	430	–	
		$I_C = -1\text{ A}; \text{note 1}$	275	400	–	
		$I_C = -2\text{ A}; \text{note 1}$	250	360	–	
		$I_C = -5\text{ A}; \text{note 1}$	150	260	–	
V_{CEsat}	collector-emitter saturation voltage	$I_C = -0.5\text{ A}; I_B = -5\text{ mA}$	–	–45	–70	mV
		$I_C = -1\text{ A}; I_B = -10\text{ mA}$	–	–70	–110	mV
		$I_C = -2.5\text{ A}; I_B = -125\text{ mA}; \text{note 1}$	–	–100	–150	mV
		$I_C = -4\text{ A}; I_B = -200\text{ mA}; \text{note 1}$	–	–150	–230	mV
		$I_C = -5\text{ A}; I_B = -500\text{ mA}; \text{note 1}$	–	–170	–270	mV
R_{CEsat}	equivalent on-resistance	$I_C = -5\text{ A}; I_B = -500\text{ mA}; \text{note 1}$	–	34	54	$\text{m}\Omega$
V_{BEsat}	base-emitter saturation voltage	$I_C = -4\text{ A}; I_B = -200\text{ mA}; \text{note 1}$	–	–0.9	–1.05	V
		$I_C = -5\text{ A}; I_B = -500\text{ mA}; \text{note 1}$	–	–0.96	–1.1	V
V_{BEon}	base-emitter turn-on voltage	$V_{CE} = -2\text{ V}; I_C = -2\text{ A}$	–	–0.74	–0.85	V
f_T	transition frequency	$I_C = -100\text{ mA}; V_{CE} = -10\text{ V};$ $f = 100\text{ MHz}$	80	100	–	MHz
C_c	collector capacitance	$V_{CB} = -10\text{ V}; I_E = I_C = 0\text{ A};$ $f = 1\text{ MHz}$	–	130	150	pF

Note

1. Pulse test: $t_p \leq 300\text{ }\mu\text{s}$; $\delta \leq 0.02$.

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20 V, 5 A

PNP low V_{CEsat} (BISS) transistor

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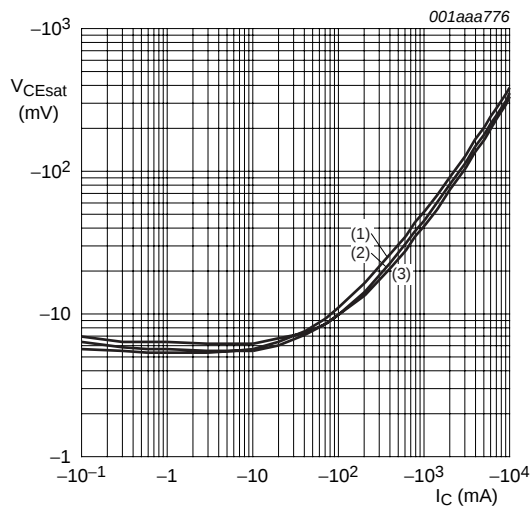
 $I_C/I_B = 20$.(1) $T_{amb} = 100\text{ }^{\circ}\text{C}$.(2) $T_{amb} = 25\text{ }^{\circ}\text{C}$.(3) $T_{amb} = -55\text{ }^{\circ}\text{C}$.

Fig.10 Collector-emitter saturation voltage as a function of collector current; typical values.

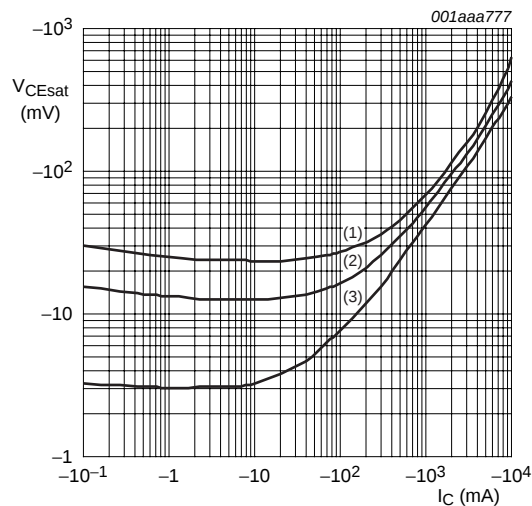
 $T_{amb} = 25\text{ }^{\circ}\text{C}$.(1) $I_C/I_B = 100$.(2) $I_C/I_B = 50$.(3) $I_C/I_B = 10$.

Fig.11 Collector-emitter saturation voltage as a function of collector current; typical values.

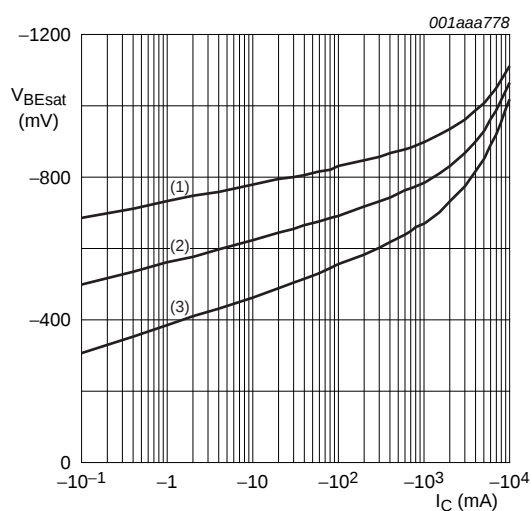
 $I_C/I_B = 20$.(1) $T_{amb} = -55\text{ }^{\circ}\text{C}$.(2) $T_{amb} = 25\text{ }^{\circ}\text{C}$.(3) $T_{amb} = 150\text{ }^{\circ}\text{C}$.

Fig.12 Base-emitter saturation voltage as a function of collector current; typical values.

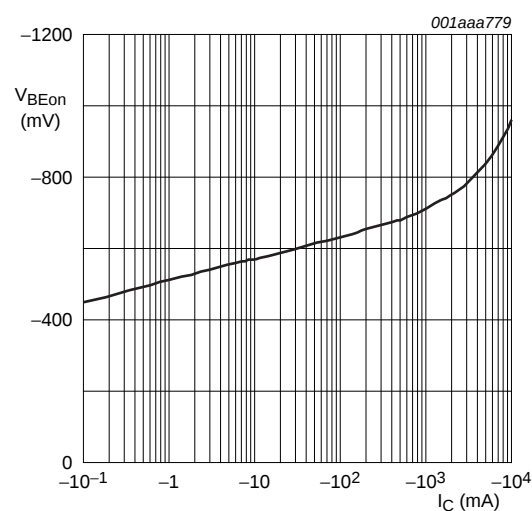
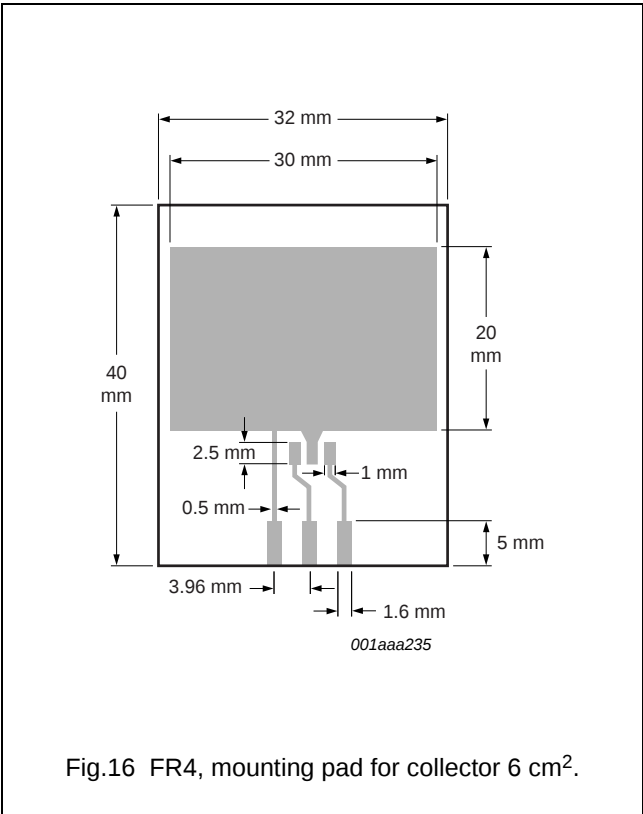
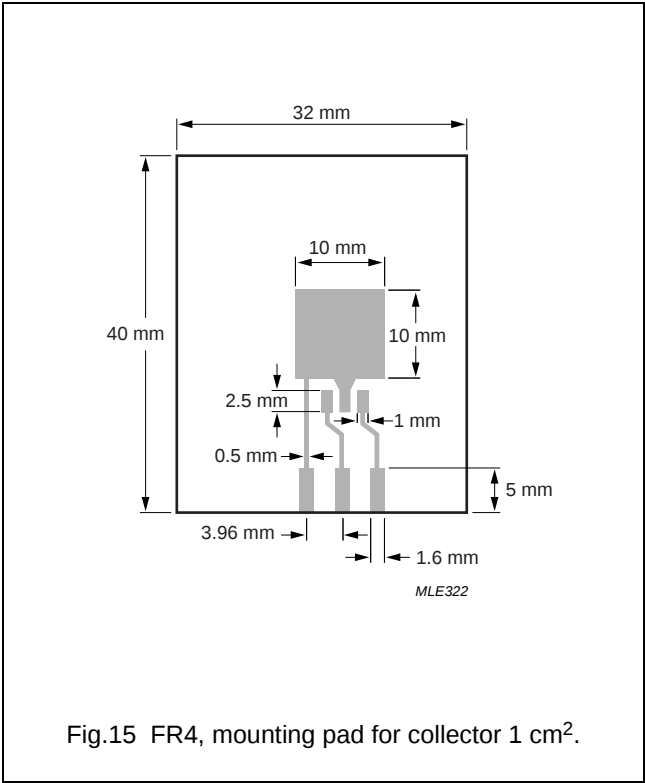
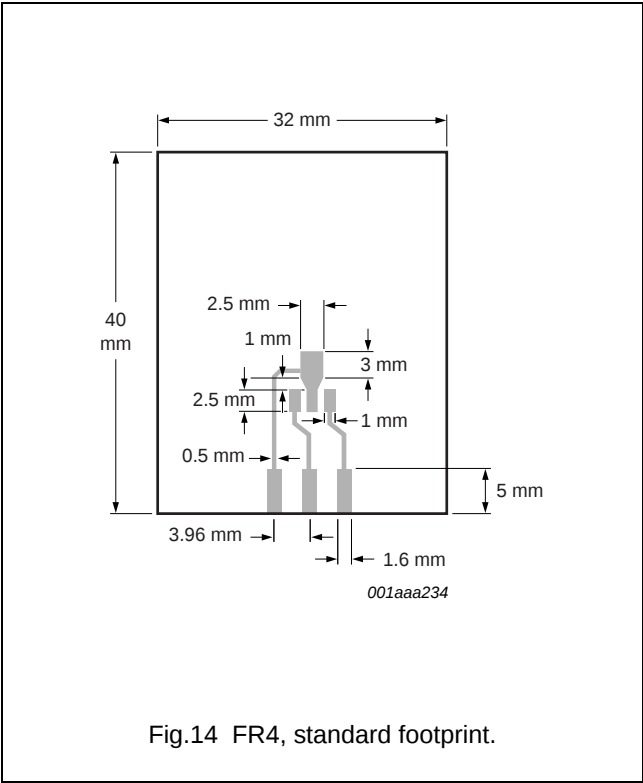
 $T_{amb} = 25\text{ }^{\circ}\text{C}$; $V_{CE} = -2\text{ V}$.

Fig.13 Base-emitter turn-on voltage as a function of collector current; typical values.

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Reference mounting conditions



20 V, 5 A

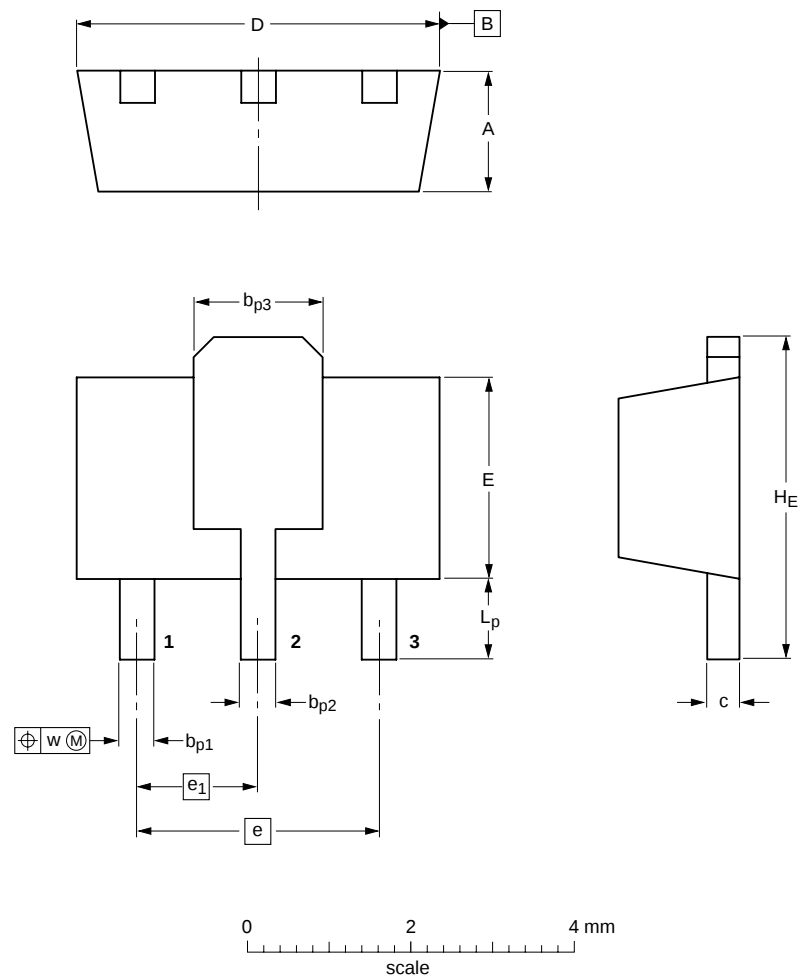
PNP low V_{CEsat} (BISS) transistor

PBSS5520X

PACKAGE OUTLINE

Plastic surface-mounted package; collector pad for good heat transfer; 3 leads

SOT89



DIMENSIONS (mm are the original dimensions)

UNIT	A	b_{p1}	b_{p2}	b_{p3}	c	D	E	e	e_1	H_E	L_p	w
mm	1.6 1.4	0.48 0.35	0.53 0.40	1.8 1.4	0.44 0.23	4.6 4.4	2.6 2.4	3.0	1.5	4.25 3.75	1.2 0.8	0.13

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT89		TO-243	SC-62			04-08-03 06-03-16

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PNP low V_{CEsat} (BISS) transistor

PBSS5520X

DATA SHEET STATUS

DOCUMENT STATUS ⁽¹⁾	PRODUCT STATUS ⁽²⁾	DEFINITION
Objective data sheet	Development	This document contains data from the objective specification for product development.
Preliminary data sheet	Qualification	This document contains data from the preliminary specification.
Product data sheet	Production	This document contains the product specification.

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Contact information

For additional information please visit: <http://www.nxp.com>

For sales offices addresses send e-mail to: salesaddresses@nxp.com

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