

PBSS4041SPN

60 V NPN/PNP low V_{CEsat} (BISS) transistor

Rev. 2 — 20 October 2010

Product data sheet

1. Product profile

1.1 General description

NPN/PNP low V_{CEsat} Breakthrough In Small Signal (BISS) transistor in a SOT96-1 (SO8) medium power Surface-Mounted Device (SMD) plastic package.

Table 1. Product overview

Type number	Package		NPN/PNP complement	PNP/PNP complement
	NXP	Name		
PBSS4041SPN	SOT96-1	SO8	PBSS4041SN	PBSS4041SP

1.2 Features and benefits

- Very low collector-emitter saturation voltage V_{CEsat}
- High collector current capability I_C and I_{CM}
- High collector current gain (h_{FE}) at high I_C
- High efficiency due to less heat generation
- Smaller required Printed-Circuit Board (PCB) area than for conventional transistors

1.3 Applications

- Loadswitch
- Battery-driven devices
- Power management
- Charging circuits
- Power switches (e.g. motors, fans)

1.4 Quick reference data

Table 2. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
TR1; NPN low V_{CEsat} transistor						
V_{CEO}	collector-emitter voltage	open base	-	-	60	V
I_C	collector current		-	-	6.7	A
I_{CM}	peak collector current	single pulse; $t_p \leq 1$ ms	-	-	15	A
R_{CEsat}	collector-emitter saturation resistance	$I_C = 4$ A; $I_B = 0.2$ A	[1] -	32	48	m Ω



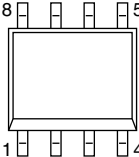
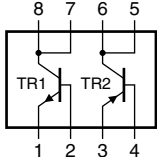
Table 2. Quick reference data ...continued

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
TR2; PNP low V_{CEsat} transistor						
V_{CEO}	collector-emitter voltage	open base	-	-	-60	V
I_C	collector current		-	-	-5.9	A
I_{CM}	peak collector current	single pulse; $t_p \leq 1$ ms	-	-	-15	A
R_{CEsat}	collector-emitter saturation resistance	$I_C = -4$ A; $I_B = -0.4$ A	[1]	-	47	m Ω

[1] Pulse test: $t_p \leq 300$ μ s; $\delta \leq 0.02$.

2. Pinning information

Table 3. Pinning

Pin	Description	Simplified outline	Graphic symbol
1	emitter TR1		 006aaa985
2	base TR1		
3	emitter TR2		
4	base TR2		
5	collector TR2		
6	collector TR2		
7	collector TR1		
8	collector TR1		

3. Ordering information

Table 4. Ordering information

Type number	Package		
	Name	Description	Version
PBSS4041SPN	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1

4. Marking

Table 5. Marking codes

Type number	Marking code
PBSS4041SPN	4041SPN

5. Limiting values

Table 6. Limiting values

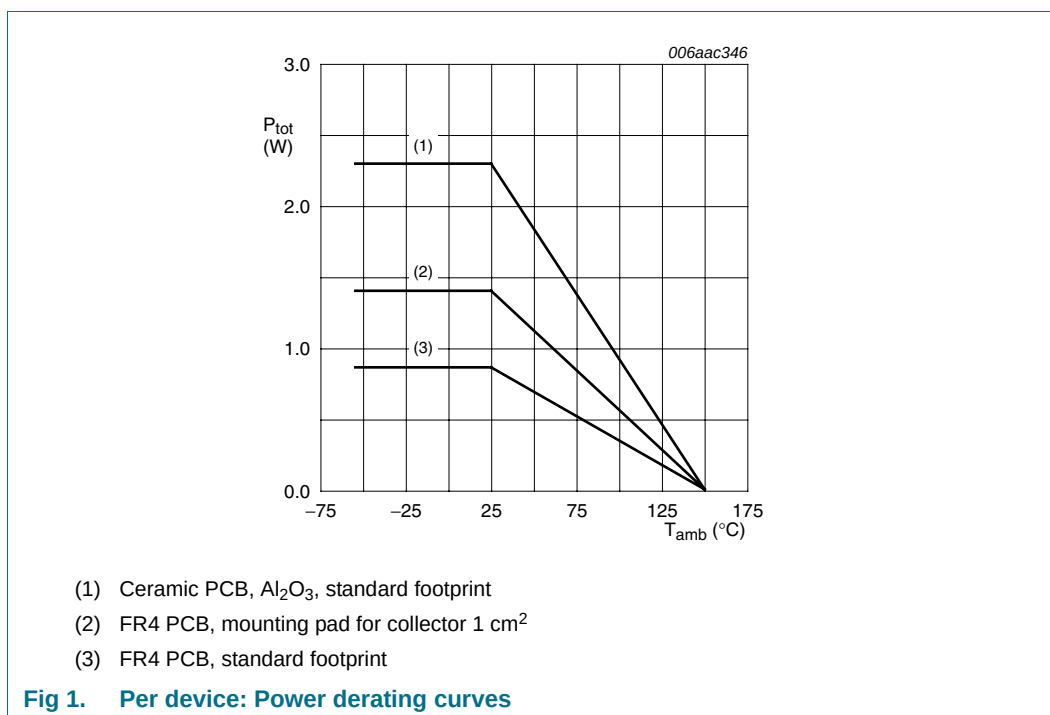
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit	
TR1 (NPN)						
I _C	collector current		-	6.7	A	
TR2 (PNP)						
I _C	collector current		-	−5.9	A	
Per transistor; for the PNP transistor with negative polarity						
V _{CBO}	collector-base voltage	open emitter	-	60	V	
V _{CEO}	collector-emitter voltage	open base	-	60	V	
V _{EBO}	emitter-base voltage	open collector	-	5	V	
I _{CM}	peak collector current	single pulse; t _p ≤ 1 ms	-	15	A	
I _B	base current		-	1	A	
P _{tot}	total power dissipation	T _{amb} ≤ 25 °C	[1]	-	0.73	W
			[2]	-	1	W
			[3]	-	1.7	W
Per device						
P _{tot}	total power dissipation	T _{amb} ≤ 25 °C	[1]	-	0.86	W
			[2]	-	1.4	W
			[3]	-	2.3	W
T _j	junction temperature		-	150	°C	
T _{amb}	ambient temperature		−55	+150	°C	
T _{stg}	storage temperature		−65	+150	°C	

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for collector 1 cm².

[3] Device mounted on a ceramic PCB, Al₂O₃, standard footprint.



6. Thermal characteristics

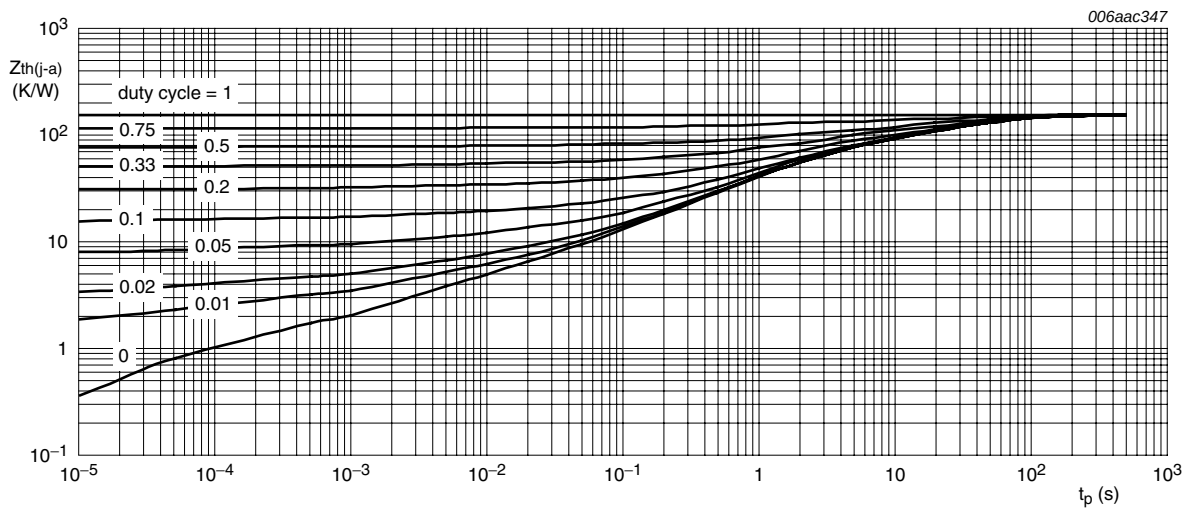
Table 7. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Per transistor						
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	170	K/W
			[2]	-	125	K/W
			[3]	-	75	K/W
$R_{th(j-sp)}$	thermal resistance from junction to solder point		-	-	40	K/W
Per device						
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	145	K/W
			[2]	-	90	K/W
			[3]	-	55	K/W

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

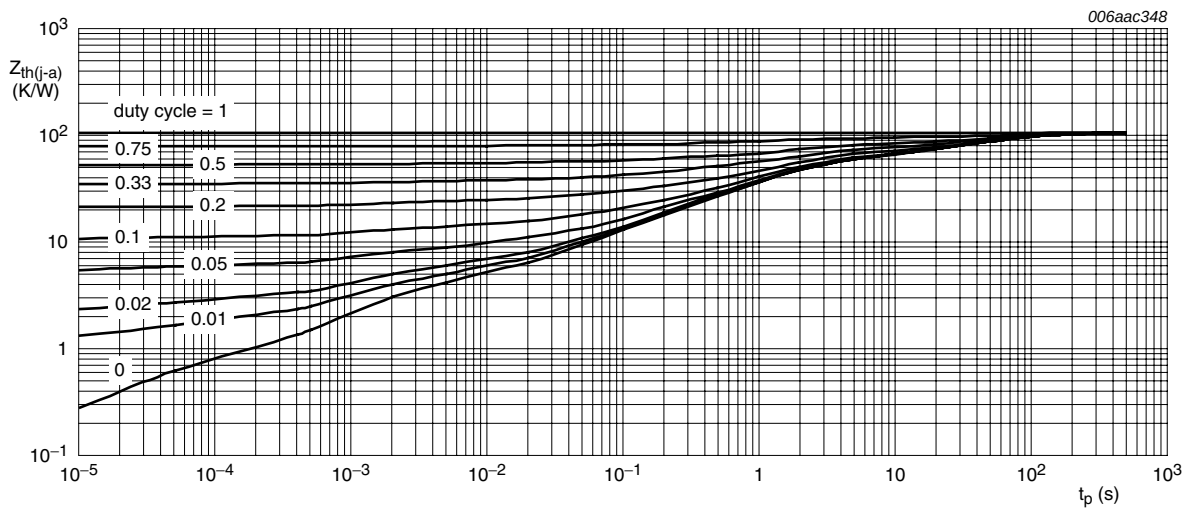
[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for collector 1 cm².

[3] Device mounted on a ceramic PCB, Al₂O₃, standard footprint.



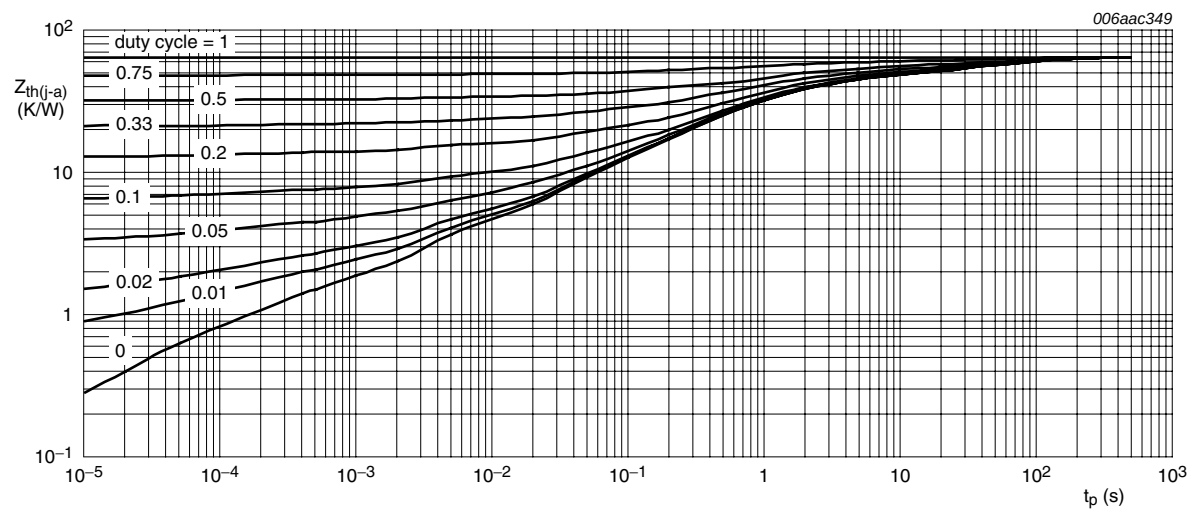
FR4 PCB, standard footprint

Fig 2. Per transistor: Transient thermal impedance from junction to ambient as a function of pulse duration; typical values



FR4 PCB, mounting pad for collector 1 cm^2

Fig 3. Per transistor: Transient thermal impedance from junction to ambient as a function of pulse duration; typical values



Ceramic PCB, Al_2O_3 , standard footprint

Fig 4. Per transistor: Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

7. Characteristics

Table 8. Characteristics

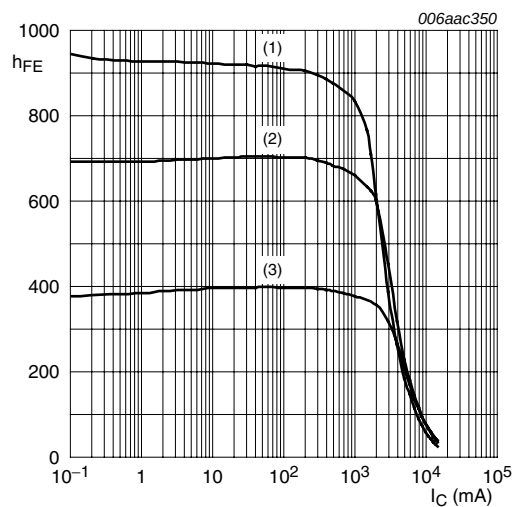
$T_{amb} = 25\text{ }^{\circ}\text{C}$ unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
TR1; NPN low V_{CEsat} transistor							
I_{CBO}	collector-base cut-off current	$V_{CB} = 60\text{ V}; I_E = 0\text{ A}$	-	-	100	nA	
		$V_{CB} = 60\text{ V}; I_E = 0\text{ A}; T_j = 150\text{ }^{\circ}\text{C}$	-	-	50	μA	
I_{CES}	collector-emitter cut-off current	$V_{CE} = 48\text{ V}; V_{BE} = 0\text{ V}$	-	-	100	nA	
I_{EBO}	emitter-base cut-off current	$V_{EB} = 5\text{ V}; I_C = 0\text{ A}$	-	-	100	nA	
h_{FE}	DC current gain	$V_{CE} = 2\text{ V}$	[1]				
		$I_C = 500\text{ mA}$	300	500	-		
		$I_C = 1\text{ A}$	300	500	-		
		$I_C = 2\text{ A}$	250	450	-		
		$I_C = 4\text{ A}$	150	250	-		
		$I_C = 6\text{ A}$	75	150	-		
V_{CEsat}	collector-emitter saturation voltage		[1]				
		$I_C = 1\text{ A}; I_B = 50\text{ mA}$	-	40	60	mV	
		$I_C = 1\text{ A}; I_B = 10\text{ mA}$	-	65	100	mV	
		$I_C = 2\text{ A}; I_B = 40\text{ mA}$	-	85	145	mV	
		$I_C = 4\text{ A}; I_B = 200\text{ mA}$	-	125	190	mV	
		$I_C = 4\text{ A}; I_B = 40\text{ mA}$	-	220	320	mV	
		$I_C = 7\text{ A}; I_B = 350\text{ mA}$	-	230	350	mV	
R_{CEsat}	collector-emitter saturation resistance	$I_C = 4\text{ A}; I_B = 200\text{ mA}$	[1]	-	32	48	$\text{m}\Omega$
V_{BEsat}	base-emitter saturation voltage		[1]				
		$I_C = 1\text{ A}; I_B = 100\text{ mA}$	-	0.86	1	V	
		$I_C = 4\text{ A}; I_B = 400\text{ mA}$	-	1.05	1.2	V	
V_{BEon}	base-emitter turn-on voltage	$V_{CE} = 2\text{ V}; I_C = 2\text{ A}$	[1]	-	0.75	0.85	V
t_d	delay time	$V_{CC} = 12.5\text{ V}; I_C = 1\text{ A};$	-	35	-	ns	
t_r	rise time	$I_{Bon} = 0.05\text{ A}; I_{Boff} = -0.05\text{ A}$	-	65	-	ns	
t_{on}	turn-on time		-	100	-	ns	
t_s	storage time		-	1050	-	ns	
t_f	fall time		-	220	-	ns	
t_{off}	turn-off time		-	1270	-	ns	
f_T	transition frequency	$V_{CE} = 10\text{ V}; I_C = 100\text{ mA};$ $f = 100\text{ MHz}$	-	130	-	MHz	
C_c	collector capacitance	$V_{CB} = 10\text{ V}; I_E = i_e = 0\text{ A};$ $f = 1\text{ MHz}$	-	35	-	pF	

Table 8. Characteristics ...continued
 $T_{amb} = 25\text{ }^{\circ}\text{C}$ unless otherwise specified.

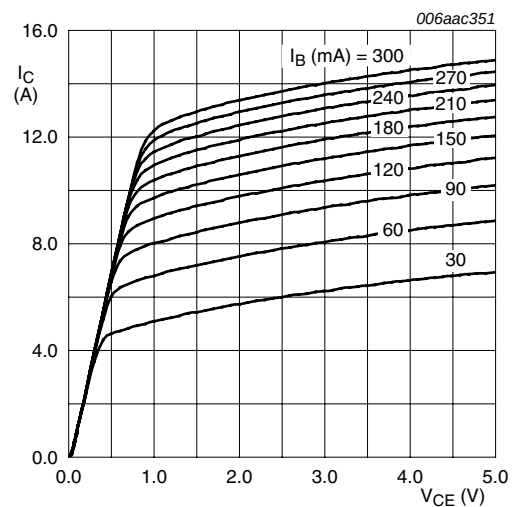
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
TR2; PNP low V_{CEsat} transistor						
I_{CBO}	collector-base cut-off current	$V_{CB} = -60\text{ V}; I_E = 0\text{ A}$	-	-	-100	nA
		$V_{CB} = -60\text{ V}; I_E = 0\text{ A}; T_j = 150\text{ }^{\circ}\text{C}$	-	-	-50	μA
I_{CES}	collector-emitter cut-off current	$V_{CE} = -48\text{ V}; V_{BE} = 0\text{ V}$	-	-	-100	nA
I_{EBO}	emitter-base cut-off current	$V_{EB} = -5\text{ V}; I_C = 0\text{ A}$	-	-	-100	nA
h_{FE}	DC current gain	$V_{CE} = -2\text{ V}$	[1]			
		$I_C = -500\text{ mA}$	200	300	-	
		$I_C = -1\text{ A}$	180	270	-	
		$I_C = -2\text{ A}$	150	250	-	
		$I_C = -4\text{ A}$	120	180	-	
		$I_C = -6\text{ A}$	80	125	-	
V_{CEsat}	collector-emitter saturation voltage	[1]				
		$I_C = -1\text{ A}; I_B = -50\text{ mA}$	-	-65	-90	mV
		$I_C = -1\text{ A}; I_B = -10\text{ mA}$	-	-130	-190	mV
		$I_C = -2\text{ A}; I_B = -40\text{ mA}$	-	-155	-230	mV
		$I_C = -4\text{ A}; I_B = -200\text{ mA}$	-	-220	-330	mV
		$I_C = -4\text{ A}; I_B = -400\text{ mA}$	-	-190	-275	mV
R_{CEsat}	collector-emitter saturation resistance	$I_C = -4\text{ A}; I_B = -400\text{ mA}$	[1] -	47	70	$\text{m}\Omega$
V_{BEsat}	base-emitter saturation voltage	[1]				
		$I_C = -1\text{ A}; I_B = -100\text{ mA}$	-	-0.84	-1	V
		$I_C = -4\text{ A}; I_B = -400\text{ mA}$	-	-1	-1.2	V
V_{BEon}	base-emitter turn-on voltage	$V_{CE} = -2\text{ V}; I_C = -2\text{ A}$	[1] -	-0.78	-0.85	V
t_d	delay time	$V_{CC} = -12.5\text{ V}; I_C = -1\text{ A};$	-	45	-	ns
t_r	rise time	$I_{Bon} = -0.05\text{ A}; I_{Boff} = 0.05\text{ A}$	-	60	-	ns
t_{on}	turn-on time		-	105	-	ns
t_s	storage time		-	440	-	ns
t_f	fall time		-	75	-	ns
t_{off}	turn-off time		-	515	-	ns
f_T	transition frequency	$V_{CB} = -10\text{ V}; I_C = -100\text{ mA}; f = 100\text{ MHz}$	-	110	-	MHz
C_c	collector capacitance	$V_{CB} = -10\text{ V}; I_E = i_e = 0\text{ A}; f = 1\text{ MHz}$	-	85	-	pF

[1] Pulse test: $t_p \leq 300\text{ }\mu\text{s}$; $\delta \leq 0.02$.



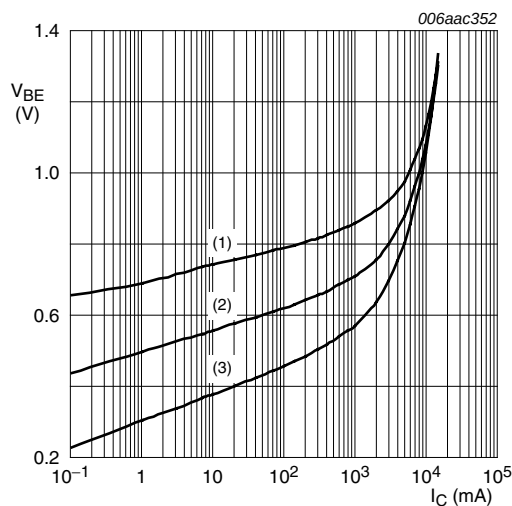
- $V_{CE} = 2\text{ V}$
- (1) $T_{amb} = 100\text{ }^{\circ}\text{C}$
 - (2) $T_{amb} = 25\text{ }^{\circ}\text{C}$
 - (3) $T_{amb} = -55\text{ }^{\circ}\text{C}$

Fig 5. TR1 (NPN): DC current gain as a function of collector current; typical values



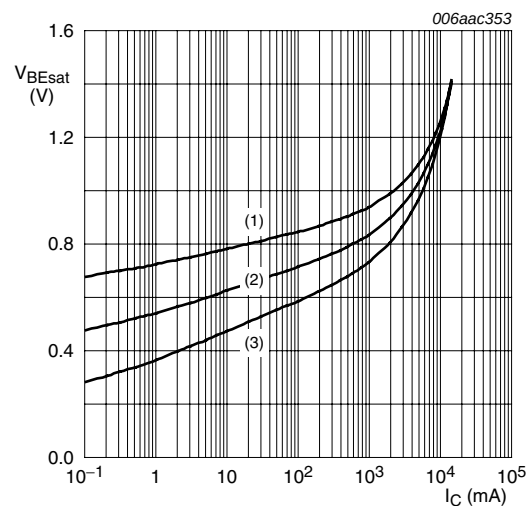
$T_{amb} = 25\text{ }^{\circ}\text{C}$

Fig 6. TR1 (NPN): Collector current as a function of collector-emitter voltage; typical values



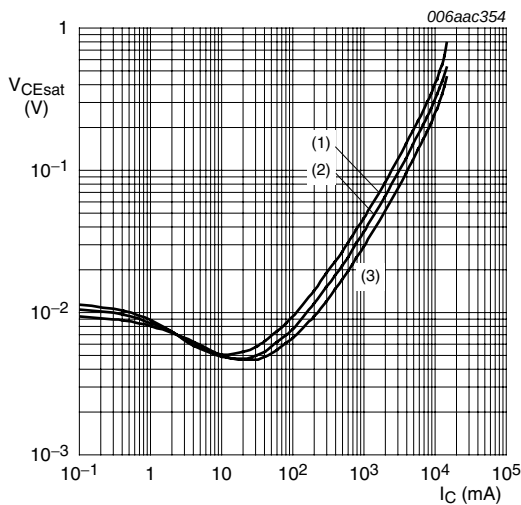
- $V_{CE} = 2\text{ V}$
- (1) $T_{amb} = -55\text{ }^{\circ}\text{C}$
 - (2) $T_{amb} = 25\text{ }^{\circ}\text{C}$
 - (3) $T_{amb} = 100\text{ }^{\circ}\text{C}$

Fig 7. TR1 (NPN): Base-emitter voltage as a function of collector current; typical values



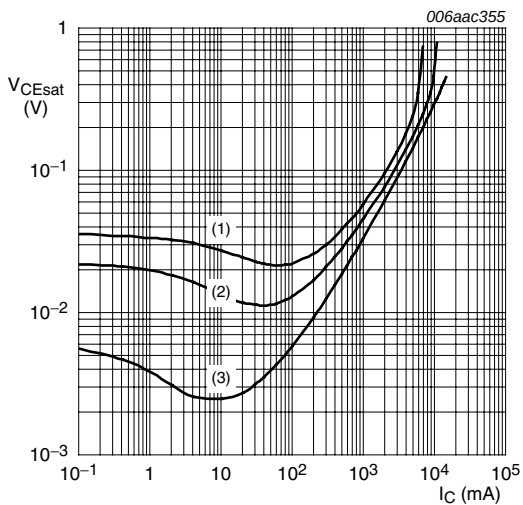
- $I_C/I_B = 20$
- (1) $T_{amb} = -55\text{ }^{\circ}\text{C}$
 - (2) $T_{amb} = 25\text{ }^{\circ}\text{C}$
 - (3) $T_{amb} = 100\text{ }^{\circ}\text{C}$

Fig 8. TR1 (NPN): Base-emitter saturation voltage as a function of collector current; typical values



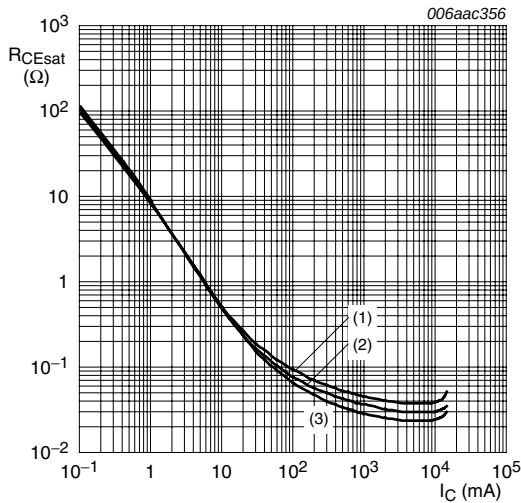
- $I_C/I_B = 20$
- (1) $T_{amb} = 100\text{ }^{\circ}\text{C}$
 - (2) $T_{amb} = 25\text{ }^{\circ}\text{C}$
 - (3) $T_{amb} = -55\text{ }^{\circ}\text{C}$

Fig 9. TR1 (NPN): Collector-emitter saturation voltage as a function of collector current; typical values



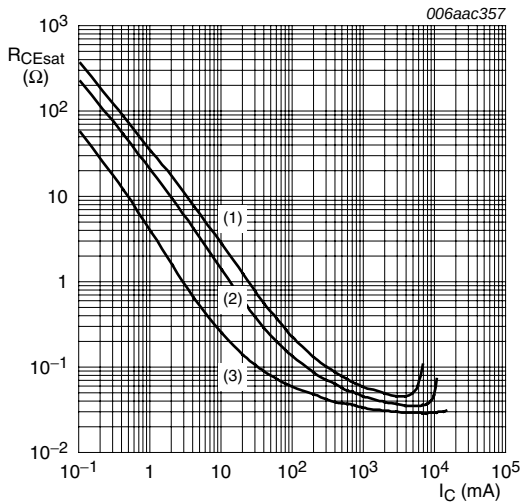
- $T_{amb} = 25\text{ }^{\circ}\text{C}$
- (1) $I_C/I_B = 100$
 - (2) $I_C/I_B = 50$
 - (3) $I_C/I_B = 10$

Fig 10. TR1 (NPN): Collector-emitter saturation voltage as a function of collector current; typical values



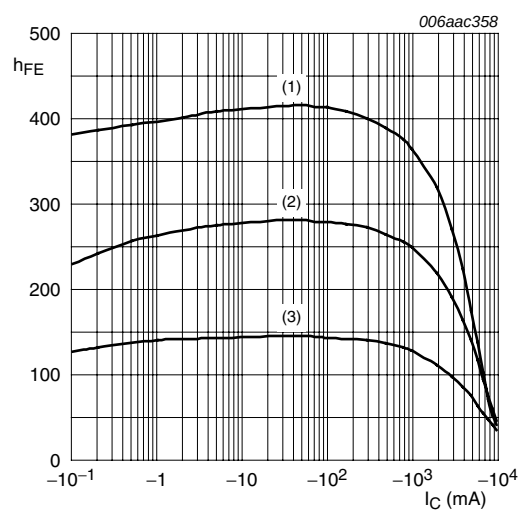
- $I_C/I_B = 20$
- (1) $T_{amb} = 100\text{ }^{\circ}\text{C}$
 - (2) $T_{amb} = 25\text{ }^{\circ}\text{C}$
 - (3) $T_{amb} = -55\text{ }^{\circ}\text{C}$

Fig 11. TR1 (NPN): Collector-emitter saturation resistance as a function of collector current; typical values



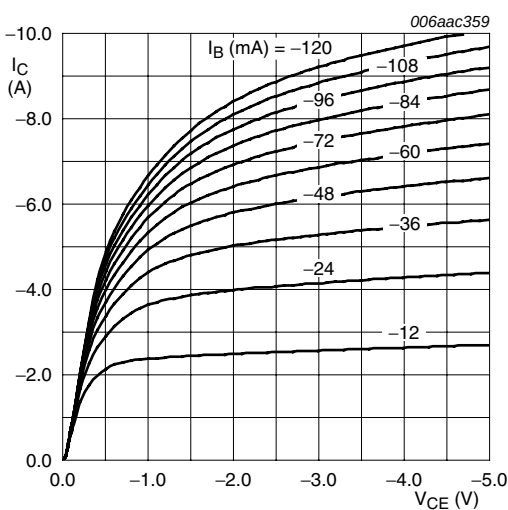
- $T_{amb} = 25\text{ }^{\circ}\text{C}$
- (1) $I_C/I_B = 100$
 - (2) $I_C/I_B = 50$
 - (3) $I_C/I_B = 10$

Fig 12. TR1 (NPN): Collector-emitter saturation resistance as a function of collector current; typical values



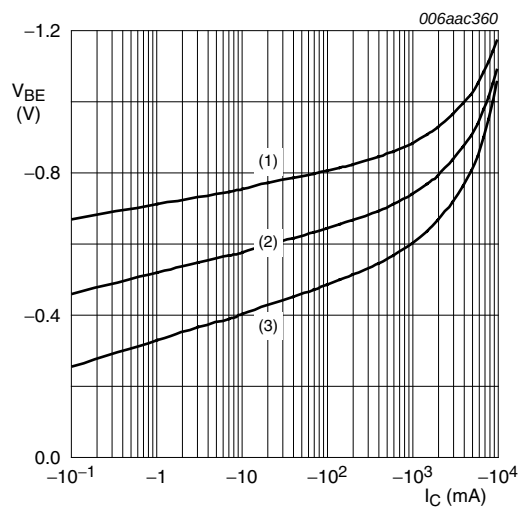
- $V_{CE} = -2\text{ V}$
- (1) $T_{amb} = 100\text{ }^{\circ}\text{C}$
 - (2) $T_{amb} = 25\text{ }^{\circ}\text{C}$
 - (3) $T_{amb} = -55\text{ }^{\circ}\text{C}$

Fig 13. TR2 (PNP): DC current gain as a function of collector current; typical values



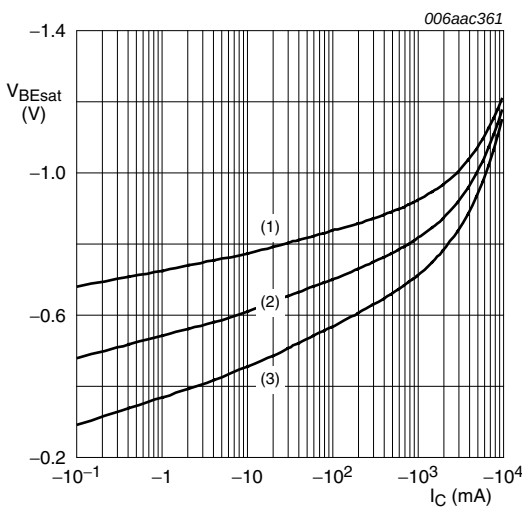
$T_{amb} = 25\text{ }^{\circ}\text{C}$

Fig 14. TR2 (PNP): Collector current as a function of collector-emitter voltage; typical values



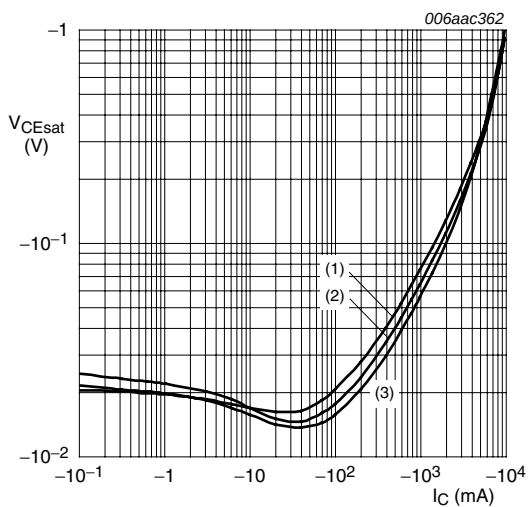
- $V_{CE} = -2\text{ V}$
- (1) $T_{amb} = -55\text{ }^{\circ}\text{C}$
 - (2) $T_{amb} = 25\text{ }^{\circ}\text{C}$
 - (3) $T_{amb} = 100\text{ }^{\circ}\text{C}$

Fig 15. TR2 (PNP): Base-emitter voltage as a function of collector current; typical values



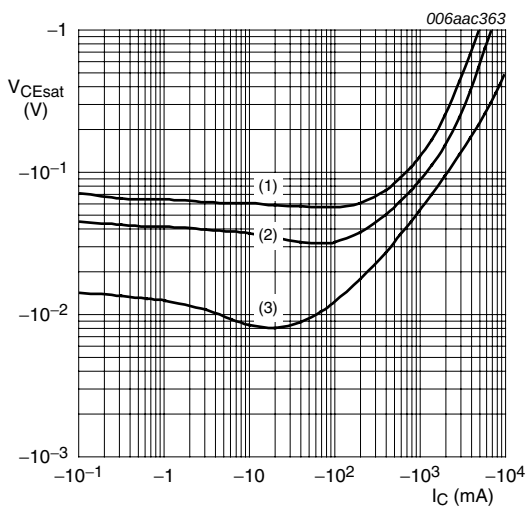
- $I_C/I_B = 20$
- (1) $T_{amb} = -55\text{ }^{\circ}\text{C}$
 - (2) $T_{amb} = 25\text{ }^{\circ}\text{C}$
 - (3) $T_{amb} = 100\text{ }^{\circ}\text{C}$

Fig 16. TR2 (PNP): Base-emitter saturation voltage as a function of collector current; typical values



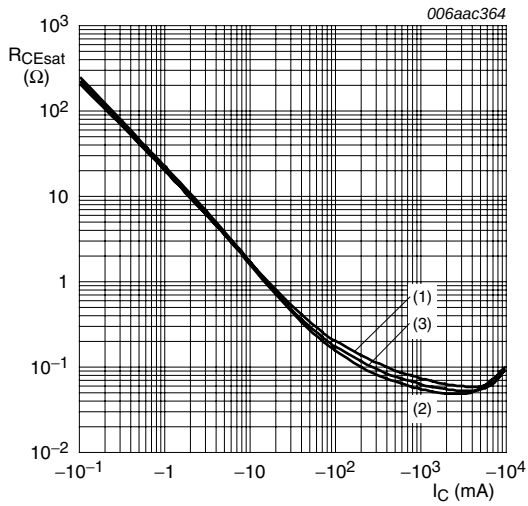
- $I_C/I_B = 20$
- (1) $T_{amb} = 100\text{ }^{\circ}\text{C}$
 - (2) $T_{amb} = 25\text{ }^{\circ}\text{C}$
 - (3) $T_{amb} = -55\text{ }^{\circ}\text{C}$

Fig 17. TR2 (PNP): Collector-emitter saturation voltage as a function of collector current; typical values



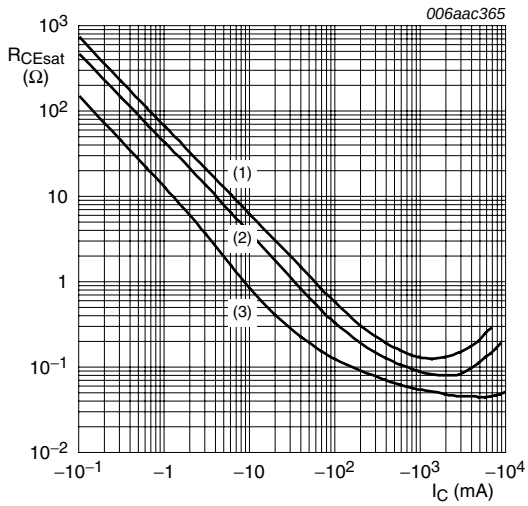
- $T_{amb} = 25\text{ }^{\circ}\text{C}$
- (1) $I_C/I_B = 100$
 - (2) $I_C/I_B = 50$
 - (3) $I_C/I_B = 10$

Fig 18. TR2 (PNP): Collector-emitter saturation voltage as a function of collector current; typical values



- $I_C/I_B = 20$
- (1) $T_{amb} = 100\text{ }^{\circ}\text{C}$
 - (2) $T_{amb} = 25\text{ }^{\circ}\text{C}$
 - (3) $T_{amb} = -55\text{ }^{\circ}\text{C}$

Fig 19. TR2 (PNP): Collector-emitter saturation resistance as a function of collector current; typical values



- $T_{amb} = 25\text{ }^{\circ}\text{C}$
- (1) $I_C/I_B = 100$
 - (2) $I_C/I_B = 50$
 - (3) $I_C/I_B = 10$

Fig 20. TR2 (PNP): Collector-emitter saturation resistance as a function of collector current; typical values

8. Test information

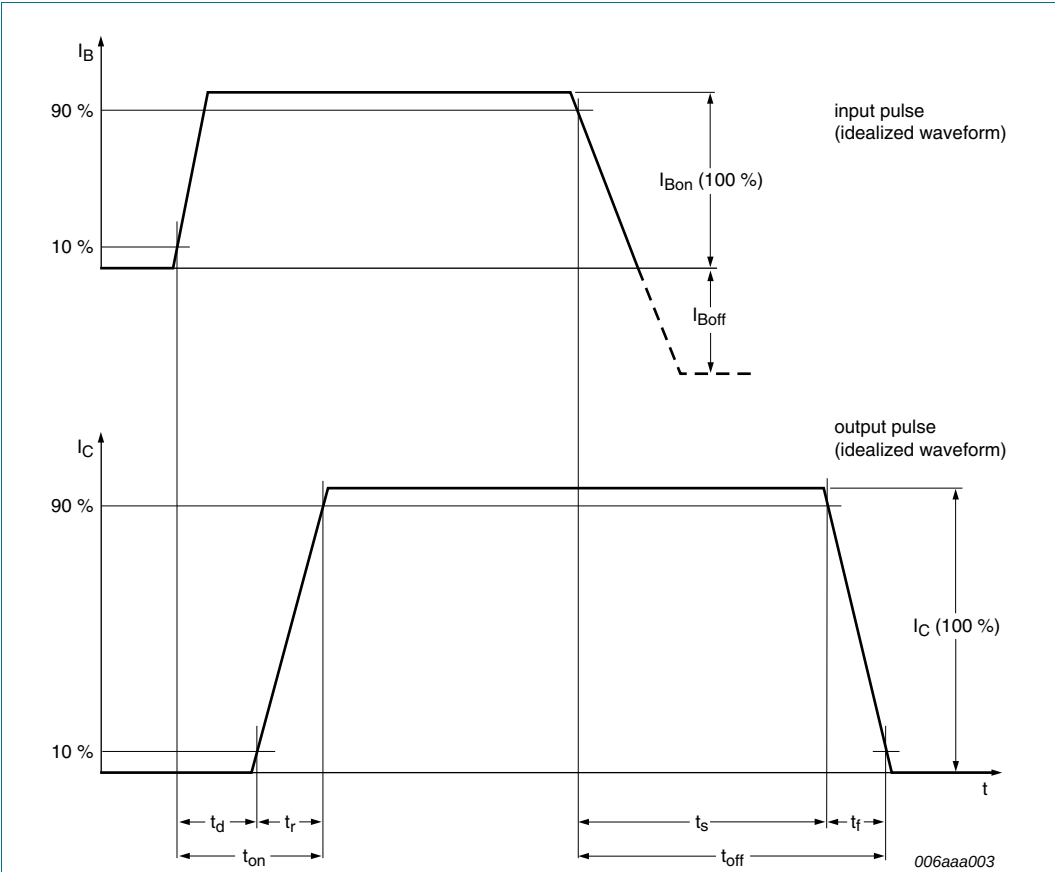
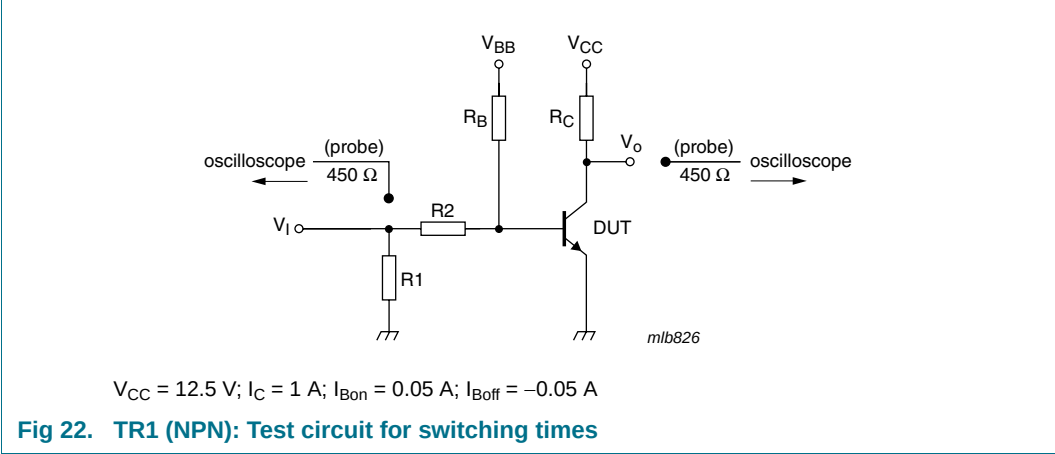


Fig 21. TR1 (NPN): BISS transistor switching time definition



$V_{CC} = 12.5\text{ V}$; $I_C = 1\text{ A}$; $I_{Bon} = 0.05\text{ A}$; $I_{Boff} = -0.05\text{ A}$

Fig 22. TR1 (NPN): Test circuit for switching times

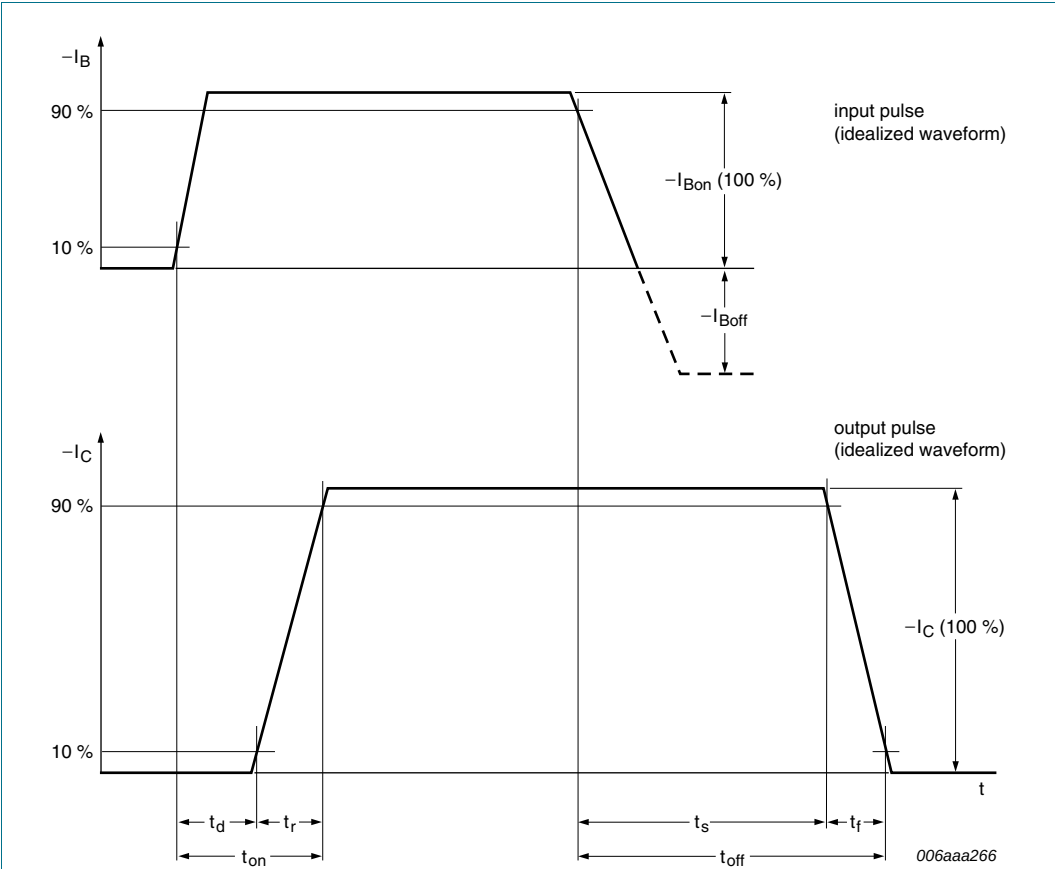
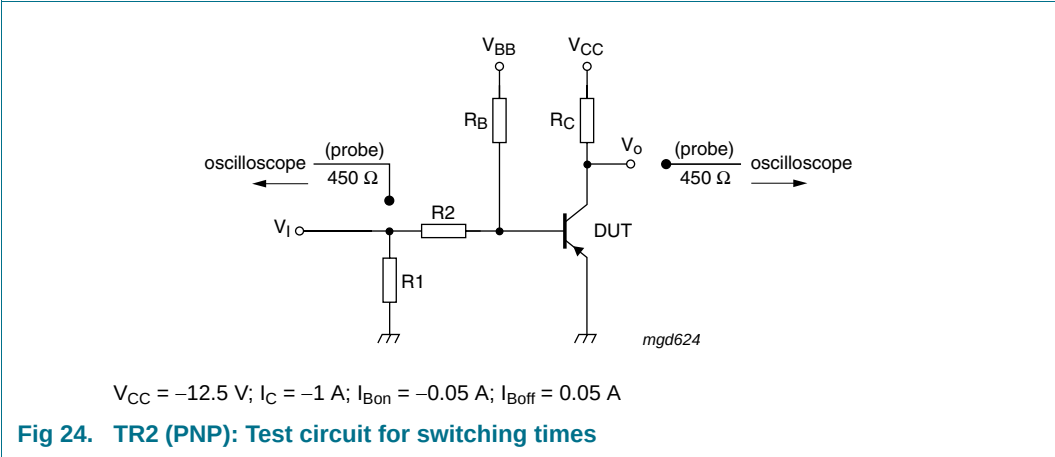


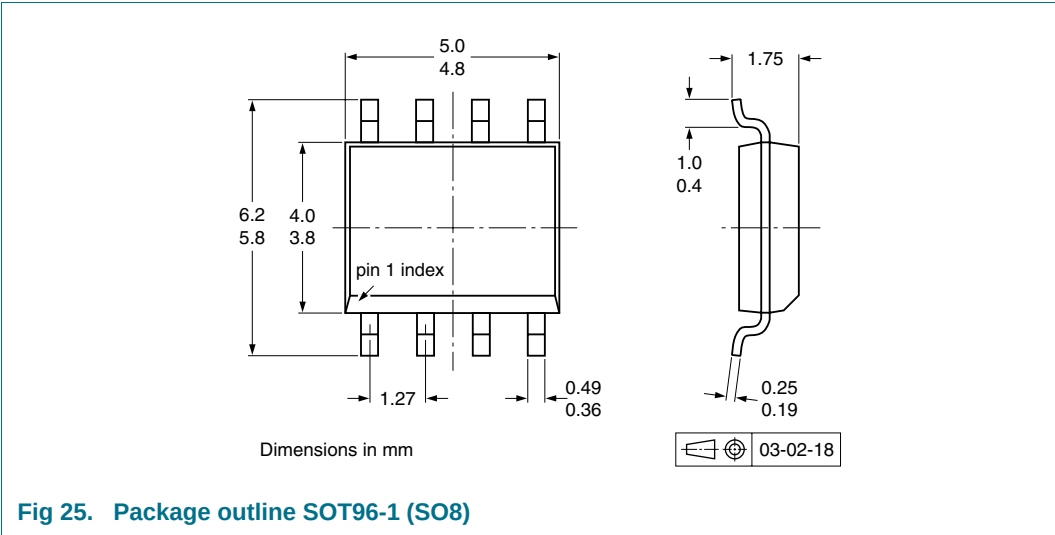
Fig 23. TR2 (PNP): BISS transistor switching time definition



$V_{CC} = -12.5\text{ V}$; $I_C = -1\text{ A}$; $I_{Bon} = -0.05\text{ A}$; $I_{Boff} = 0.05\text{ A}$

Fig 24. TR2 (PNP): Test circuit for switching times

9. Package outline



10. Packing information

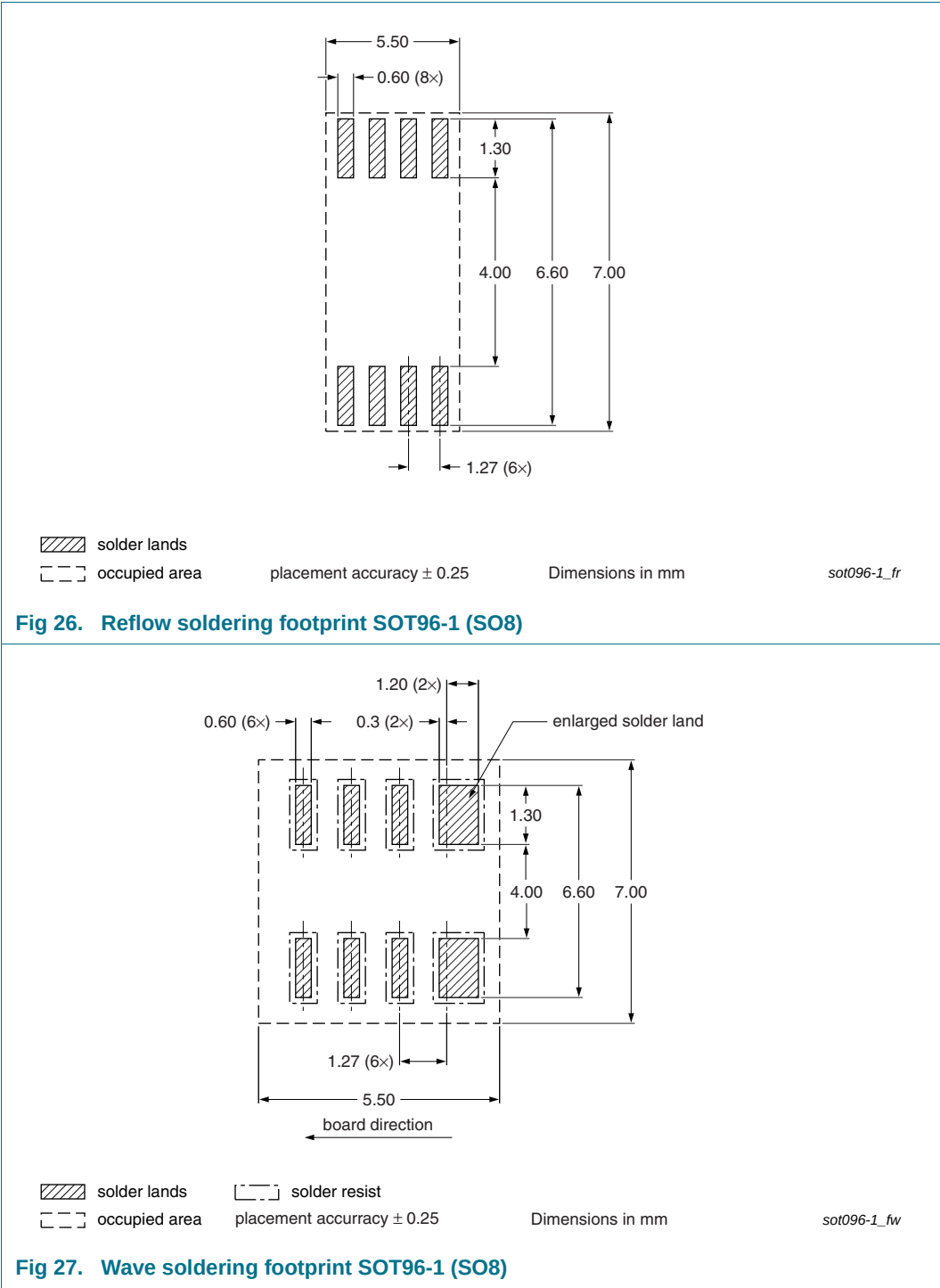
Table 9. Packing methods

The indicated -xxx are the last three digits of the 12NC ordering code.^[1]

Type number	Package	Description	Packing quantity	
			1000	2500
PBSS4041SPN	SOT96-1	8 mm pitch, 12 mm tape and reel	-115	-118

[1] For further information and the availability of packing methods, see [Section 14](#).

11. Soldering



12. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PBSS4041SPN v.2	20101020	Product data sheet	-	PBSS4041SPN v.1
Modifications:	• Figure 1 "Per device: Power derating curves" : updated.			
PBSS4041SPN v.1	20100714	Product data sheet	-	-

13. Legal information

13.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

13.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

13.3 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or

malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nxp.com/profile/terms>, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from national authorities.

Quick reference data — The Quick reference data is an extract of the product data given in the Limiting values and Characteristics sections of this document, and as such is not complete, exhaustive or legally binding.

13.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

14. Contact information

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: salesaddresses@nxp.com

15. Contents

1	Product profile	1
1.1	General description	1
1.2	Features and benefits	1
1.3	Applications	1
1.4	Quick reference data	1
2	Pinning information	2
3	Ordering information	2
4	Marking	2
5	Limiting values	3
6	Thermal characteristics	4
7	Characteristics	7
8	Test information	13
9	Package outline	15
10	Packing information	15
11	Soldering	16
12	Revision history	17
13	Legal information	18
13.1	Data sheet status	18
13.2	Definitions	18
13.3	Disclaimers	18
13.4	Trademarks	19
14	Contact information	19
15	Contents	20

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

© NXP B.V. 2010.

All rights reserved.

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 20 October 2010

Document identifier: PBSS4041SPN