

PMD9050D

MOSFET driver

Rev. 01 — 27 November 2006

Product data sheet

1. Product profile

1.1 General description

NPN transistor and high-speed switching diode supplemented by an NPN/PNP transistor pair connected as a silicon-controlled switch in a SOT457 (SC-74) small Surface-Mounted Device (SMD) plastic package.

1.2 Features

- General-purpose transistor and high-speed switching diode as driver
- Silicon-controlled switch to bypass the driver transistor
- Application-optimized pinout
- Internal connections to minimize layout effort
- Space-saving solution
- Reduces component count

1.3 Applications

- MOSFET driver with silicon-controlled switch

1.4 Quick reference data

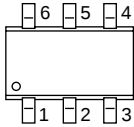
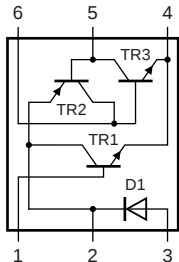
Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Per transistor; for the PNP transistor with negative polarity						
V_{CEO}	collector-emitter voltage	open base	-	-	45	V
I_C	collector current		-	-	0.1	A
I_{CM}	peak collector current	single pulse; $t_p \leq 1$ ms	-	-	0.2	A
Diode (D1)						
I_F	forward current		-	-	0.2	A
V_F	forward voltage	$I_F = 200$ mA	[1] -	-	1.1	V
V_R	reverse voltage		-	-	60	V

[1] Pulse test: $t_p \leq 300$ μ s; $\delta \leq 0.02$.

2. Pinning information

Table 2. Pinning

Pin	Symbol	Description	Simplified outline	Symbol
1	IN	input		
2	OUT	output		
3	RC	collector resistor		
4	GND	ground		
5	ON	output enable		
6	OFF	output disable		

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3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PMD9050D	SC-74	plastic surface-mounted package (TSOP6); 6 leads	SOT457

4. Marking

Table 4. Marking codes

Type number	Marking code
PMD9050D	9G

5. Limiting values

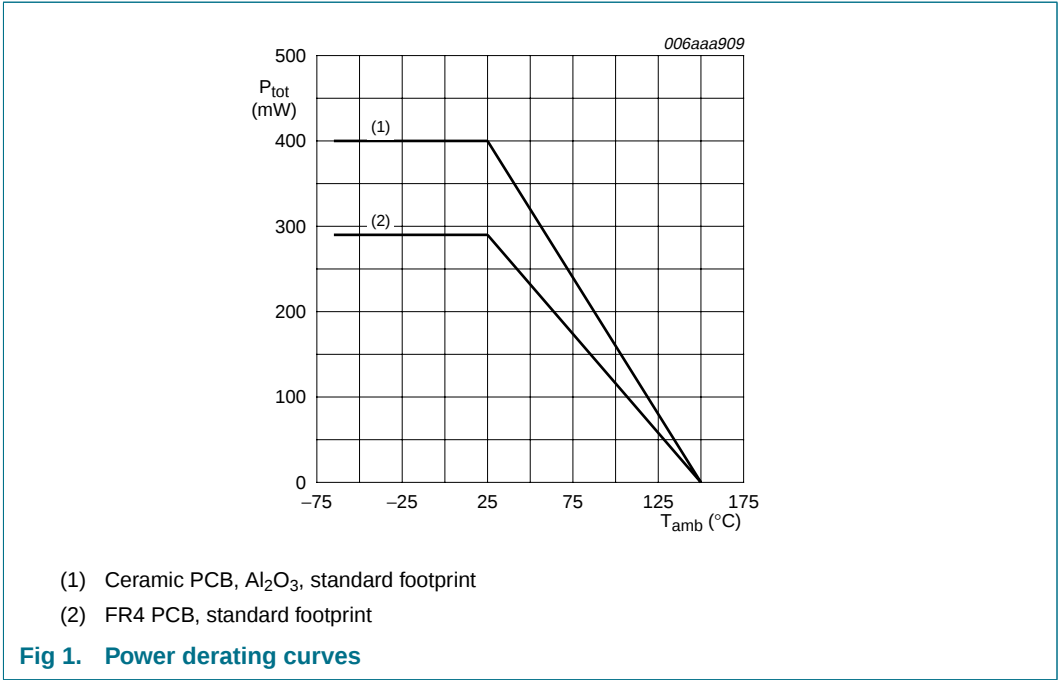
Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
Per transistor; for the PNP transistor with negative polarity					
V _{CBO}	collector-base voltage	open emitter	-	50	V
V _{CEO}	collector-emitter voltage	open base	-	45	V
V _{EBO}	emitter-base voltage	open collector	-	5	V
I _C	collector current		-	0.1	A
I _{CM}	peak collector current	single pulse; t _p ≤ 1 ms	-	0.2	A
I _B	base current		-	0.1	A
I _{BM}	peak base current	single pulse; t _p ≤ 1 ms	-	0.2	A
Diode (D1)					
V _{RRM}	repetitive peak reverse voltage		-	60	V
V _R	reverse voltage		-	60	V
I _F	forward current		-	0.2	A
I _{FRM}	repetitive peak forward current	t _p ≤ 1 ms; δ = 0.25	-	0.6	A
I _{FSM}	non-repetitive peak forward current	square wave			
		t _p ≤ 1 μs	-	9	A
		t _p ≤ 100 μs	-	3	A
		t _p ≤ 10 ms	-	1.7	A
Device					
P _{tot}	total power dissipation	T _{amb} ≤ 25 °C	[1]	-	290 mW
			[2]	-	400 mW
T _j	junction temperature		-	150	°C
T _{amb}	ambient temperature		-65	+150	°C
T _{stg}	storage temperature		-65	+150	°C

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

[2] Device mounted on a ceramic PCB, Al₂O₃, standard footprint.

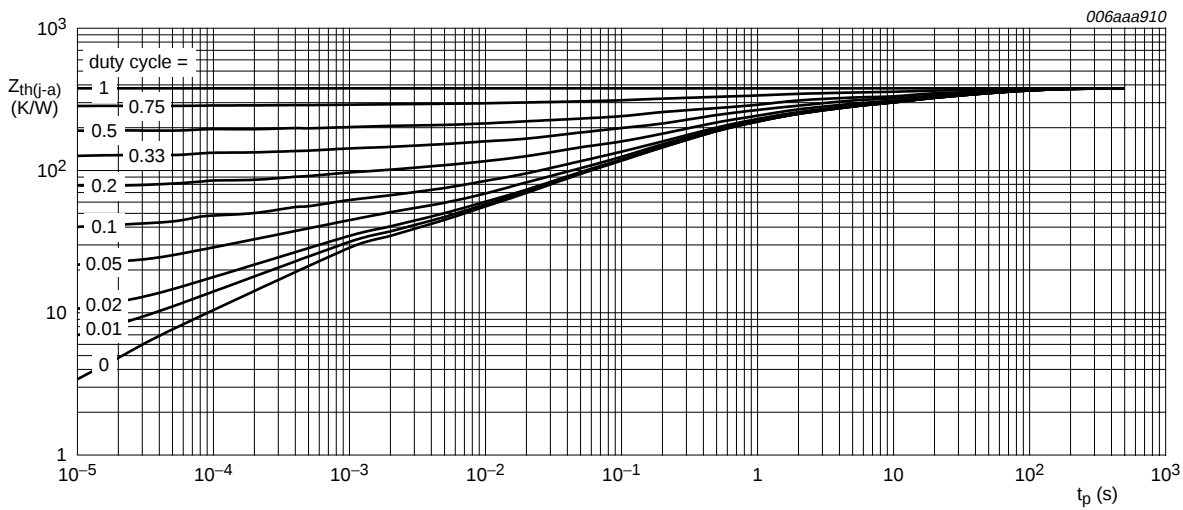


6. Thermal characteristics

Table 6. Thermal characteristics

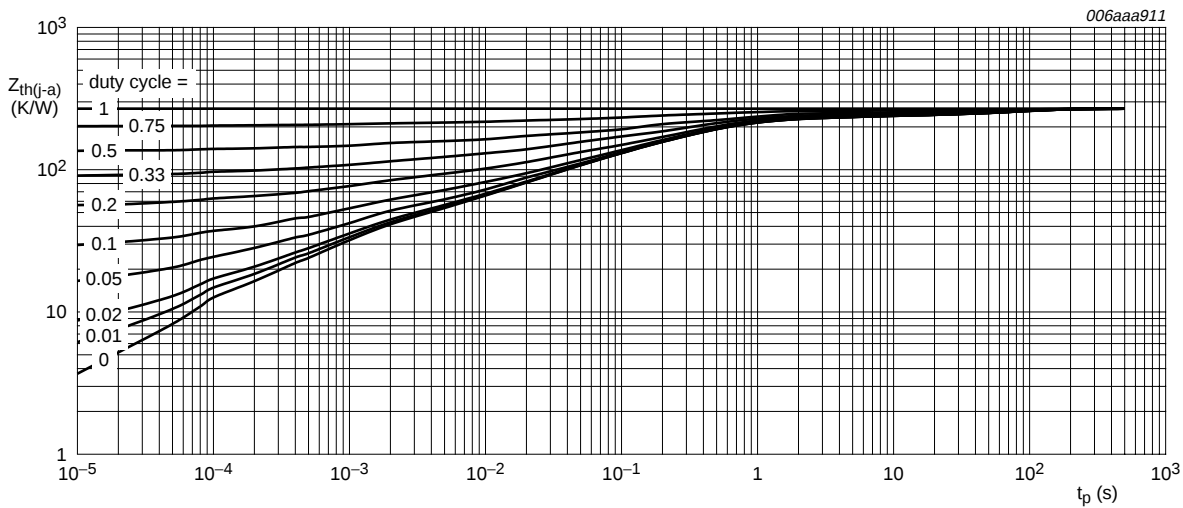
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Device						
R _{th(j-a)}	thermal resistance from junction to ambient	in free air	[1]	-	-	430 K/W
			[2]	-	-	312 K/W

- [1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.
- [2] Device mounted on a ceramic PCB, Al₂O₃, standard footprint.



FR4 PCB, standard footprint

Fig 2. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values



Ceramic PCB, Al_2O_3 , standard footprint

Fig 3. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

7. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Per transistor; for the PNP transistor with negative polarity						
I_{CBO}	collector-base cut-off current	$V_{CB} = 30\text{ V}; I_E = 0\text{ A}$	-	-	50	nA
		$V_{CB} = 30\text{ V}; I_E = 0\text{ A}; T_j = 150\text{ °C}$	-	-	10	μA
I_{EBO}	emitter-base cut-off current	$V_{EB} = 5\text{ V}; I_C = 0\text{ A}$	-	-	100	nA
h_{FE}	DC current gain					
	TR1 and TR3 (NPN)	$V_{CE} = 5\text{ V}; I_C = 1\text{ mA}$	200	320	450	
		$V_{CE} = 5\text{ V}; I_C = 100\text{ mA}$	95	165	-	
		$V_{CE} = 5\text{ V}; I_C = 200\text{ mA}$	24	40	-	
	TR2 (PNP)	$V_{CE} = 5\text{ V}; I_C = 1\text{ mA}$	200	270	450	
		$V_{CE} = 5\text{ V}; I_C = 100\text{ mA}$	95	120	-	
		$V_{CE} = 5\text{ V}; I_C = 200\text{ mA}$	24	45	-	
V_{CEsat}	collector-emitter saturation voltage	$I_C = 10\text{ mA}; I_B = 0.5\text{ mA}$	-	70	200	mV
		$I_C = 100\text{ mA}; I_B = 5\text{ mA}$	-	200	400	mV
		$I_C = 200\text{ mA}; I_B = 20\text{ mA}$	-	350	500	mV
V_{BEsat}	base-emitter saturation voltage	$I_C = 10\text{ mA}; I_B = 0.5\text{ mA}$	-	0.74	-	V
		$I_C = 100\text{ mA}; I_B = 5\text{ mA}$	-	0.91	-	V
		$I_C = 200\text{ mA}; I_B = 20\text{ mA}$	-	1	1.2	V
V_{BE}	base-emitter voltage	$V_{CE} = 5\text{ V}; I_C = 2\text{ mA}$	-	660	-	mV
Diode (D1)						
V_F	forward voltage	$I_F = 200\text{ mA}$	[1]	-	1.1	V
I_R	reverse current	$V_R = 60\text{ V}$	-	-	100	nA
		$V_R = 60\text{ V}; T_j = 150\text{ °C}$	-	-	100	μA
t_{rr}	reverse recovery time		[2]	-	6	ns
V_{FR}	forward recovery voltage		[3]	-	2	V
Transistor 1 (TR1)						
t_d	delay time	$I_C = 0.05\text{ A}; I_{B(on)} = 2.5\text{ mA}; I_{B(off)} = -2.5\text{ mA}$	-	12	-	ns
t_r	rise time		-	78	-	ns
t_{on}	turn-on time		-	90	-	ns
t_s	storage time		-	853	-	ns
t_f	fall time		-	205	-	ns
t_{off}	turn-off time		-	1058	-	ns

[1] Pulse test: $t_p \leq 300\text{ }\mu\text{s}$; $\delta \leq 0.02$.

[2] When switched from $I_F = 400\text{ mA}$ to $I_R = 400\text{ mA}$; $R_L = 100\text{ }\Omega$; measured at $I_R = 40\text{ mA}$.

[3] When switched from $I_F = 400\text{ mA}$; $t_r = 30\text{ ns}$.

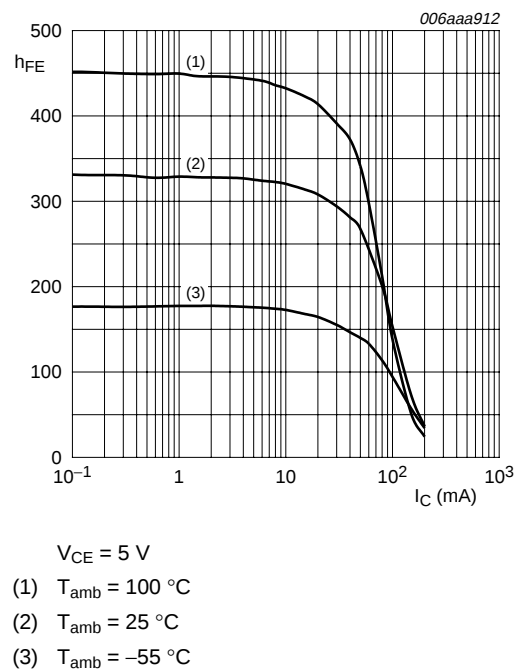


Fig 4. TR1 (NPN): DC current gain as a function of collector current; typical values

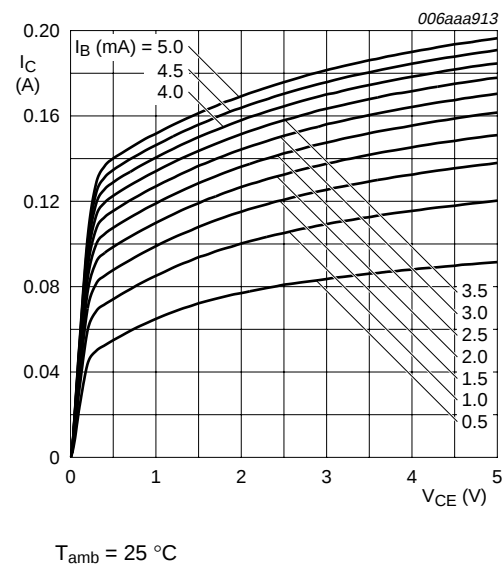


Fig 5. TR1 (NPN): Collector current as a function of collector-emitter voltage; typical values

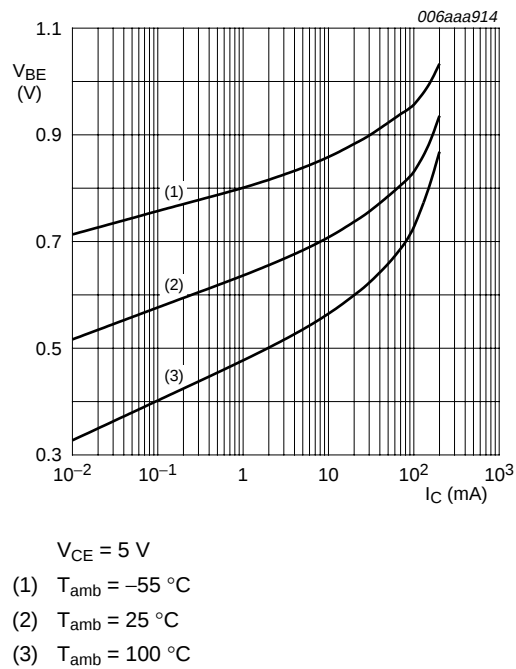


Fig 6. TR1 (NPN): Base-emitter voltage as a function of collector current; typical values

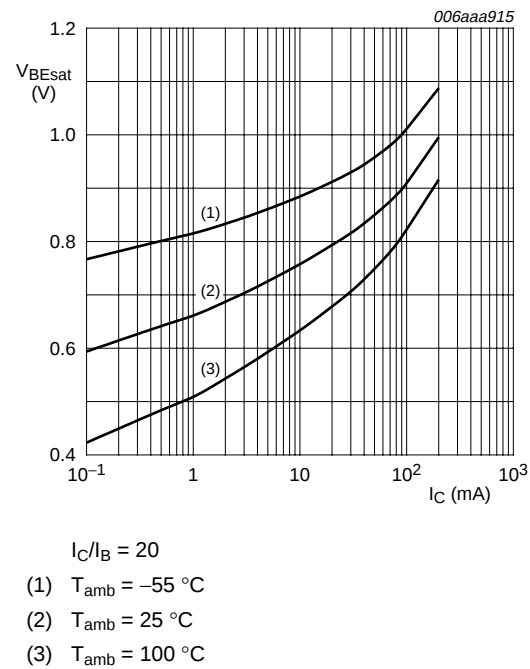
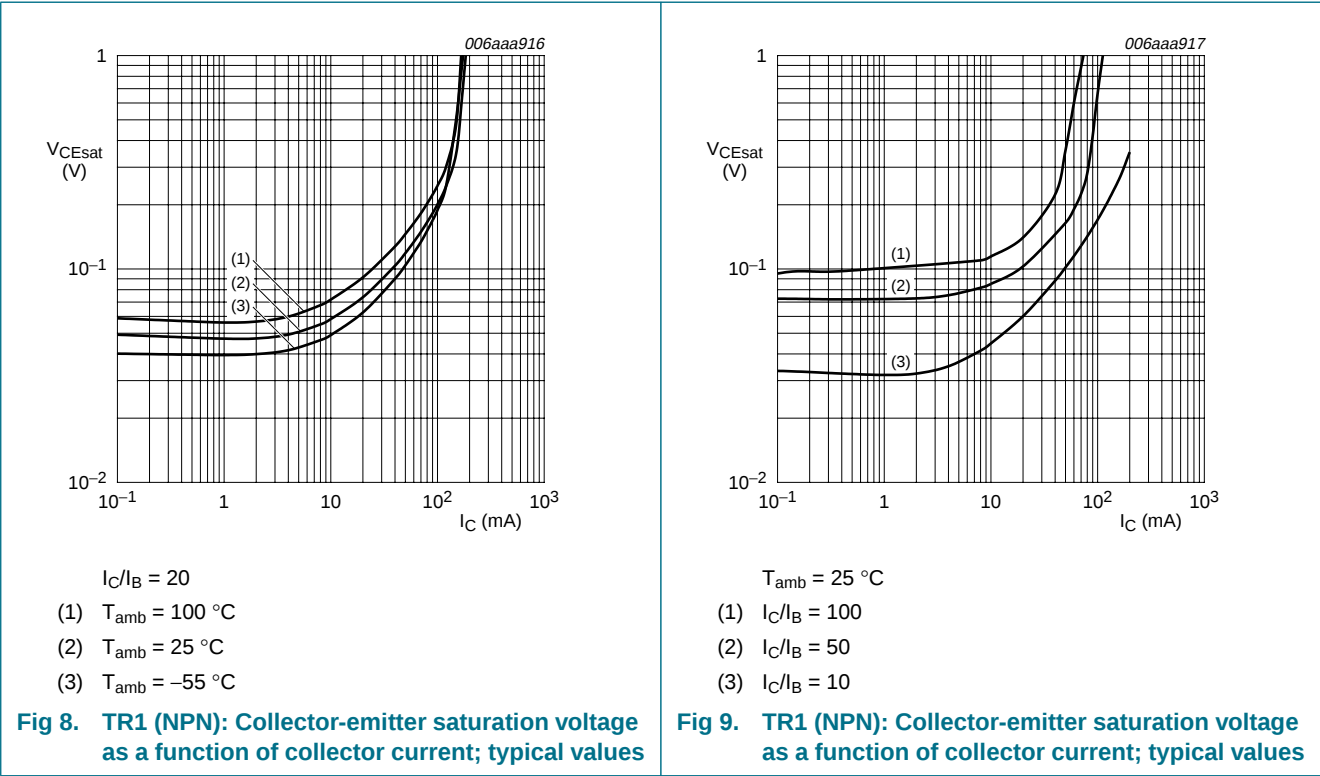
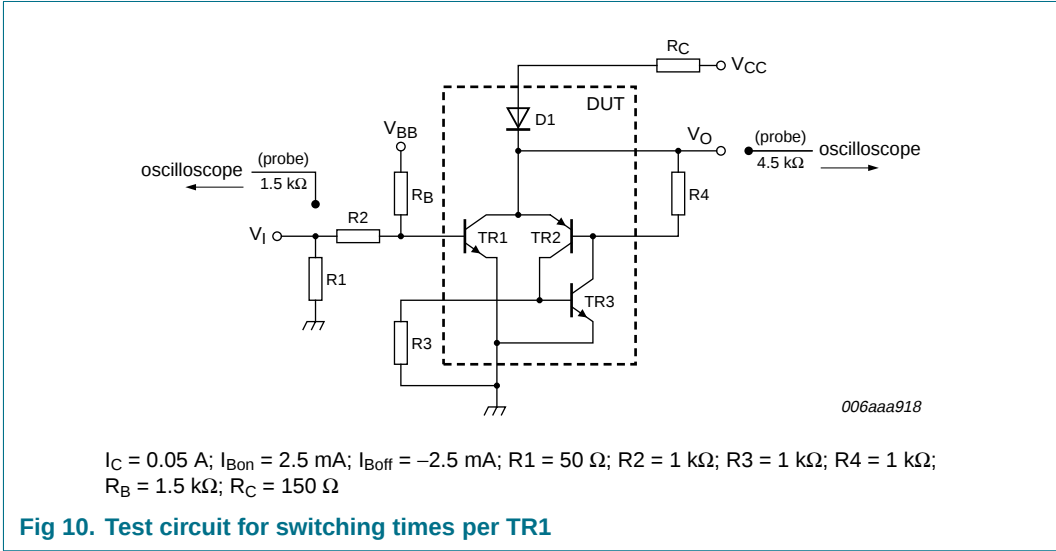


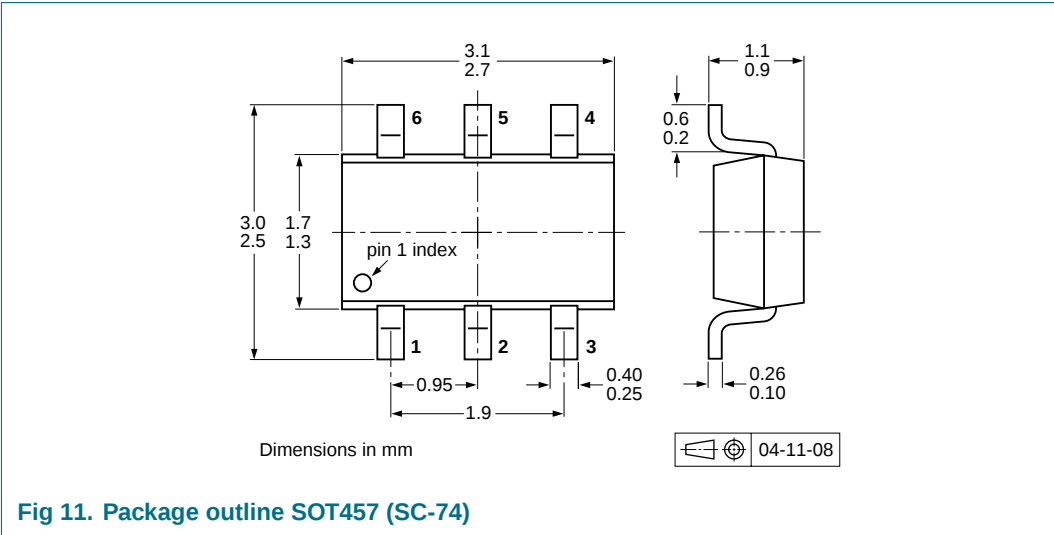
Fig 7. TR1 (NPN): Base-emitter saturation voltage as a function of collector current; typical values



8. Test information



9. Package outline



10. Packing information

Table 8. Packing methods					
The indicated -xxx are the last three digits of the 12NC ordering code. ^[1]					
Type number	Package	Description		Packing quantity	
				3000	10000
PMD9050D	SOT457	4 mm pitch, 8 mm tape and reel; T1	^[2]	-115	-135
		4 mm pitch, 8 mm tape and reel; T2	^[3]	-125	-165

[1] For further information and the availability of packing methods, see [Section 14](#).

[2] T1: normal taping

[3] T2: reverse taping

11. Soldering

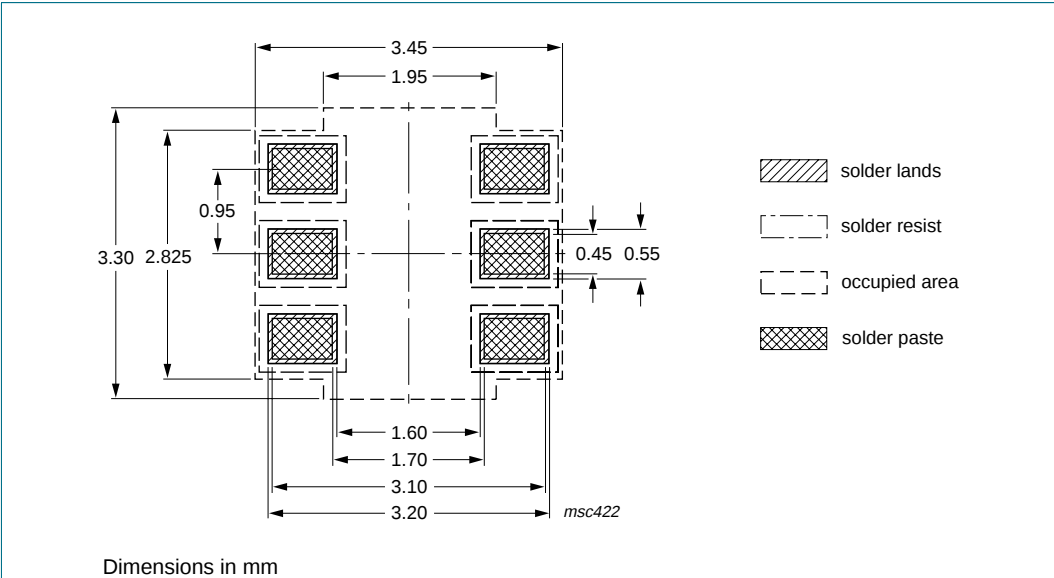


Fig 12. Reflow soldering footprint

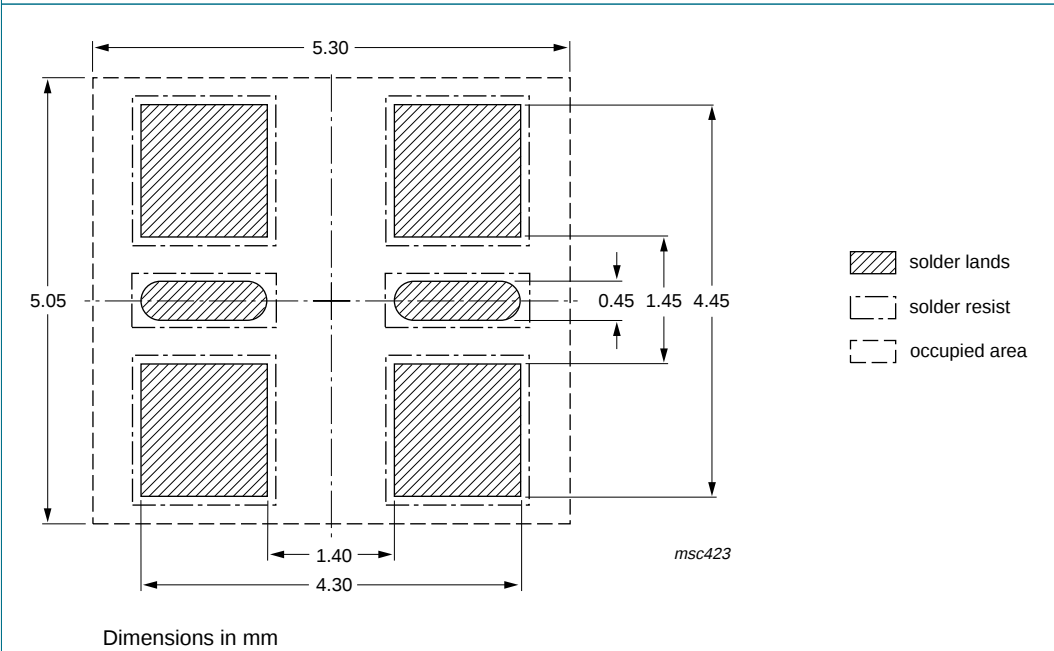


Fig 13. Wave soldering footprint

12. Revision history

Table 9. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PMD9050D_1	20061127	Product data sheet	-	-

13. Legal information

13.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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