Features

- **Up to 1.6 Million Used Gates and 596 Pads, with 3.3V, 3V, and 2.5V Libraries**
- **High Speed - 170 ps Gate Delay - 2 Input NAND, FO = 2 (Nominal)**
- **System Level Integration Technology Cores on Request**
- **SRAM and TRAM (Gate Level or Embedded)**
- **I/O Interfaces:**
  - **5V Tolerant/Compliant (S) or 3V (R) Matrix Options**
  - **CMOS, LVTTL, LVDS, PCI, USB**
  - **Output Currents Programmable from 2 to 24 mA, by Step of 2 mA**
- **250 MHz PLL (On Request), 220 MHz LVDS and 800 MHz Max Toggle Frequency at 3.3V**
- **Deep Submicron CAD Flow**
- **QML Q with SMD 5962-01B01**

Description

The MH1 Gate Array and Embedded Array families from Atmel are fabricated on a 0.35 micron CMOS process, with up to 4 levels of metal. This family features arrays with up to 1.6 million routable gates and 596 pads. The high density cores and/or high pin count capabilities of the MH1 family, coupled with the ability to embed memories on the same silicon, make the MH1 series of arrays one of the best choices for System Level Integration.

The MH1 series is supported by an advanced software environment based on industry standards linking proprietary and commercial tools. Verilog®, DFT®, Synopsys® and Vital are the reference front end tools. The Cadence® 'Logic Design Planner' floor planning associated with timing driven layout provides an efficient back end cycle.

The MH1 series comes as a dual use of the MH1RT series, without the latch up and total dose immunity features.

The MH1 series comes as the Atmel seventh generation of ASIC series designed for military and avionics types of applications in a 15-year time frame.

It is also made available to any of the currently available quality grades: commercial, industrial, automotive and military.

1.6M Used Gates 0.35 µm CMOS Sea of Gates/ Embedded Array

MH1

Rev. 4138G–AERO–05/04

Table 1. List of Available MH1 Matrices

Device Number	Typical Routable Gates	Max Pad Count	Max I/O Count	Gate Speed[1]	Max Sites Count
MH1099	519,000	332	324	170 ps	920 385
MH1156	764,000	412	404	170 ps	1 447 975
MH1242	1,198,000	512	504	170 ps	2 275 377
MH1332	1,634,000	596	588	170 ps	3 098 804

Note: 1. Nominal 2 Input NAND Gate FO = 2 at 3 volts.

Design

Design Systems Supported

Atmel supports several major software systems for design with complete macro cell libraries, as well as utilities for checking the netlist and accurate pre-route delay simulations.

The following design systems are supported:

Table 2. Design Systems Supported

System	Available Tools
Cadence®	Verilog-XL™ - Verilog Simulator Logic Design Planner™ - Floorplanner BuildGates® - Synthesis (Ambit)
Mentor/Model Tech™	Modelsim Verilog and VHDL (VITAL) Simulator DFT - Scan Insertion and ATPG, BIST
Synopsys®	Design Compiler® - Synthesis Primetime™ - Static Path Formality® - Equivalence Checking

Design Flow and Tools

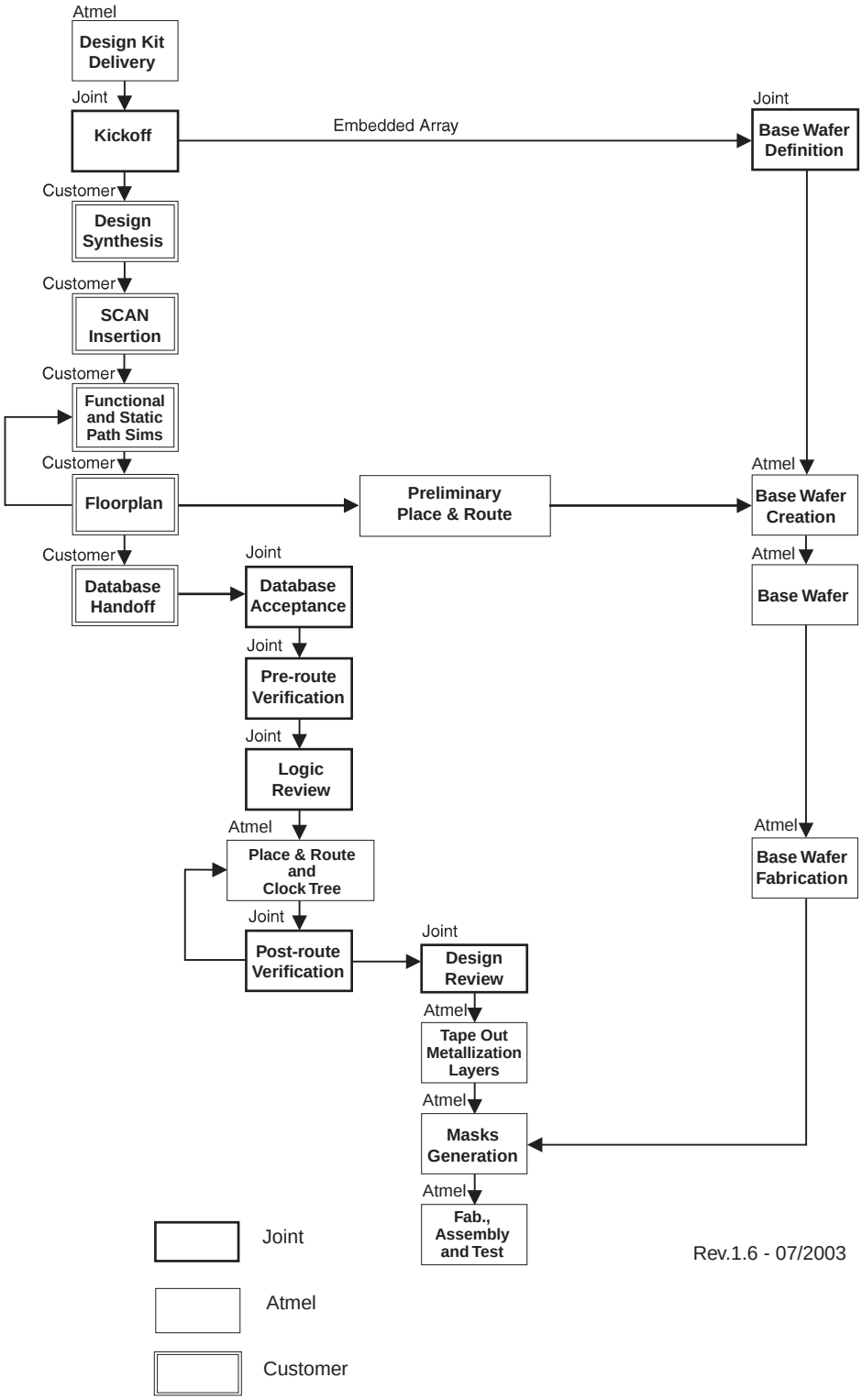
Atmel's design flow for Gate Array/Embedded Array is structured to allow the designer to consolidate the greatest number of system components possible onto the same silicon chip, using available third party design tools. Atmel's cell library reflects silicon performance over extremes of temperature, voltage, and process, and includes the effects of metal loading, inter-level capacitance, and edge rise and fall times. The Design Flow includes clock tree synthesis to minimize skew and latency. RC extraction is performed on final design database and incorporated into the timing analysis.

The Typical Gate Array/Embedded Array Design Flow, shown on page 4, provides a pictorial description of the typical interaction between Atmel's Gate Array/Embedded Array design staff and the customer. Atmel will deliver design kits to support the customer's synthesis, verification, floorplanning, and SCAN insertion activities. Tools such as Synopsys Synthesis, Cadence and Mentor Logic Simulators are used, and many others are available. Should a design include embedded memory or an embedded core, Atmel needs to understand the partition of the Array, and define the location of the memory blocks and/or cores (preliminary place and route) so that an underlayer layout model can be created (Base Wafer).

Following a Preliminary Design Review, so called Logic Review, the design is routed, and post-route RC data is extracted. Following post-route verification and a Final Design Review, so called Design Review, the design is taped out for fabrication.

The purpose of these reviews is to check the conformity of the design to Atmel rules, and acknowledge it in formal documents.

Figure 1. Typical Gate Array/Embedded Array Design Flow



Pin Definition Requirements

The corner pads are reserved for Power and Ground only. All other pads are fully programmable as Input, Output, Bidirectional, Power or Ground. When implementing a design with 5V tolerant buffers, one buffer site must be reserved for the V_{DD5} pin, which is used to distribute power to the buffers.

Figure 1. Gate Array

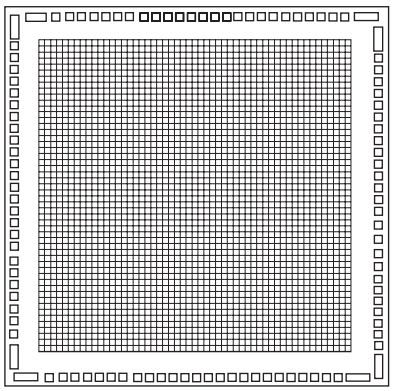
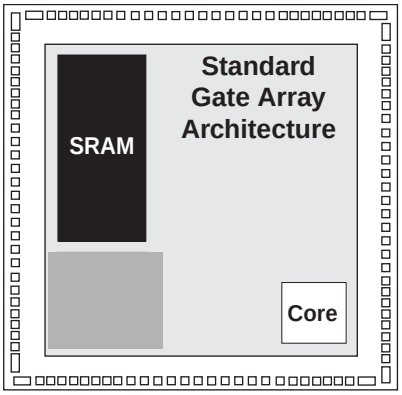


Figure 2. Embedded Array



I/O Site: Pad and Sub-Sections

The I/O sites can be configured as input, output, 3-state output and bidirectional buffers, each with pull-up or pull-down capability, if required, by utilizing their corresponding subsection. Bidirectional buffers are the result of an input and output buffers placed in adjacent sub-sections in the same I/O site. Special buffers may require multiple I/O sites. Oscillators require 2 I/O sites, each power and ground pin utilizes one I/O site.

PCI Buffers

PCI compatible input and output buffers are available for each bias voltage, 3V and 5V.

LVDS Buffers

Each LVDS buffer uses 2 I/O sites.

LVDS drivers are specific for each bias voltage and require one external current bias resistor per chip; LVDS receiver is the same for all bias voltages and requires 1 external line matching 100Ω resistor per receiver.

Memory Blocks

Memory blocks can be either synthesized on gates (when smaller than 8 bits) or compiled and embedded in the array itself.

ASIC Design Translation

Atmel has successfully translated existing designs from most major ASIC vendors (LSI Logic®, Motorola®, SMOS™, Oki®, NEC®, Fujitsu® and others) into the gate arrays. These designs have been optimized for speed and gate count and modified to add logic or memory, or replicated for a pin-to-pin compatible, drop-in replacement.

Design Entry

Design entry is performed by the customer using an Atmel ASIC library. A complete netlist and vector set must then be provided to Atmel. Upon acceptance of this data set, Atmel continues with the standard design flow.

FPGA and PLD Conversions

Atmel has successfully translated existing FPGA/PLD designs from most major vendors (Xilinx®, Actel™ and others) into the gate arrays. There are four primary reasons to convert from an FPGA/PLD to a gate array. Conversion of high volume devices for a single or combined design is cost effective. Performance can often be optimized for speed or low power consumption. Several FPGA/PLDs can be combined onto a single chip to minimize cost while reducing on-board space requirements. Finally, in situations where an FPGA/PLD was used for fast cycle time prototyping, a gate array may provide a lower cost answer for long-term volume production.

MH1 Series Cell Library

Atmel's MH1 Series gate arrays make use of an extensive library of macro cell structures, including logic cells, buffers and inverters, multiplexers, decoders, and I/O options. Soft macros are also available.

The MH1 Series PLL operates at frequencies of up to 250 MHz with minimal phase error and jitter, making it ideal for frequency synthesis of high speed on-chip clocks and chip to chip synchronization.

These cells are well characterized by use of SPICE modeling at the transistor level, with performance verified on manufactured test arrays. Characterization is performed over the rated temperature and voltage ranges to ensure that the simulation accurately predicts the performance of the finished product.

Cells	Number of Cells
Logic Cells	95
I/O Buffers	
3V or 2.5V or 3.3V	110
5V Tolerant	36
5V Compliant	70
Specific Cells	
LVDS, PCI	11

Electrical Characteristics

Absolute Maximum Ratings

Operating Ambient Temperature	-55℃ to +125℃
Storage Temperature	-65℃ to +150℃
Maximum Input Voltage	VDD +0.5V and VCC + 0.5V
Maximum 3.3V Operating Voltage	4V (VDD)
Maximum 5V Operating Voltage	6V (VCC)

*NOTE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

Applicable over recommended operating temperature and voltage range unless otherwise noted.

Table 3. 2.5V DC Characteristics

Symbol	Parameter	Buffer	Test Condition	Min	Typ	Max	Units
T_A	Operating Temperature	All	–	-55	25	125	C
V_{DD}	Supply Voltage	All	–	2.3	2.5	2.7	V
I_{IL}	Low-level Input Current Pull-up resistors PRU1 (1) Pull down resistor PRD1	CMOS	V_{IN} = V_{SS}	-1 70 -5	– –	1 230 5	µA
I_{IH}	High level Input Current Pull-up resistors PRU1 Pull down resistor PRD1 (2)	CMOS	V_{IN} = V_{DD}(max)	-1 -5 70	– –	1 5 540	µA
Ioz	High impedance state output current	All	Vin = Vdd or Vss, Vdd = Vdd (max) No pull resistor	-1	–	1	µA
Vil	Low level Input voltage	CMOS	–	–	–	0.3 Vdd	V
		PCI	–	–	–	0.325 Vdd	
		CMOS Schmitt level	–	–	–	0.62	
Vih	High level Input voltage	CMOS	–	0.7 Vdd	–		V
		PCI	–	0.475 Vdd	–	–	
		CMOS Schmitt level	–	1.56	–		
Delta V	CMOS Hysterisys	–	–	–	0.42		V
V_{OL}	Low-level Output Voltage (3)	PO11	I_{OL} = 0.8 mA, Vdd = Vdd (min)	–	–	0.4	V
Voh	High level output voltage (4)	PO11	Ioh = -0.6 mA, Vdd = Vdd (min)	2	–		V
Ios	Output short circuit current Iosn Iosp	 PO11 PO11	Vdd = Vdd (max), Vout = Vdd Vouy = Vss	–	–	 15 8	mA
Iccsb	Leakage current per cell	–	Vdd = Vdd (max)	–	0.27	4	nA
Iccop	Dynamic current per gate	–	Vdd = Vdd (max)	–	–	0.32	µW/MHz

1. For standard pull-ups: PRU(#), # = {1-31} index for Ron: Ron = # x RO where RO = 19 kΩ typ, 30 kΩ max, 12 kΩ min
2. For standard pull-downs: PRD(#), # = {1-31} index for Ron: Ron = # x RO where RO = 11 kΩ typ, 30 kΩ max, 5 kΩ min
3. For output buffers PO (1-C) (1-C):
   1-C: hex value: convert hex to decimal x IO = p and n-channel output drive
   IO = 1.6 mA for standard buffers measured at Vol = 0.4V
4. For output buffers PO (1-C) (1-C):
   1-C: hex value: convert hex to decimal x IO = p and n-channel output drive
   IO = -1.6 mA for standard buffers measured at Voh = 2V

Applicable over recommended operating temperature and voltage range unless otherwise noted.

Table 4. 3V DC Characteristics

Symbol	Parameter	Buffer	Test Condition	Min	Typ	Max	Units
T_A	Operating Temperature	All	–	-55	25	125	°C
V_{DD}	Supply Voltage	All	–	2.7	3.0	3.3	V
I_{IL}	Low-level Input Current Pull-up resistors PRU1 (1) Pull down resistor PRD1	CMOS	V_{IN} = V_{SS}	-1 108 -5	–	1 330 5	µA
I_{IH}	High level Input Current Pull-up resistors PRU1 Pull down resistor PRD1 (2)	CMOS	V_{IN} = V_{DD} (max)	-1 -5 108	–	1 5 825	µA
Ioz	High impedance state output current	All	Vin = Vdd or Vss, Vdd = Vdd (max) No pull resistor	-1	–	1	µA
Vil	Low level Input voltage	CMOS	–	–	–	0.8	V
		PCI	–	–	–	0.325 Vdd	
		CMOS Schmitt level	–	–	–	0.72	
Vih	High level Input voltage	CMOS	–	2	–	–	V
		PCI	–	0.475 Vdd	–	–	
		CMOS Schmitt level	–	1.89	–	–	
Delta V	CMOS Hysterisis	–	–	–	0.53	–	V
V_{OL}	Low-level Output Voltage (3)	PO11	I_{OL} = 1 mA, Vdd = Vdd (min)	– –	–	0.4	V
Voh	High level output voltage (4)	PO11	Ioh = -0.6 mA, Vdd = Vdd (min)	2.4	–		V
Ios Iosn Iosp	Output short circuit current	PO11 PO11	Vdd = Vdd (max), Vout = Vdd Vouy = Vss	–	–	21 12	mA
Iccsb	Leakage current per cell	–	Vdd = Vdd (max)	–	0.6	5	nA
Iccop	Dynamic current per gate	–	Vdd = Vdd (max)	–	–	0.54	µW/MHz

1. For standard pull-ups: PRU(#), # = {1-31} index for Ron: Ron = # x RO where RO = 15 kΩ typ, 25 kΩ max, 10 kΩ min
2. For standard pull-downs:PRD(#), # = {1-31} index for Ron: Ron = # x RO where RO = 9 kΩ typ, 25 kΩ max, 4 kΩ min
3. For output buffers PO (1-C) (1-C):
   1-C: hex value: convert hex to decimal x IO = p and n-channel output drive
   IO = 1.8 mA for standard buffers (including cold sparing) measured at Vol = 0.4V
4. For output buffers PO (1-C) (1-C):
   1-C: hex value: convert hex to decimal x IO = p and n-channel output drive
   IO = -1.8 mA for standard buffers (including cold sparing) measured at Voh = 2.4V

Applicable over recommended operating temperature and voltage range unless otherwise noted.

Table 5. 3.3V DC Characteristics

Symbol	Parameter	Buffer	Test Condition	Min	Typ	Max	Units
T_A	Operating Temperature	All		-55	25	125	°C
V_{DD}	Supply Voltage	All		3	3.3	3.6	V
I_{IL}	Low-level Input Current Pull-up resistors PRU1 (1) Pull down resistor PRD1	CMOS	V_{IN} = V_{SS}	-1 120 -5		1 400 5	µA
I_{IH}	High level Input Current Pull-up resistors PRU1 Pull down resistor PRD1 (2)	CMOS	V_{IN} = V_{DD} (max)	-1 -5 150		1 5 900	µA
Ioz	High impedance state output current	All	Vin = Vdd or Vss, Vdd = Vdd (max) No pull resistor	-1		1	µA
Vil	Low level Input voltage	CMOS				0.8	V
		PCI				0.325 Vdd	
		CMOS Schmitt level				0.8	
Vih	High level Input voltage	CMOS		2			V
		PCI		0.475 Vdd			
		CMOS Schmitt level		2			
Delta V	CMOS Hysterisis				0.6		V
V_{OL}	Low-level Output Voltage (3)	PO11	I_{OL} = 2 mA, Vdd = Vdd (min)			0.4	V
Voh	High level output voltage (4)	PO11	Ioh = -1.8 mA, Vdd = Vdd (min)	2.4			V
Ios	Output short circuit current Iosn Iosp	 PO11 PO11	Vdd = Vdd (max), Vout = Vdd Vouy = Vss			 23 13	mA
Iccsb	Leakage current per cell		Vdd = Vdd (max)		0.7	5	nA
Iccop	Dynamic current per gate		Vdd = Vdd (max)			0.69	µW/MHz

1. For standard pull-ups: PRU(#), # = {1-31} index for Ron: Ron = # x RO where RO = 14 kΩ typ, 25 kΩ max, 9 kΩ min
2. For standard pull-downs:PRD(#), # = {1-31} index for Ron: Ron = # x RO where RO = 8 kΩ typ, 20 kΩ max, 4 kΩ min
3. For output buffers PO (1-C) (1-C):
   1-C: hex value: convert hex to decimal x IO = p and n-channel output drive
   IO = 2 mA for standard buffers measured at Vol = 0.4V
4. For output buffers PO (1-C) (1-C):
   1-C: hex value: convert hex to decimal x IO = p and n-channel output drive
   IO = -2 mA for standard buffers measured at Voh = 2.4V

Applicable over recommended operating temperature and voltage range unless otherwise noted.

Table 6. 5V DC Characteristics

Symbol	Parameter	Buffer	Test Condition	Min	Typ	Max	Units
T_A	Operating Temperature	All	–	-55	25	125	°C
V_{DD}	Supply Voltage	5V Tolerant	–	3.0	3.3	3.6	V
V_{CC}	Supply Voltage	5V Compliant	–				
I_{IL}	Low-level Input Current Pull-up resistors PRU1 (1) Pull down resistor PRD1	CMOS	V_{IN} = V_{SS}	-1 180 -5	–	1 690 5	µA
I_{IH}	High level Input Current Pull-up resistors PRU1 Pull down resistor PRD1 (2)	CMOS	V_{IN} = V_{DD} (max)	-1 -5 30	–	1 5 400	µA
Ioz	High impedance state output current	All	Vin = Vdd or Vss, Vdd = Vdd (max) No pull resistor	-1	–	1	µA
Vil	Low level Input voltage	PICV, PICV5	–	–	–	0.8	V
		PCI	–	–	–	0.325 Vdd	
		CMOS Schmitt level	–	–	–	0.8	
Vih	High level Input voltage	PICV, PICV5	–	2	–	–	V
		PCI	–	0.475 Vdd	–	–	
		CMOS Schmitt level	–	2	–	–	
V_{OL} (3)	Low Voltage/2.5V range Low Voltage/3.0V range Low Voltage/3.3V range Low Voltage/2.5V range Low Voltage/3.0V range Low Voltage/3.3V range	PO11V PO11V PO11V PO11V5 PO11V5 PO11V5	Iol = 0.5 mA Iol = 0.6 mA Iol = 1.2 mA Iol = 1.1mA Iol = 1.3 mA Iol = 1.5 mA	–	–	0.4	V
Voh (4)	Low Voltage/2.5V range Low Voltage/3.0V range Low Voltage/3.3V range Low Voltage/2.5V range Low Voltage/3.0V range Low Voltage/3.3V range	PO11V PO11V PO11V PO11V5 PO11V5 PO11V5	Ioh = 0.5 mA Ioh = 0.6 mA Ioh = 1.2 mA Ioh = 1.1mA Ioh = 1.3 mA Ioh = 1.5 mA	2 2.4 2.4 2 2.4 2.4	–	–	V
Ios	Output short circuit current Iosn Iosp	 PO11V PO11V	Vdd = Vdd (max), Vout = Vdd Vouy = Vss	–	–	 28 17	mA

1. For 5V tolerant/compliant pull-ups: PRU(#), # = {1-31} index for Ron: Ron = # x RO where RO = 14 kΩ typ, 25 kΩ max, 8 kΩ min.
2. For 5V tolerant/compliant pull-downs: PRD(#), # = {1-31} index for Ron: Ron = # x RO where:
   RO = 19 kΩ typ, 45 kΩ max, 9 kΩ min in 3.3V range,
   RO = 23 kΩ typ, 55 kΩ max, 11 kΩ min in 3V range,
   RO = 36 kΩ typ, 80 kΩ max, 17 kΩ min in 2.5V range,

3. For output buffers PO (1-C) (1-C):
   1-C: hex value: convert hex to decimal x IO = p and n-channel output drive
   IO = 1.4 mA for tolerant buffers in 3.3V range (Vcc = 4.5V) measured at Vol = 0.4V
   IO = 1.3 mA for tolerant buffers in 3.0V range (Vcc = 4.5V) measured at Vol = 0.4V
   IO = 1.0 mA for tolerant buffers in 2.5V range (Vcc = 4.5V) measured at Vol = 0.4V
   IO = 1.6 mA for compliant buffers in 3.3V range (Vcc = 4.5 V) measured at Vol = 2.4V
   IO = 1. mA for compliant buffers in 3.0V range (Vcc = 4.5 V) measured at Vol = 2.4V
   IO = 1.1 mA for compliant buffers in 2.5V range (Vcc = 4.5 V) measured at Vol = 2.0 V
4. IO = -1.4 mA for tolerant buffers in 3.3V range (Vcc = 4.5V) measured at Vol = 2.4V
   IO = -1.3 mA for tolerant buffers in 3.0V range (Vcc = 4.5V) measured at Vol = 2.4V
   IO = -1.0 mA for tolerant buffers in 2.5V range (Vcc = 4.5V) measured at Vol = 2V
   IO = -1.6 mA for compliant buffers in 3.3V range (Vcc = 3.3V) measured at Vol = 2.4V
   IO = -1.4 mA for compliant buffers in 3.0V range (Vcc = 3 V) measured at Vol = 2.4V
   IO = -1.1 mA for compliant buffers in 2.5V range (Vcc = 4.5 V) measured at Vol = 2.0V

DC and AC Characteristics for LVDS Driver

Applicable over recommended operating temperature and voltage range unless otherwise noted.

Table 7. 2.5V LVDS Driver DC/AC Characteristics (Preliminary)

Symbol	Parameter	Test Condition	Min	Max	Units	Comments
T_A	Operating Temperature	–	-55	125	°C	–
V_{DD}	Supply Voltage	–	2.3	2.7	V	–
|VOD|	Output differential voltage	Rload = 100Ω	230.7	446.5	mV	Figure 3
Vol	Output voltage low	Rload = 100Ω	1224	1817	mV	Figure 3
Voh	Output voltage high	Rload = 100Ω	993	1406	mV	Figure 3
VOS	Output offset voltage	Rload = 100Ω	1108	1610	mV	Figure 3
|Delta VOD|	Change in |VOD| between "0" and "1"	Rload = 100Ω	0	50	mV	–
|Delat VOS|	Change in |VOS| between "0" and "1"	Rload = 100Ω	0	100	mV	–
ISA, ISB	Output current	Drivers shorted to ground or VDD	1.0	6.3	mA	–
ISAB	Output current	Drivers shorted together	2.4	4.8	mA	–
Rbias	Bias resistor	–	9.8	10.2	kΩ	1 per chip
Ibias	Bias static current	–	5.8	11.7	mA	–
Fmax	Maximum operating frequency	VDD = 2.5V ± 0.2V	–	180	MHz	Consumption 14.8 mA
Clock	Clock signal duty cycle	Max frequency	45	55	%	–
Tfall	Fall time 80 - 20%	Rload = 100Ω	669	1178	ps	Figure 4
Trise	Rise time 20 - 80%	Rload = 100Ω	670	1167	ps	Figure 4
Tp	Propagation delay	Rload = 100Ω	1270	2660	ps	Figure 4
Tsk1	Duty cycle skew	Rload = 100Ω	0	110	ps	–
Tsk2	Channel to channel skew (same edge)	Rload = 100Ω	0	50	ps	–

Applicable over recommended operating temperature and voltage range unless otherwise noted.

Table 8. 3V LVDS Driver DC/AC Characteristics

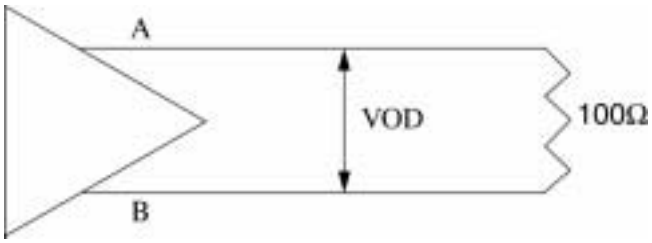
Symbol	Parameter	Test Condition	Min	Max	Units	Comments
T_A	Operating Temperature	–	-55	125	°C	–
V_{DD}	Supply Voltage	–	2.7	3.3	V	–
|VOD|	Output differential voltage	Rload = 100Ω	244	462	mV	Figure 3
Vol	Output voltage low	Rload = 100Ω	1088	1775	mV	Figure 3
Voh	Output voltage high	Rload = 100Ω	828	1358	mV	Figure 3
VOS	Output offset voltage	Rload = 100Ω	958	‘568	mV	Figure 3
|Delta VOD|	Change in |VOD| between "0" and "1"	Rload = 100Ω	0	50	mV	–
|Delat VOS|	Change in |VOS| between "0" and "1"	Rload = 100Ω	0	150	mV	–
ISA, ISB	Output current	Drivers shorted to ground or VDD	1.0	6.3	mA	–
ISAB	Output current	Drivers shorted together	2.6	5	mA	–
Rbias	Bias resistor	–	12.8	13.2	kΩ	1 per chip
Ibias	Bias static current	–	6.5	13.8	mA	–
Fmax	Maximum operating frequency	VDD = 3.3V ± 0.3V	–	200	MHz	Consumption 18.6 mA
Clock	Clock signal duty cycle	Max frequency	45	55	%	–
Tfall	Fall time 80 - 20%	Rload = 100Ω	512	968	ps	Figure 4
Trise	Rise time 20 - 80%	Rload = 100Ω	512	970	ps	Figure 4
Tp	Propagation delay	Rload = 100Ω	1150	2300	ps	Figure 4
Tsk1	Duty cycle skew	Rload = 100Ω	0	70	ps	–
Tsk2	Channel to channel skew (same edge)	Rload = 100Ω	0	50	ps	–

Applicable over recommended operating temperature and voltage range unless otherwise noted.

Table 9. 3.3V LVDS Driver DC/AC Characteristics (Preliminary)

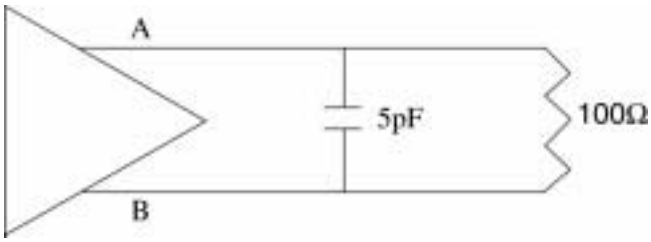
Symbol	Parameter	Test Condition	Min	Max	Units	Comments
T_A	Operating Temperature	–	-55	125	°C	–
V_{DD}	Supply Voltage	–	3	3.6	V	–
|VOD|	Output differential voltage	Rload = 100Ω	251.4	452.2	mV	Figure 3
Vol	Output voltage low	Rload = 100Ω	1071	1731	mV	Figure 3
Voh	Output voltage high	Rload = 100Ω	804	1323	mV	Figure 3
VOS	Output offset voltage	Rload = 100Ω	937	1527	mV	Figure 3
|Delta VOD|	Change in |VOD| between "0" and "1"	Rload = 100Ω	0	50	mV	–
|Delat VOS|	Change in |VOS| between "0" and "1"	Rload = 100Ω	0	200	mV	–
ISA, ISB	Output current	Drivers shorted to ground or VDD	1.0	6.2	mA	–
ISAB	Output current	Drivers shorted together	2.6	4.8	mA	–
Rbias	Bias resistor	–	16.3	16.7	kΩ	1 per chip
Ibias	Bias static current	–	7	14.6	mA	–
Fmax	Maximum operating frequency	VDD = 3.3V ± 0.3V	–	220	MHz	Consumption 20.9 mA
Clock	Clock signal duty cycle	Max frequency	45	55	%	–
Tfall	Fall time 80 - 20%	Rload = 100Ω	445	838	ps	Figure 4
Trise	Rise time 20 - 80%	Rload = 100Ω	445	841	ps	Figure 4
Tp	Propagation delay	Rload = 100Ω	1120	2120	ps	Figure 4
Tsk1	Duty cycle skew	Rload = 100Ω	0	80	ps	–
Tsk2	Channel to channel skew (same edge)	Rload = 100Ω	0	50	ps	–

Figure 3. Test termination measurements



$$VOS = \frac{(VA + VB)}{2}$$

Figure 4. Rise and Fall Measurements



Applicable over recommended operating temperature and voltage range unless otherwise noted.

Table 10. LVDS Receiver DC/AC Characteristics

Symbol	Parameter	Test Condition	Min	Max	Units
T_A	Operating Temperature	–	-55	125	°C
V_{DD}	Supply Voltage	–	2.3	3.6	V
Vi	Input voltage range	–	0	2400	mV
Vidth	Input differential voltage	–	-100	+100	mV
Tp	Propagation delay	Cout = 50 pF, VDD = 2.5V ± 0.2V Cout = 50 pF, VDD = 3.0V ± 0.3V Cout = 50 pF, VDD = 3.3V ± 0.3V	0.9 0.7 0.7	3.5 2.7 2.4	ns
Tskew	Duty cycle distortion	Cout = 50 pF	-	500	ps

Table 11. I/O Buffers DC Characteristics

Symbol	Parameter	Test Condition	Typical	Units
C_{IN}	Capacitance, Input Buffer (die)	3V	2.4	pF
C_{OUT}	Capacitance, Output Buffer (die)	3V	5.6	pF
$C_{I/O}$	Capacitance, Bi-Directional	3V	6.6	pF

Testability Techniques

For complex designs, involving blocks of memory and/or cores, careful attention must be given to design-for-test techniques. The sheer size of complex designs and the number of functional vectors that would need to be created to exercise them fully, strongly suggests the use of more efficient techniques. Combinations of SCAN paths, multiplexed access to memory and/or core blocks, and built-in-self-test logic must be employed, in addition to functional test patterns, to provide both the user and Atmel the ability to test the finished product.

An example of a highly complex design could include a PLL for clock management or synthesis, SRAM and glue logic to support the inter connectivity of each of these blocks. The design of each of these blocks must take into consideration the fact that the manufactured device will be tested on a high performance digital tester. Combinations of parametric, functional, and structural tests, defined for digital testers, should be employed to create a suite of manufacturing tests.

The type of block dictates the type of testability technique to be employed. The PLL will, by construction, provide access to key nodes so that functional and/or parametric testing can be performed. Since a digital tester must control all the clocks during the testing of a Gate Array/Embedded Array, provision must be made for the VCO to be bypassed. Atmel's PLLs include a multiplexing capability for just this purpose. The addition of a few pins will allow other portions of the PLL to be isolated for test, without impinging upon the normal functionality.

Access to SRAM blocks must be provided so that controllability and observability of the inputs and outputs to the blocks are achieved with the minimum amount of preconditioning. SRAM blocks need to provide access to both address and data ports so that comprehensive memory tests can be performed. Multiplexing I/O pins provides a method for providing this accessibility.

The glue logic can be designed using full SCAN techniques to enhance its testability.

It should be noted that, in almost all of these cases, the purpose of the testability technique is to provide Atmel a means to assess the structural integrity of a Gate Array/Embedded Array, i.e., sort devices with manufacturing-induced defects. All of the techniques described above should be considered supplemental to a set of patterns which exercise the functionality of the design in its anticipated operating modes.

Advanced Packaging

The MH1 Series are offered in ceramic packages, multi-layers quad flat packs (MQFP), and a BGA based on ceramic land grid arrays, so called Multi Layer Column Grid Array (MCGA). Awide range of plastic package is also proposed. High volume onshore and offshore contractors can provide assembly and test for commercial or industrial quality grades, when agreed.

Table 12. Packaging Options

Package Type [1]	**Pin Count**
Plastic Packages	[2]
MQFP[3]	196, 256 and 352
MCGA[3]	349, 472 (1.27 mm pitch), and 576 (1 mm pitch)

Notes:
1. Contact Atmel local desing centres to check the availability of the matrix/package combination.
2. Contact Atmel for availability.
3. Four decks package.

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