Features

- 16 Channel GPS Correlator
  - 8192 Search Bins with GPS Acquisition Accelerator
  - Accuracy: 2.5m CEP (Stand-Alone, S/A off)
  - Time to First Fix: 34s (Cold Start)
  - Acquisition Sensitivity: –140 dBm
  - Tracking Sensitivity: –150 dBm
- Utilizes the ARM7TDMI® ARM® Thumb® Processor Core
  - High-performance 32-bit RISC Architecture
  - High-density 16-bit Instruction Set
  - EmbeddedICE™ (In-circuit Emulator)
- 128 Kbyte Internal RAM
- 384 Kbyte Internal ROM, Firmware Version V5.0
- Position Technology Provided by u-blox
- Fully Programmable External Bus Interface (EBI)
  - Maximum External Address Space of 8 Mbytes
  - Up to 4 Chip Selects
  - Software Programmable 8-bit/16-bit External Data Bus
- 6-channel Peripheral Data Controller (PDC)
- 8-level Priority, Individually Maskable, Vectored Interrupt Controller
  - 2 External Interrupts
- 32 User-programmable I/O Lines
- 1 USB Device Port
  - Universal Serial Bus (USB) V2.0 Full-speed Device
  - Embedded USB V2.0 Full-speed Transceiver
  - Suspend/Resume Logic
  - Ping-pong Mode for Isochronous and Bulk Endpoints
- 2 USARTs
  - 2 Dedicated Peripheral Data Controller (PDC) Channels per USART
- Master/Slave SPI Interface
  - 2 Dedicated Peripheral Data Controller (PDC) Channels
  - 8-bit to 16-bit Programmable Data Length
  - 4 External Slave Chip Selects
- Programmable Watchdog Timer
- Advanced Power Management Controller (APMC)
  - Peripherals Can Be Deactivated Individually
  - Geared Master Clock to Reduce Power Consumption
  - Sleep State with Disabled Master Clock
  - Hibernate State with 32.768 kHz Master Clock
- Real Time Clock (RTC)
- 2.3V to 3.6V or 1.8V Core Supply Voltage
- Includes Power Supervisor
- 1.8V to 3.3V User-definable I/O Voltage for Several GPIOs with 5V Tolerance
- 4 Kbytes Battery Backup Memory
- 9 mm × 9 mm 100-pin BGA Package (LFBGA100)
- RoHS-compliant

GPS Baseband Processor

ATR0621P

4890H–GPS–08/08

1. Description

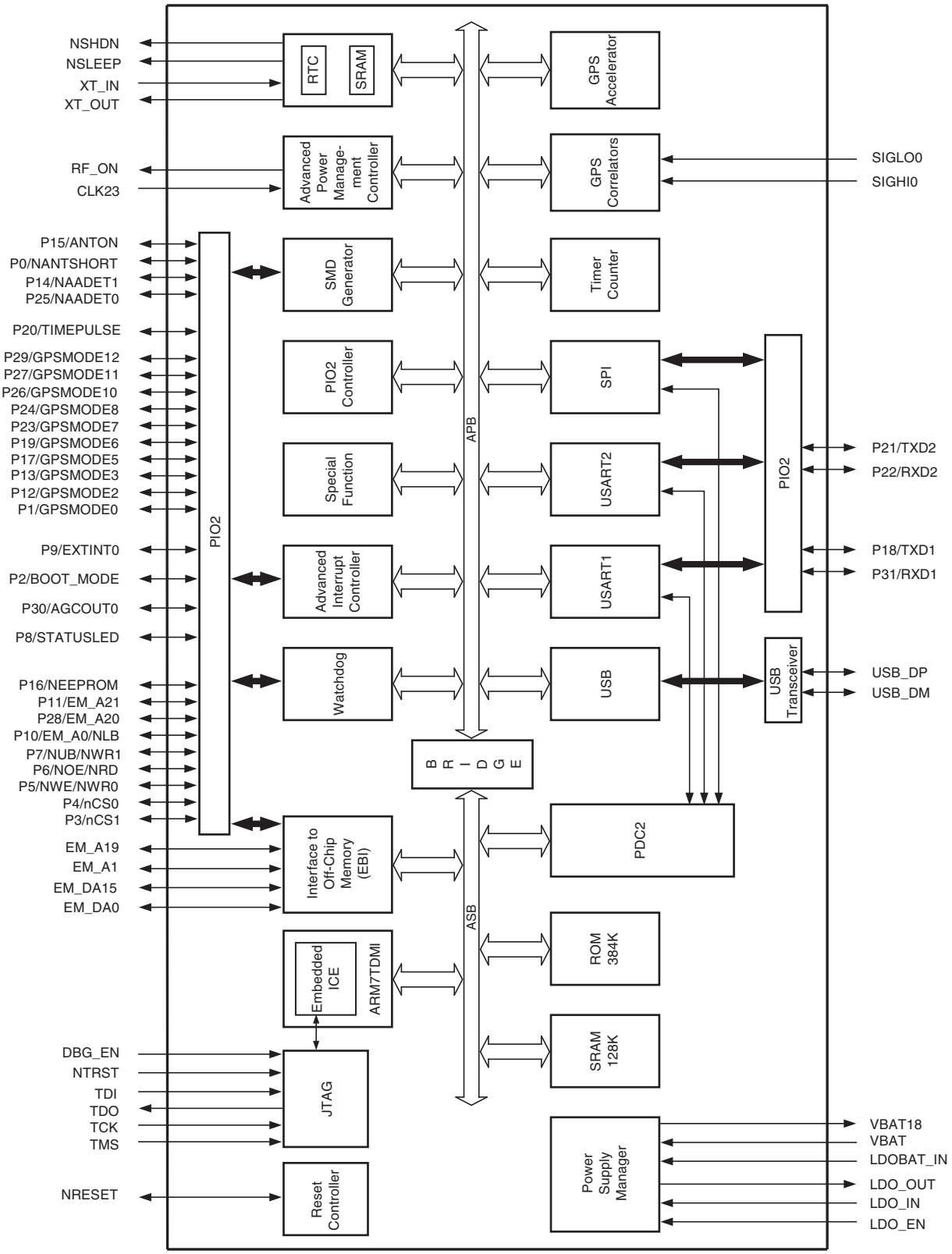
The GPS baseband processor ATR0621P includes a 16-channel GPS correlator and is based on the ARM7TDMI processor core.

This processor has a high-performance 32-bit RISC architecture and very low power consumption. In addition, a large number of internally banked registers result in very fast exception handling, making the device ideal for real-time control applications. The ATR0621P has two USART and an USB device port. This port is compliant with the Universal Serial Bus (USB) V2.0 full-speed device specification. The ATR0621P has a direct connection to off-chip memory, including Flash, through the External Bus Interface (EBI).

The ATR0621P includes full GPS firmware, licensed from u-blox AG, which performs the basic GPS operation, including tracking, acquisition, navigation and position data output. For normal PVT (Position/Velocity/Time) applications, there is no need for off-chip Flash memory or ROM. The firmware supports e.g. the NMEA® protocol (2.1 and 2.3), a binary protocol for PVT data, configuration and debugging, the RTCM protocol for DGPS, SBAS (WAAS, EGNOS and MSAS) and A-GPS (aiding). It is also possible to store the configuration settings in an optional external EEPROM.

The ATR0621P is manufactured using the Atmel® high-density CMOS technology. By combining the ARM7TDMI microcontroller core with on-chip SRAM, 16-channel GPS correlator and a wide range of peripheral functions on a monolithic chip, the ATR0621P provides a highly-flexible and cost-effective solution for GPS applications.

Figure 1-1. Block Diagram



2. Architectural Overview

2.1 Description

The ATR0621P architecture consists of two main buses, the Advanced System Bus (ASB) and the Advanced Peripheral Bus (APB). The ASB is designed for maximum performance. It interfaces the processor with the on-chip 32-bit memories and the external memories and devices by means of the External Bus Interface (EBI). The APB is designed for accesses to on-chip peripherals and is optimized for low power consumption. The AMBA™ Bridge provides an interface between the ASB and the APB.

An on-chip Peripheral Data Controller (PDC2) transfers data between the on-chip USARTs/SPI and the on-chip and off-chip memories without processor intervention. Most importantly, the PDC2 removes the processor interrupt handling overhead and significantly reduces the number of clock cycles required for a data transfer. It can transfer up to 64K contiguous bytes without reprogramming the starting address. As a result, the performance of the microcontroller is increased and the power consumption reduced.

The ATR0621P peripherals are designed to be easily programmable with a minimum number of instructions. Each peripheral has a 16 Kbyte address space allocated in the upper 3 Mbyte of the 4 Gbyte address space. (Except for the interrupt controller, which has 4 Kbyte address space.) The peripheral base address is the lowest address of its memory space. The peripheral register set is composed of control, mode, data, status, and interrupt registers.

To maximize the efficiency of bit manipulation, frequently written registers are mapped into three memory locations. The first address is used to set the individual register bits, the second resets the bits, and the third address reads the value stored in the register. A bit can be set or reset by writing a “1” to the corresponding position at the appropriate address. Writing a “0” has no effect. Individual bits can thus be modified without having to use costly read-modify-write and complex bit-manipulation instructions.

All of the external signals of the on-chip peripherals are under the control of the Parallel I/O (PIO2) Controller. The PIO2 Controller can be programmed to insert an input filter on each pin or generate an interrupt on a signal change. After reset, the user must carefully program the PIO2 Controller in order to define which peripheral signals are connected with off-chip logic.

The ARM7TDMI processor operates in little-endian mode on the ATR0621P GPS Baseband. The processor's internal architecture and the ARM and Thumb instruction sets are described in the ARM7TDMI datasheet.

The ARM standard In-Circuit Emulation debug interface is supported via the JTAG/ICE port of the ATR0621P.

Features of the ROM firmware are described in software documentation available from u-blox AG, Switzerland.

3. Pin Configuration

3.1 Pinout

Figure 3-1. Pinout LFBGA100 (Top View)

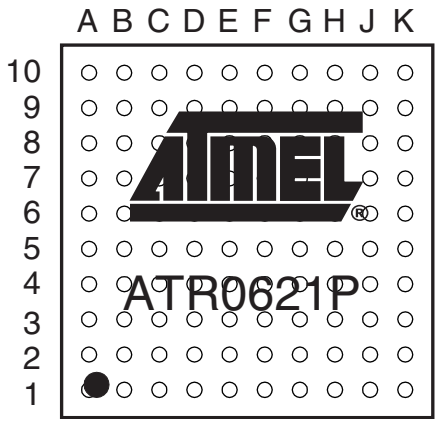


Table 3-1. ATR0621P Pinout

Pin Name	LFBGA100	Pin Type	Pull Resistor (Reset Value)(1)	Firmware Label	PIO Bank A		PIO Bank B	
CLK23	G9	IN						
DBG_EN	H4	IN	PD					
EM_A1	A6	OUT						
EM_A2	A5	OUT						
EM_A3	A4	OUT						
EM_A4	A2	OUT						
EM_A5	A3	OUT						
EM_A6	B5	OUT						
EM_A7	B4	OUT						
EM_A8	B2	OUT						
EM_A9	D4	OUT						
EM_A10	C2	OUT						
EM_A11	D6	OUT						
EM_A12	D7	OUT						
EM_A13	C3	OUT						
EM_A14	C1	OUT						
EM_A15	D5	OUT						

Notes:
1. PD = internal pull-down resistor, PU = internal pull-up resistor, OH = switched to Output High at reset
2. VBAT18 represent the internal power supply of the backup power domain, see section “Power Supply” on page 21
3. VDDIO is the supply voltage for the following GPIO pins: P1, P2, P8, P12, P14, P16, P17, P18, P19, P20, P21, P23, P24, P25, P26, P27 and P29, see section “Power Supply” on page 21
4. VDD_USB is the supply voltage for the following USB pins: USB_DM and USB_DP, see section “Power Supply” on page 21. For operation of the USB interface, supply of 3.0V to 3.6V is required.
5. This pin is not connected

Table 3-1. ATR0621P Pinout (Continued)

Pin Name	LFBGA100	Pin Type	Pull Resistor (Reset Value)[1]	Firmware Label	PIO Bank A		PIO Bank B	
EM_A16	C6	OUT						
EM_A17	F8	OUT						
EM_A18	B3	OUT						
EM_A19	C5	OUT						
EM_DA0	B6	I/O	PD					
EM_DA1	B10	I/O	PD					
EM_DA2	C7	I/O	PD					
EM_DA3	C10	I/O	PD					
EM_DA4	D10	I/O	PD					
EM_DA5	E7	I/O	PD					
EM_DA6	E9	I/O	PD					
EM_DA7	B7	I/O	PD					
EM_DA8	B8	I/O	PD					
EM_DA9	A9	I/O	PD					
EM_DA10	C8	I/O	PD					
EM_DA11	B9	I/O	PD					
EM_DA12	D8	I/O	PD					
EM_DA13	C9	I/O	PD					
EM_DA14	D9	I/O	PD					
EM_DA15	E8	I/O	PD					
GND	A1	IN						
GND	A10	IN						
GND	K1	IN						
GND	K10	IN						
LDOBAT_IN	K8	IN						
LDO_EN	H7	IN						
LDO_IN	K7	IN						
LDO_OUT	H6	OUT						
NRESET	C4	I/O	Open Drain PU					
NSHDN	G7	OUT						
NSLEEP	J6	OUT						
NTRST	K2	IN	PD					
P0	K9	I/O	PD	NANTSHORT				
P1	G3	I/O	Configurable (PD)	GPSMODE0		AGCOUT1		

Notes:
1. PD = internal pull-down resistor, PU = internal pull-up resistor, OH = switched to Output High at reset
2. VBAT18 represent the internal power supply of the backup power domain, see section "Power Supply" on page 21
3. VDDIO is the supply voltage for the following GPIO pins: P1, P2, P8, P12, P14, P16, P17, P18, P19, P20, P21, P23, P24, P25, P26, P27 and P29, see section "Power Supply" on page 21
4. VDD_USB is the supply voltage for the following USB pins: USB_DM and USB_DP, see section "Power Supply" on page 21. For operation of the USB interface, supply of 3.0V to 3.6V is required.
5. This pin is not connected

Table 3-1. ATR0621P Pinout (Continued)

Pin Name	LFBGA100	Pin Type	Pull Resistor (Reset Value)[1]	Firmware Label	PIO Bank A		PIO Bank B	
P2	G4	I/O	Configurable (PD)	BOOT_MODE		“0”		
P3	H5	I/O	OH	NCS1		NCS1		“0”
P4	A7	I/O	OH	NCS0		NCS0		“0”
P5	B1	I/O	OH	NWE/NWR0		NWE/NWR0		“0”
P6	A8	I/O	OH	NOE/NRD		NOE/NRD		“0”
P7	D2	I/O	OH	NUB/NWR1		NUB/NWR1		“0”
P8	G2	I/O	Configurable (PD)	STATUSLED		“0”		
P9	J8	I/O	PU to VBAT18	EXTINT0	EXTINT0			
P10	E4	I/O	OH	EM_A0/NLB		EM_A0/NLB		“0”
P11	H10	I/O	OH	EM_A21		NCS2		EM_A21
P12	F3	I/O	Configurable (PU)	GPSMODE2		NPCS2		
P13	G10	I/O	PU to VBAT18	GPSMODE3	EXTINT1			
P14	J5	I/O	Configurable (PD)	NAADET1		“0”		
P15	K5	I/O	PD	ANTON				
P16	E1	I/O	Configurable (PU)	NEEPROM	SIGHI1			NWD_OVF
P17	J4	I/O	Configurable (PD)	GPSMODE5	SCK1	SCK1		
P18	K4	I/O	Configurable (PU)	TXD1		TXD1		“0”
P19	F1	I/O	Configurable (PU)	GPSMODE6	SIGLO1			“0”
P20	H2	I/O	Configurable (PD)	TIMEPULSE	SCK2	SCK2		TIMEPULSE
P21	F2	I/O	Configurable (PU)	TXD2		TXD2		“0”
P22	H8	I/O	PU to VBAT18	RXD2	RXD2			
P23	H3	I/O	Configurable (PU)	GPSMODE7	SCK	SCK		MCLK_OUT
P24	H1	I/O	Configurable (PU)	GPSMODE8	MOSI	MOSI		“0”
P25	D1	I/O	Configurable (PD)	NAADET0	MISO	MISO		“0”
P26	G8	I/O	Configurable (PU)	GPSMODE10	NSS	NPCS0		“0”
P27	E2	I/O	Configurable (PU)	GPSMODE11		NPCS1		
P28	G1	I/O	OH	EM_A20		NCS3		EM_A20
P29	E3	I/O	Configurable (PU)	GPSMODE12		NPCS3		
P30	G5	I/O	PD	AGCOUT0		AGCOUT0		“0”
P31	H9	I/O	PU to VBAT18	RXD1	RXD1			
RF_ON	K6	OUT	PD					
SIGHI0	F9	IN						
SIGLO0	E10	IN						
TCK	J3	IN	PU					

Notes:
1. PD = internal pull-down resistor, PU = internal pull-up resistor, OH = switched to Output High at reset
2. VBAT18 represent the internal power supply of the backup power domain, see section “Power Supply” on page 21
3. VDDIO is the supply voltage for the following GPIO pins: P1, P2, P8, P12, P14, P16, P17, P18, P19, P20, P21, P23, P24, P25, P26, P27 and P29, see section “Power Supply” on page 21
4. VDD_USB is the supply voltage for the following USB pins: USB_DM and USB_DP, see section “Power Supply” on page 21. For operation of the USB interface, supply of 3.0V to 3.6V is required.
5. This pin is not connected

Table 3-1. ATR0621P Pinout (Continued)

Pin Name	LFBGA100	Pin Type	Pull Resistor (Reset Value)[1]	Firmware Label	PIO Bank A		PIO Bank B	
TDI	J2	IN	PU					
TDO	K3	OUT						
TMS	J1	IN	PU					
USB_DM	F10	I/O						
USB_DP	D3	I/O						
VBAT	J7	IN						
VBAT18[2]	G6	OUT						
VDD18	E6	IN						
VDD18	F7	IN						
VDD18	F6	IN						
VDDIO[3]	E5	IN						
VDD_USB[4]	F5	IN						
XT_IN	J9	IN						
XT_OUT	J10	OUT						
NC[5]	F4	-						

Notes:
1. PD = internal pull-down resistor, PU = internal pull-up resistor, OH = switched to Output High at reset
2. VBAT18 represent the internal power supply of the backup power domain, see section “Power Supply” on page 21
3. VDDIO is the supply voltage for the following GPIO pins: P1, P2, P8, P12, P14, P16, P17, P18, P19, P20, P21, P23, P24, P25, P26, P27 and P29, see section “Power Supply” on page 21
4. VDD_USB is the supply voltage for the following USB pins: USB_DM and USB_DP, see section “Power Supply” on page 21. For operation of the USB interface, supply of 3.0V to 3.6V is required.
5. This pin is not connected

3.2 Signal Description

Table 3-2. ATR0621P Signal Description

Module	Name	Function	Type	Active Level	Comment
EBI	EM_A0 to EM_A21	External memory address bus	Output	–	All valid after reset
	EM_DA0 to EM_DA15	External memory data bus	I/O	–	Internal pull-down resistor
	NCS0 to NCS1	Chip select	Output	Low	Output high in RESET state
	NCS2 to NCS3	Chip select	Output	Low	Output high in RESET state
	NWR0	Lower byte write signal	Output	Low	Output high in RESET state
	NWR1	Upper byte write signal	Output	Low	Output high in RESET state
	NRD	Read signal	Output	Low	Output high in RESET state
	NWE	Write enable	Output	Low	Output high in RESET state
	NOE	Output enable	Output	Low	Output high in RESET state
	NUB	Upper byte select (16-bit SRAM)	Output	Low	Output high in RESET state
	NLB	Lower byte select (16-bit SRAM)	Output	Low	Output high in RESET state
	BOOT_MODE	Boot mode input	Input	–	PIO-controlled after reset, internal pull-down resistor
USART	TXD1-2	Transmit data output	Output	–	PIO-controlled after reset
	RXD1-2	Receive data input	Input	–	PIO-controlled after reset
	SCK1-2	External synchronous serial clock	I/O	–	PIO-controlled after reset
USB	USB_DP	USB data (D+)	I/O	–	
	USB_DM	USB data (D-)	I/O	–	
APMC	RF_ON		Output	–	Interface to ATR0601
AIC	EXTINT0-1	External interrupt request	Input	High/ Low/ Edge	PIO-controlled after reset
AGC	AGCOUT0-1	Automatic gain control	Output	–	Interface to ATR0601 PIO-controlled after reset
RTC	NSLEEP	Sleep output	Output	Low	Interface to ATR0601
	NSHDN	Shutdown output	Output	Low	Connect to pin LDO_EN
	XT_IN	Oscillator input	Input	–	RTC oscillator
	XT_OUT	Oscillator output	Output	–	RTC oscillator
SPI	SCK	SPI clock	I/O	–	PIO-controlled after reset
	MOSI	Master out slave in	I/O	–	PIO-controlled after reset
	MISO	Master in slave out	I/O	–	PIO-controlled after reset
	NSS/NPCS0	Slave select	I/O	Low	PIO-controlled after reset
	NPCS1-3	Slave select	Output	Low	PIO-controlled after reset
WD	NWD_OVF	Watchdog timer overflow	Output	–	PIO-controlled after reset
PIO	P0-31	Programmable I/O port	I/O	–	Input after reset (except P3 to P7, P10, P11, P28)

Note: 1. The USB transceiver is disabled if VDD_USB < 2.0V. In this case the pins USB_DM and USB_DP are connected to GND (internal pull-down resistors). The USB transceiver is enabled if VDD_USB is within 3.0V and 3.6V.

Table 3-2. ATR0621P Signal Description (Continued)

Module	Name	Function	Type	Active Level	Comment
GPS	SIGHI0	Digital IF	Input	–	Interface to ATR0601
	SIGLO0	Digital IF	Input	–	Interface to ATR0601
	SIGHI1	Digital IF	Input	–	PIO-controlled after reset
	SIGLO1	Digital IF	Input	–	PIO-controlled after reset
	TIMEPULSE	GPS synchronized time pulse	Output	–	PIO-controlled after reset
CONFIG	GPSMODE0-12	GPS mode	Input	–	PIO-controlled after reset
	STATUSLED	Status LED	Output	–	PIO-controlled after reset
	NEEPROM	Enable EEPROM support	Input	Low	PIO-controlled after reset
	ANTON	Active antenna power on output	Output	–	PIO-controlled after reset
	NANTSHORT	Active antenna short circuit detection Input	Input	Low	PIO-controlled after reset
	NAADET0-1	Active antenna detection input	Input	Low	PIO-controlled after reset
JTAG/ICE	TMS	Test mode select	Input	–	Internal pull-up resistor
	TDI	Test data in	Input	–	Internal pull-up resistor
	TDO	Test data out	Output	–	Output high in RESET state
	TCK	Test clock	Input	–	Internal pull-up resistor
	NTRST	Test reset input	Input	Low	Internal pull-down resistor
	DBG_EN	Debug enable	Input	High	Internal pull-down resistor
CLOCK	CLK23	Clock input	Input	–	Interface to ATR0601, Schmitt trigger input
	MCLK_OUT	Master clock output	Output	–	PIO-controlled after reset
RESET	NRESET	Reset input	I/O	Low	Open drain with internal pull-up resistor
POWER	VDD18		Power	–	Core voltage 1.8V
	VDDIO		Power	–	Variable I/O voltage 1.65V to 3.6V
	VDD_USB		Power	–	USB voltage 0 to 2.0V or 3.0Vto 3.6V(1)
	GND		Power	–	Ground
LDOBAT	LDOBAT_IN		Power	–	2.3V to 3.6V
	VBAT		Power	–	1.5V to 3.6V
	VBAT18		Out	–	1.8V backup voltage
LDO18	LDO_IN	LDO in	Power	–	2.3V to 3.6V
	LDO_OUT	LDO out	Power	–	1.8V core voltage, maximum 80 mA
	LDO_EN	LDO enable	Input	–	

Note: 1. The USB transceiver is disabled if VDD_USB < 2.0V. In this case the pins USB_DM and USB_DP are connected to GND (internal pull-down resistors). The USB transceiver is enabled if VDD_USB is within 3.0V and 3.6V.

3.3 Setting GPSMODE0 to GPSMODE12

The start-up configuration of a ROM-based system without external non-volatile memory is defined by the status of the GPSMODE pins after system reset. Alternatively, the system can be configured through message commands passed through the serial interface after start-up. This configuration of the ATR0621P can be stored in an external non-volatile memory like FLASH memory or EEPROM. *Default* designates settings used by ROM firmware if GPSMODE configuration is disabled (GPSMODE0 =0).

Table 3-3. GPSMODE Functions

Pin	Function
GPSMODE0 (P1)	Enable configuration with GPSMODE pins
GPSMODE1 (P9)	This pin (EXTINT0) is used for FixNow™ functionality and not used for GPSMODE configuration
GPSMODE2 (P12)	GPS sensitivity settings
GPSMODE3 (P13)	
GPSMODE4 (P14)	This pin (NAADET1) is used as active antenna supervisor input and not used for GPSMODE configuration. This is the default selection if GPSMODE configuration is disabled.
GPSMODE5 (P17)	Serial I/O configuration
GPSMODE6 (P19)	
GPSMODE7 (P23)	USB power mode
GPSMODE8 (P24)	General I/O configuration
GPSMODE9 (P25)	This pin (NAADET0) is used as active antenna supervisor input and not used for GPSMODE configuration
GPSMODE10 (P26)	General I/O configuration
GPSMODE11 (P27)	
GPSMODE12 (P29)	Serial I/O configuration

In the case that GPSMODE pins with internal pull-up or pull-down resistors are connected to GND/VDD18, additional current is drawn over these resistors. Especially GPSMODE3 can impact the back-up current.

3.3.1 Enable GPSMODE Pin Configuration

Table 3-4. Enable Configuration with GPSMODE Pins

GPSMODE0 (Reset = PD)	Description
0(1)	Ignore all GPSMODE pins. The default settings as indicated below are used.
1	Use settings as specified with GPSMODE[2, 3, 5 to 8, 10 to 12]

Note: 1. Leave open

If the GPSMODE configuration is enabled (GPSMODE0 = 1) and the other GPSMODE pins are not connected externally, the reset default values of the internal pull-down and pull-up resistors will be used.

3.3.2 Sensitivity Settings

Table 3-5. GPS Sensitivity Settings

GPSMODE3 (Fixed PU)	GPSMODE2 (Reset = PU)	Description
0[1]	0	Auto mode
0[1]	1[2]	Fast mode
1[2]	0	Normal mode (Default ROM value)
1[2]	1[2]	High sensitivity

Notes: 1. Increased back-up current
2. Leave open

For all GPS receivers the sensitivity depends on the integration time of the GPS signals. Therefore there is a trade-off between sensitivity and the time to detect the GPS signal (Time to first fix). The three modes, “Fast Acquisition”, “Normal” and “High Sensitivity”, have a fixed integration time. The “Normal” mode, recommended for the most applications, is a trade off between the sensitivity and TTFF. The “Fast Acquisition” mode is optimized for fast acquisition, at the cost of a lower sensitivity. The “High Sensitivity” mode is optimized for higher sensitivity, at the cost of longer TTFF. The “Auto” mode adjusts the integration time (sensitivity) automatically according to the measured signal levels. That means the receiver with this setting has a fast TTFF at strong signals, a high sensitivity to acquire weak signals but some times at medium signal level a higher TTFF as the “Normal” mode. These sensitivity settings affect only the startup performance not the tracking performance.

3.3.3 Serial I/O Configuration

The ATR0621P features a two-stage I/O message and protocol selection procedure for the two available serial ports. At the first stage, a certain protocol can be enabled or disabled for a given USART port or the USB port. Selectable protocols are RTCM, NMEA and UBX. At the second stage, messages can be enabled or disabled for each enabled protocol on each port. In all configurations discussed below, all protocols are enabled on all ports. But output messages are enabled in a way that ports appear to communicate at only one protocol. However, each port will accept any input message in any of the three implemented protocols.

Table 3-6. Serial I/O Configuration

GPSMODE12 (Reset = PU)	GPSMODE6 (Reset = PU)	GPSMODE5 (Reset = PD)	USART1/USB (Output Protocol/ Baud Rate (kBaud))	USART2 (Output Protocol/ Baud Rate (kBaud))	Messages[1]	Information Messages
0	0	0[2]	UBX/57.6	NMEA/19.2	High	User, Notice, Warning, Error
0	0	1	UBX/38.4	NMEA/9.6	Medium	User, Notice, Warning, Error
0	1[2]	0[2]	UBX/19.2	NMEA/4.8	Low	User, Notice, Warning, Error
0	1[2]	1	–/Auto	–/Auto	Off	None
1[2]	0	0[2]	NMEA/19.2	UBX/57.6	High	User, Notice, Warning, Error
1[2]	0	1	NMEA/4.8	UBX/19.2	Low	User, Notice, Warning, Error
1[2]	1[2]	0[2]	NMEA/9.6	UBX/38.4	Medium	User, Notice, Warning, Error
1[2]	1[2]	1	UBX/115.2	NMEA/19.2	Debug	All

Notes: 1. See Table 3-7 to Table 3-10 on page 13, the messages are described in the ANTARIS4 protocol specification
2. Leave open

Both USART ports and the USB port accept input messages in all three supported protocols (NMEA, RTCM and UBX) at the configured baud rate. Input messages of all three protocols can be arbitrarily mixed. Response to a query input message will always use the same protocol as the query input message. The USB port does only accept NMEA and UBX as input protocol by default. RTCM can be enabled via protocol messages on demand.

In Auto Mode, no output message is sent out by default, but all input messages are accepted at any supported baud rate. Again, USB is restricted to only NMEA and UBX protocols. Response to query input commands will be given the same protocol and baud rate as it was used for the query command. Using the respective configuration commands, periodic output messages can be enabled.

The following message settings are used in the tables below:

Table 3-7. Supported Messages at Setting *Low*

NMEA Port	Standard	GGA, RMC
UBX Port	NAV	SOL, SVINFO
	MON	EXCEPT

Table 3-8. Supported Messages at Setting *Medium*

NMEA Port	Standard	GGA, RMC, GSA, GSV, GLL, VTG, ZDA
UBX Port	NAV	SOL, SVINFO, POSECEF, POSLLH, STATUS, DOP, VELECEF, VELNED, TIMEGPS, TIMEUTC, CLOCK
	MON	EXCEPT

Table 3-9. Supported Messages at Setting *High*

NMEA Port	Standard	GGA, RMC, GSA, GSV, GLL, VTG, ZDA, GRS, GST
	Proprietary	PUBX00, PUBX03, PUBX04
UBX Port	NAV	SOL, SVINFO, POSECEF, POSLLH, STATUS, DOP, VELECEF, VELNED, TIMEGPS, TIMEUTC, CLOCK
	MON	SCHD, IO, IPC, EXCEPT

Table 3-10. Supported Messages at Setting *Debug* (Additional Undocumented Message May be Part of Output Data)

NMEA Port	Standard	GGA, RMC, GSA, GSV, GLL, VTG, ZDA, GRS, GST
	Proprietary	PUBX00, PUBX03, PUBX04
UBX Port	NAV	SOL, SVINFO, POSECEF, POSLLH, STATUS, DOP, VELECEF, VELNED, TIMEGPS, TIMEUTC, CLOCK
	MON	SCHD, IO, IPC, EXCEPT
	RXM	RAW (RAW message support requires an additional license)

The following settings apply if GPSMODE configuration is not enabled, that is, GPSMODE = 0 (*ROM-Defaults*):

Table 3-11. Serial I/O Default Setting if GPSMODE Configuration is Deselected (GPSMODE0 = 0)

	USB NMEA	**USART1 NMEA**	**USART2 UBX**
Baud rate (kBaud)		57.6	57.6
Input protocol	UBX, NMEA	UBX, NMEA, RTCM	UBX, NMEA, RTCM
Output protocol	NMEA	NMEA	UBX
Messages	GGA, RMC, GSA, GSV	GGA, RMC, GSA, GSV	NAV: SOL, SVINFO MON: EXCEPT
Information messages (UBX INF or NMEA TXT)	User Notice, Warning, Error	User, Notice, Warning, Error	User, Notice, Warning, Error

3.3.4 USB Power Mode

For correct response to the USB host queries, the device has to know its power mode. This is configured via GPSMODE7. If set to *bus powered*, an upper current limit of 100 mA is reported to the USB host; that is, the device classifies itself as a “low-power bus-powered function” with no more than one USB power unit load.

Table 3-12. USB Power Modes

GPSMODE7 (Reset = PU)	**Description**
0	USB device is bus-powered (maximum current limit 100 mA)
1[1]	USB device is self-powered (default ROM value)

Note: 1. Leave open

3.3.5 Active Antenna Supervisor

The two pins P0/NANTSHORT and P15/ANTON plus one pin of P25/NAADET0/MISO or P14/NAADET1 are always initialized as general purpose I/Os and used as follows:

- P15/ANTON is an output which can be used to switch on and off antenna power supply.
- Input P0/NANTSHORT will indicate an antenna short circuit, i.e. zero DC voltage at the antenna, to the firmware. If the antenna is switched off by output P15/ANTON, it is assumed that also input P0/NANTSHORT will signal zero DC voltage, i.e. switch to its active low state.
- Input P25/NAADET0/MISO or P14/NAADET1 will indicate a DC current into the antenna. In case of short circuit, both P0 and P25/P14 will be active, i.e. at low level. If the antenna is switched off by output P15/ANTON, it is assumed that also input P25/NAADET0/MISO will signal zero DC current, i.e. switch to its active low state. Which pin is used as NAADET (P14 or P25) depends on the settings of GPSMODE11 and GPSMODE10 (see Table 3-14 on page 15).

Table 3-13. Pin Usage of Active Antenna Supervisor

Pin	Usage	Meaning
P0/NANTSHORT	NANTSHORT	Active antenna short circuit detection High = No antenna DC short circuit present Low = Antenna DC short circuit present
P25/NAADET0/ MISO or P14/NAADET1	NAADET	Active antenna detection input High = No active antenna present Low = Active antenna is present
P15/ANTON	ANTON	Active antenna power on output High = Power supply to active antenna is switched on Low = Power supply to active antenna is switched off

Table 3-14. Antenna Detection I/O Settings

GPSMODE11 (Reset = PU)	GPSMODE10 (Reset = PU)	GPSMODE8 (Reset = PU)	Location of NAADET	Comment
0	0	0	P25/NAADET0/MISO	
0	0	1(1)	P25/NAADET0/MISO	
0	1(1)	0	P14/NAADET1	Reserved for further use. Do not use this setting.
0	1(1)	1(1)	P14/NAADET1 (Default ROM value)	
1(1)	0	0	P14/NAADET1	Reserved for further use. Do not use this setting.
1(1)	0	1(1)	P14/NAADET1	Reserved for further use. Do not use this setting.
1(1)	1(1)	0	P25/NAADET0/MISO	
1(1)	1(1)	1(1)	P25/NAADET0/MISO	

Note: 1. Leave open

The Antenna Supervisor Software will be configured as follows:

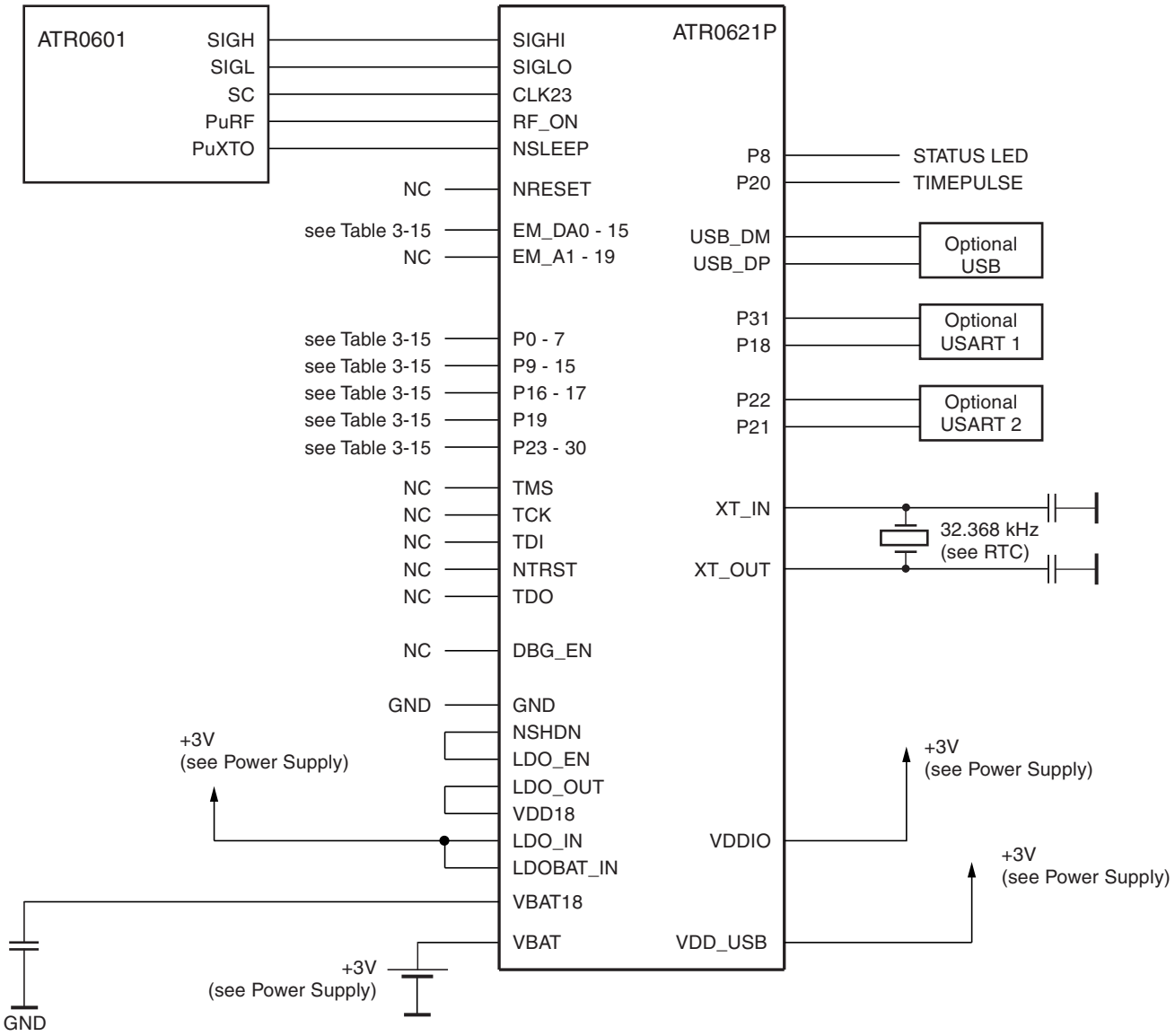
1. Enable Control Signal
2. Enable Short Circuit Detection (power down antenna via ANTON if short is detected via NANTSHORT)
3. Enable Open Circuit Detection via NAADET

The antenna supervisor function may not be disabled by GPSMODE pin selection.

If the antenna supervisor function is not used, please leave open ANTON, NANTSHORT and NAADET.

3.4 External Connections for a Working GPS System

Figure 3-2. Example of an External Connection



NC: Not connected

Table 3-15. Recommended Pin Connection

Pin Name	Recommended External Circuit
P0/NANTSHORT	Internal pull-down resistor, leave open if Antenna Supervision functionality is unused.
P1/GPSMODE0	Internal pull-down resistor, leave open, in order to disable the GPSMODE pin configuration feature. Connect to VDD18 to enable the GPSMODE pin configuration feature. Refer to GPSMODE definitions in section "Setting GPSMODE0 to GPSMODE12" on page 11. Can be left open if configured as output by user application.
P2/BOOT_MODE	Internal pull-down resistor, leave open.
P3/NCS1	Output in default ROM firmware: leave open, only needs pull-up resistor to VDD18 or pull-down resistor to GND if used as GPIO input by user application and is not always driven from external sources.
P4/NCS0	Output in default ROM firmware: leave open, only needs pull-up resistor to VDD18 or pull-down resistor to GND if used as GPIO input by user application and is not always driven from external sources.
P5/NWE/NWR0	Output in default ROM firmware: leave open, only needs pull-up resistor to VDD18 or pull-down resistor to GND if used as GPIO input by user application and is not always driven from external sources.
P6/NOE/NRD	Output in default ROM firmware: leave open, only needs pull-up resistor to VDD18 or pull-down resistor to GND if used as GPIO input by user application and is not always driven from external sources.
P7/NUB/NWR1	Output in default ROM firmware: leave open, only needs pull-up resistor to VDD18 or pull-down resistor to GND if used as GPIO input by user application and is not always driven from external sources.
P8/STATUSLED	Output in default ROM firmware: leave open, only needs pull-up resistor to VDD18 or pull-down resistor to GND if used as GPIO input by user application and is not always driven from external sources.
P9/EXTINT0	Internal pull-up resistor, leave open if unused.
P10/EM_A0/NLB	Output in default ROM firmware: leave open, only needs pull-up resistor to VDD18 or pull-down resistor to GND if used as GPIO input by user application and is not always driven from external sources.
P11/EM_A21/NCS2	Output in default ROM firmware: leave open, only needs pull-up resistor to VDD18 or pull-down resistor to GND if used as GPIO input by user application and is not always driven from external sources.
P12/GPSMODE2/NPCS2	Internal pull-up resistor, can be left open if the GPSMODE feature is not used or configured as output by user application. Refer to GPSMODE definitions in section "Setting GPSMODE0 to GPSMODE12" on page 11.
P13/GPSMODE3/EXTINT1	Internal pull-up resistor, can be left open if the GPSMODE feature is not used or configured as output by user application. Refer to GPSMODE definitions in section "Setting GPSMODE0 to GPSMODE12" on page 11.
P14/NAADET1	Internal pull-down resistor, leave open if Antenna Supervision functionality is unused.
P15/ANTON	Internal pull-down resistor, leave open if Antenna Supervision functionality is unused.
P16/NEEPROM	Internal pull-up resistor, leave open if no serial EEPROM is connected. Otherwise connect to GND.
P17/GPSMODE5/SCK1	Internal pull-down resistor, can be left open if the GPSMODE feature is not used or configured as output by user application. Refer to GPSMODE definitions in section "Setting GPSMODE0 to GPSMODE12" on page 11.
P18/TXD1	Output in default ROM firmware: leave open if serial interface is not used.
P19/GPSMODE6/SIGLO1	Internal pull-up resistor, can be left open if the GPSMODE feature is not used or configured as output by user application. Refer to GPSMODE definitions in section "Setting GPSMODE0 to GPSMODE12" on page 11.
P20/TIMEPULSE/SCK2	Output in default ROM firmware: leave open if timepulse feature is not used.
P21/TXD2	Output in default ROM firmware: leave open if serial interface not used.
P22/RXD2	Internal pull-up resistor, leave open if serial interface is not used.
P23/GPSMODE7/SCK	Internal pull-up resistor, can be left open if the GPSMODE feature is not used or configured as output by user application. Refer to GPSMODE definitions in section "Setting GPSMODE0 to GPSMODE12" on page 11.

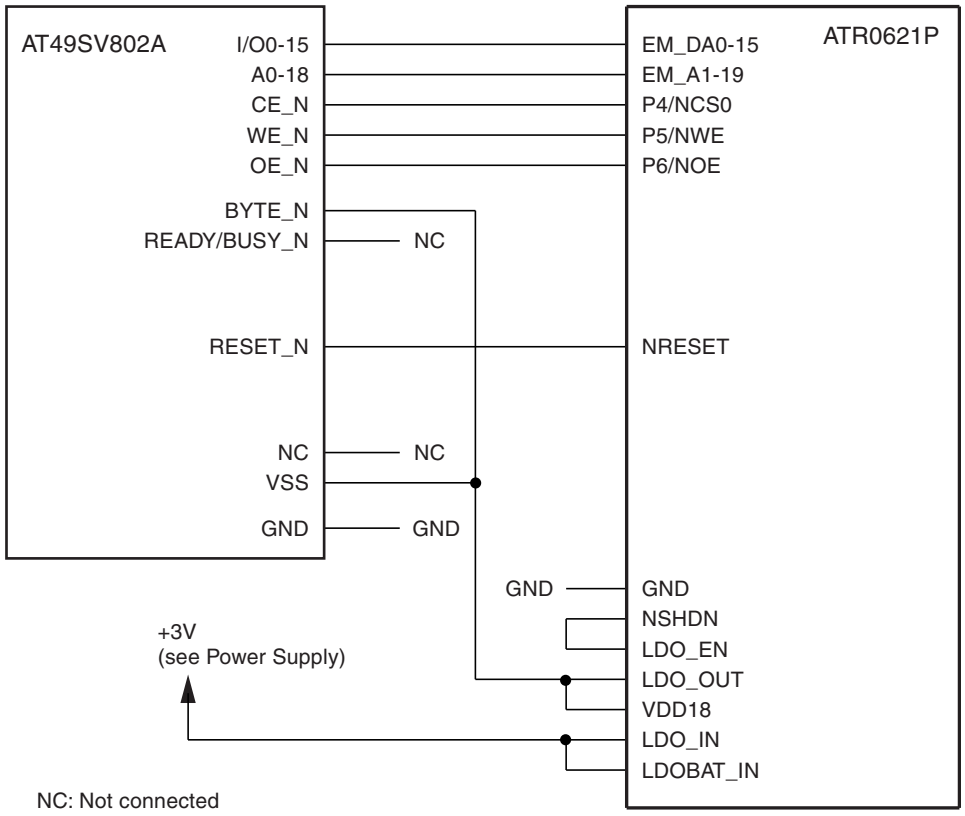
Table 3-15. Recommended Pin Connection (Continued)

Pin Name	Recommended External Circuit
P24/GPSMODE8/MOSI	Internal pull-up resistor, can be left open if the GPSMODE feature is not used or configured as output by user application. Refer to GPSMODE definitions in section "Setting GPSMODE0 to GPSMODE12" on page 11.
P25/NAADET0/MISO	Internal pull-down resistor, leave open if Antenna Supervision functionality is unused. Can be left open if configured as output by user application.
P26/GPSMODE10/NSS/ NPCS0	Internal pull-up resistor, can be left open if the GPSMODE feature is not used or configured as output by user application. Refer to GPSMODE definitions in section "Setting GPSMODE0 to GPSMODE12" on page 11.
P27/GPSMODE11/NPCS1	Internal pull-up resistor, can be left open if the GPSMODE feature is not used or configured as output by user application. Refer to GPSMODE definitions in section "Setting GPSMODE0 to GPSMODE12" on page 11.
P28/EM_A20/NCS3	Output in default ROM firmware: leave open, only needs pull-up resistor to VDD18 or pull-down resistor to GND if used as GPIO input by user application and is not always driven from external sources.
P29/GPSMODE12/NPCS3	Internal pull-up resistor, can be left open if the GPSMODE feature is not used or configured as output by user application. Refer to GPSMODE definitions in section "Setting GPSMODE0 to GPSMODE12" on page 11.
P30/AGCOUT0	Internal pull-down resistor, leave open.
P31/RXD1	Internal pull-up resistor, leave open if serial interface is not used.
EM_DA0 – EM_DA15	If no external memory is used, could be leave open (internal pull-down).

3.4.1 Connecting an Optional FLASH Memory

The ATR0621P offers the possibility to connect an external FLASH memory. The high performance ARM7™ 32-bit RISC processor of the ATR0621P can be used to run application specific code, that is stored in the FLASH memory. The 32-bit RISC processor of the ATR0621 accesses the external memory via the EBI (External Bus Interface). Atmel recommends to use 1.8V FLASH memory, e.g. the Atmel AT49SV802A. The LDO_OUT pin of the ATR0621P can supply the external FLASH memory. Figure 3-3 shows an example of the external FLASH memory connection.

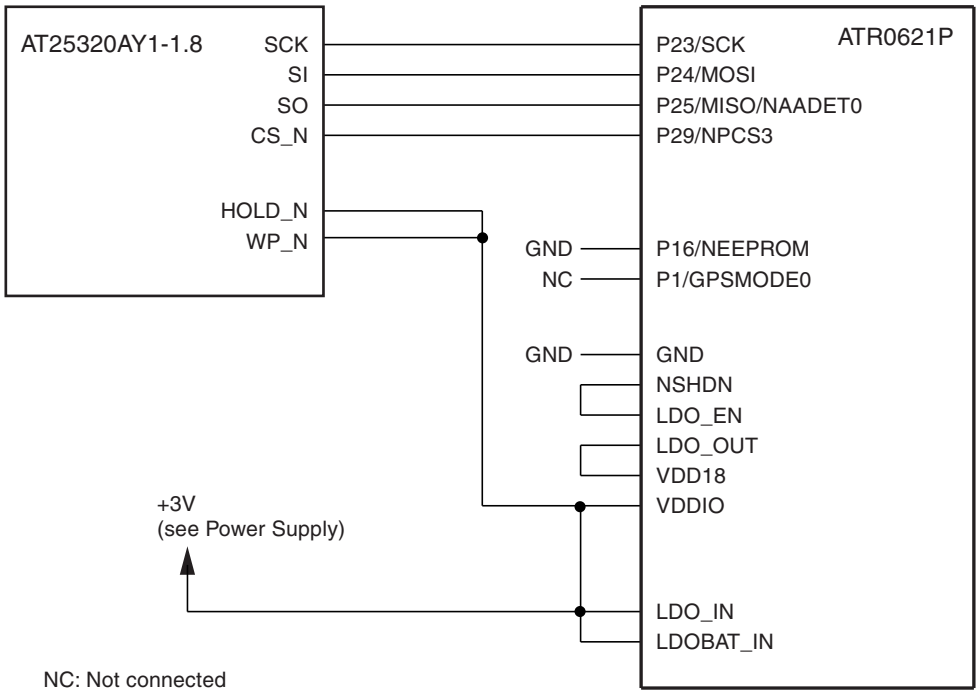
Figure 3-3. Example of an External FLASH Memory Connection



3.4.2 Connecting an Optional Serial EEPROM

The ATR0621P offers the possibility to connect an external serial EEPROM. The internal ROM firmware supports to store the configuration of the ATR0621P in serial EEPROM. The pin P16/NEEPROM signals the firmware that a serial EEPROM is connected with the ATR0621P. The 32-bit RISC processor of the ATR0621P accesses the external memory with SPI (Serial Peripheral Interface). Atmel recommends to use 32 Kbit 1.8V serial EEPROM, e.g. the Atmel AT25320AY1-1.8. Figure 3-4 shows an example of the serial EEPROM connection.

Figure 3-4. Example of a Serial EEPROM Connection



Note: The GPSMODE pin configuration feature can be disabled, because the configuration can be stored in the serial EEPROM. VDDIO is the supply voltage for the pins: P23, P24, P25 and P29.

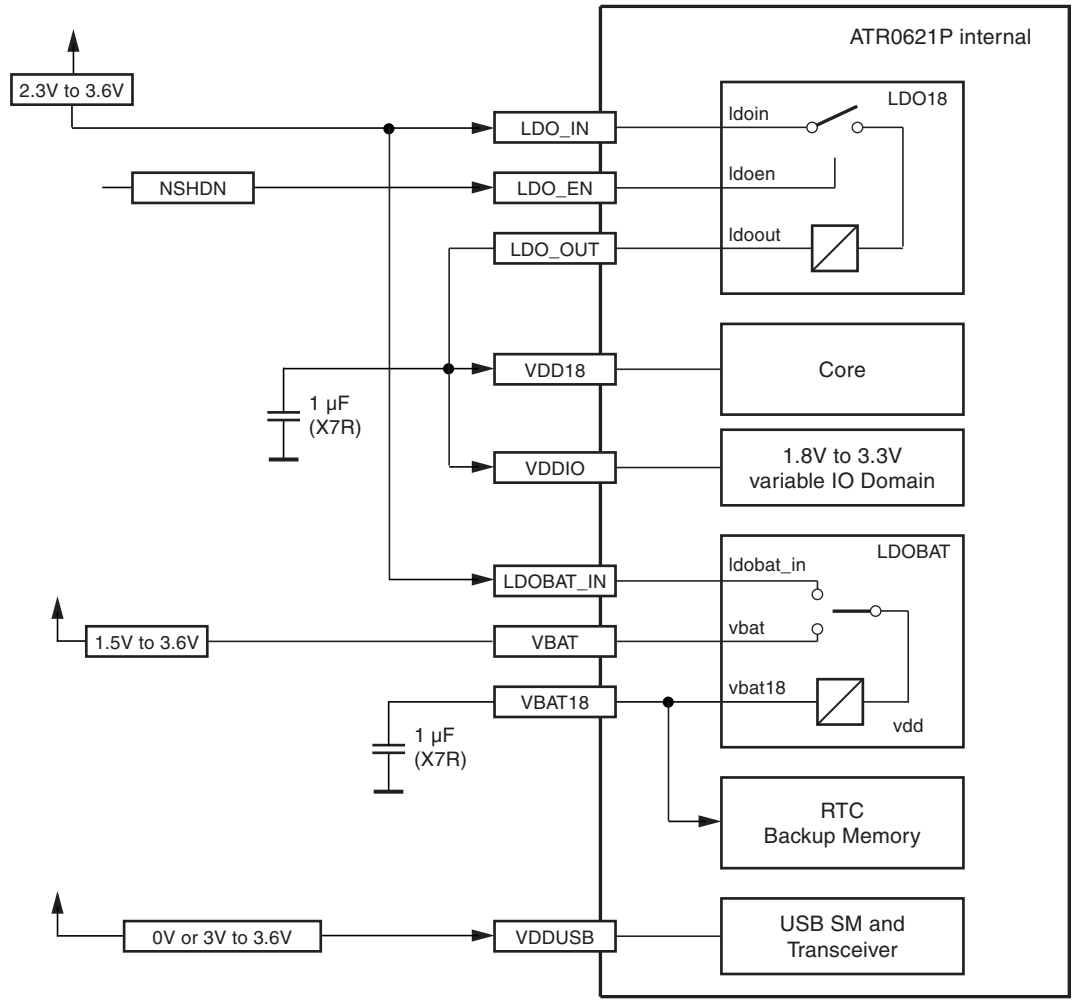
4. Power Supply

The baseband IC is supplied with four distinct supply voltages:

- VDD18, the nominal 1.8V supply voltage for the core, the RF-I/O pins, the memory interface and the test pins and all GPIO-pins not mentioned in next item.
- VDDIO, the variable supply voltage within 1.8V to 3.6V for following GPIO-pins: P1, P2, P8, P12, P14, P16, P17, P18, P19, P20, P21, P23, P24, P25, P26, P27 and P29. In input mode, these pins are 5V input tolerant.
- VDD_USB, the power supply of the USB pins: USB_DM and USB_DP.
- VBAT18 to supply the backup domain: RTC, backup SRAM and the pins NSLEEP, NSHDN, LDO_EN, VBAT18, P9/EXTIN0, P13/EXTINT1, P22/RXD2 and P31/RXD1 and the 32kHz oscillator. In input mode, the four GPIO-pins are 5V input tolerant.

Figure 4-1, Figure 4-2 and Figure 4-3 show examples of the wiring of ATR0621 power supply.

Figure 4-1. External Wiring Example Using Internal LDOs and Backup Power Supply



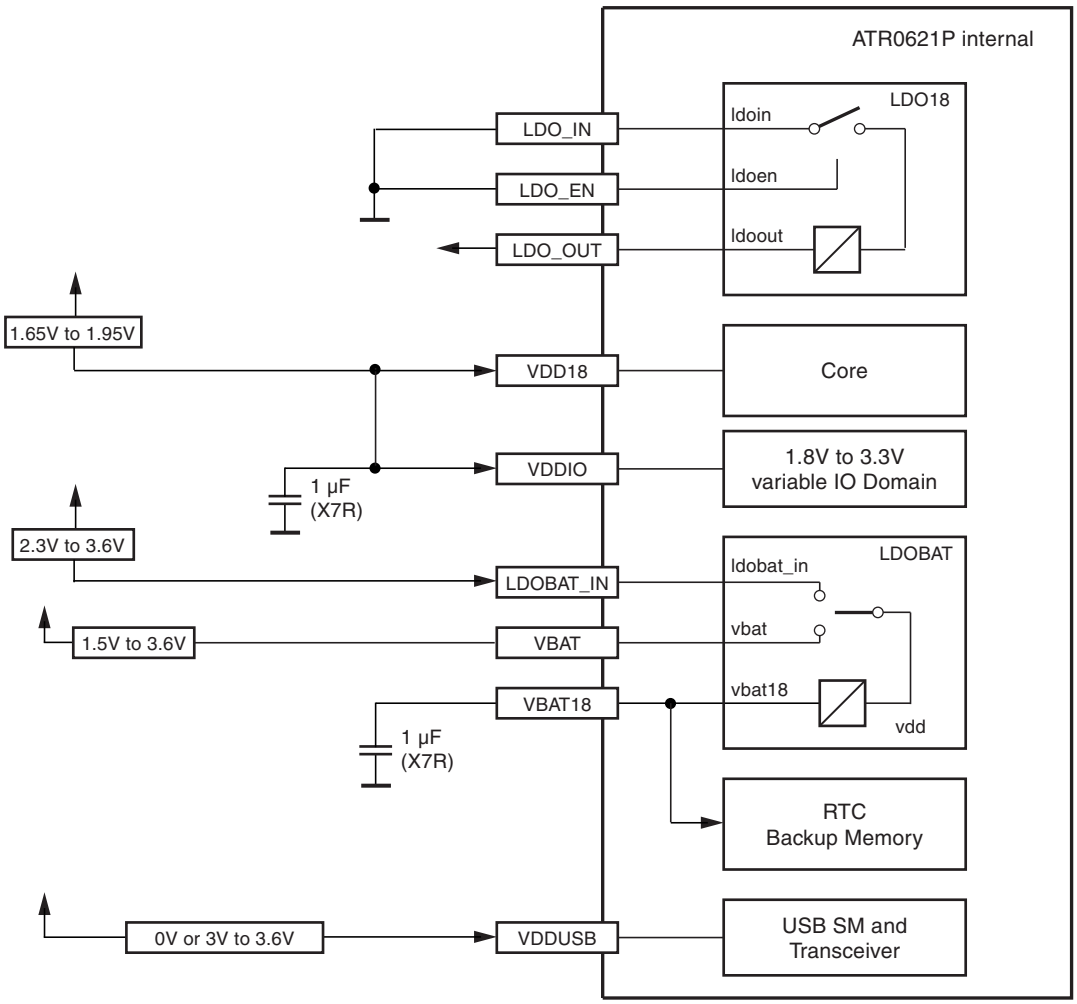
The baseband IC contains a built in low dropout voltage regulator LDO18. This regulator can be used if the host system does not provide the core voltage VDD18 of 1.8V nominal. In such case, LDO18 will provide a 1.8V supply voltage from any input voltage VDD between 2.3V and 3.6V. It will also allow supplying external components such as FLASH memory with 1.8V. The LDO_EN input can be used to shut down VDD18 if the system is in standby mode.

If the host system does however supply a 1.8V core voltage directly, this voltage has to be connected to the VDD18 supply pins of the baseband IC. LDO_EN must be connected to GND. LDO_IN can be connected to GND. LDO_OUT must not be connected.

A second built in low dropout voltage regulator LDOBAT provides the supply voltage for the RTC and backup SRAM from any input voltage VBAT between 1.5V and 3.6V. The backup battery is only discharged if VDD - supplied via pin LDOBAT_IN - is shut down.

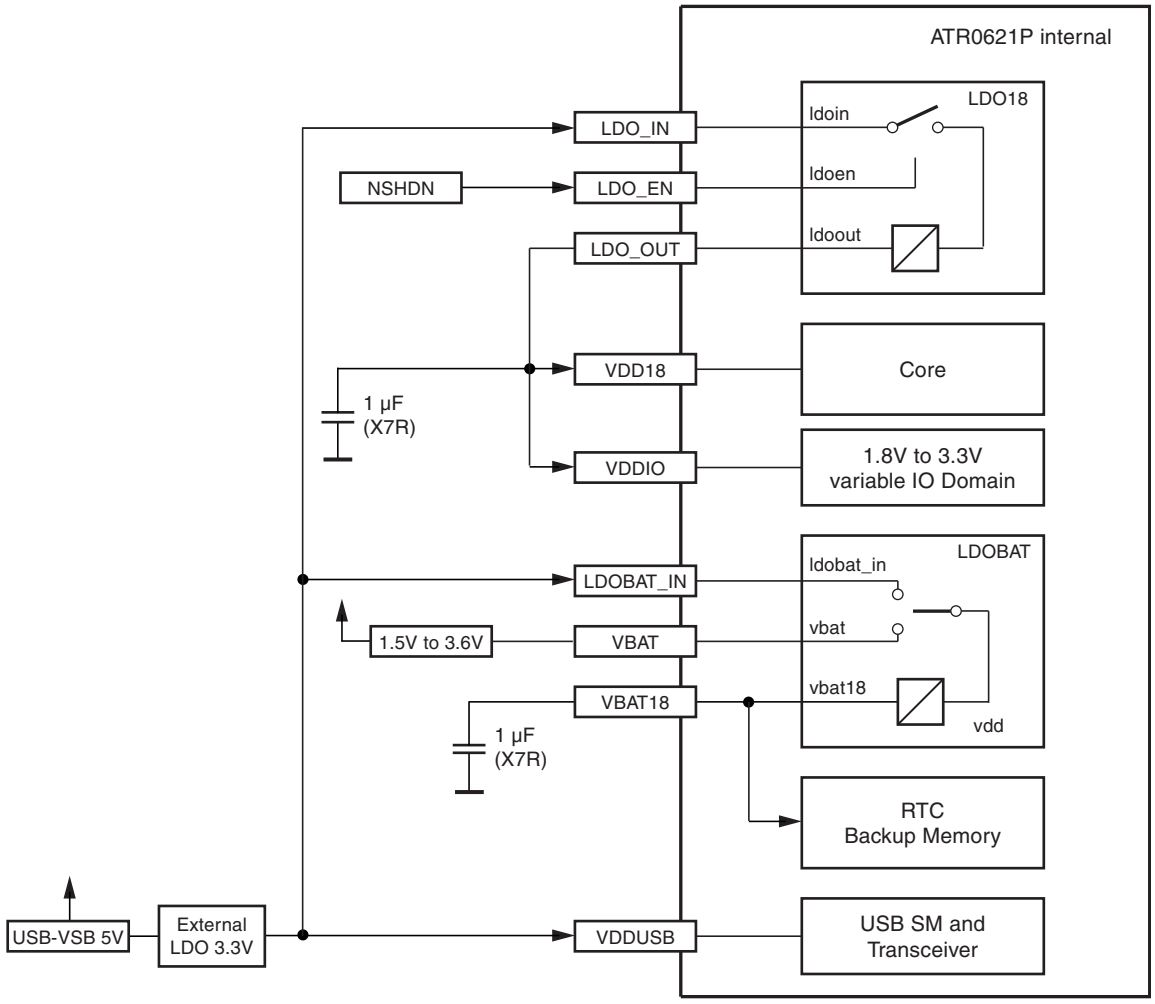
Only after VDD18 has been supplied to ATR0621 the RTC section will be initialized properly. If only VBAT is applied first, the current consumption of the RTC and backup SRAM is undetermined.

Figure 4-2. External Wiring Example Using 1.8V from Host System and Backup Power Supply



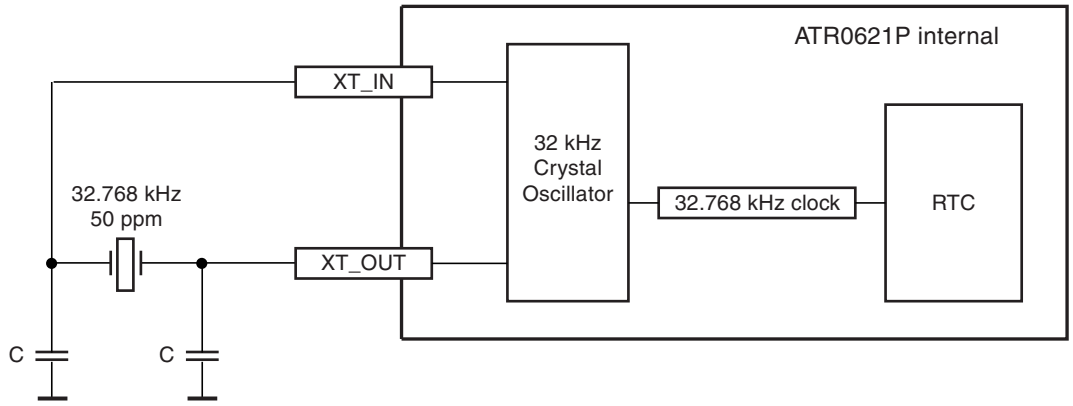
The USB Transceiver is disabled if VDD_USB < 2.0V. In this case the pins USB_DM and USB_DP are connected to GND (internal pull-down resistors). The USB Transceiver is enabled if VDD_USB within 3.0V and 3.6V.

Figure 4-3. External Wiring Example Using Internal LDOs, USB Supply Voltage and Backup Power Supply



5. RTC Oscillator

Figure 5-1. Crystal Connection



$C = 2 \times C_{load}$, C_{load} can be derived from the crystal datasheet. Maximum value for C is 25 pF.

6. Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Parameters	Pin	Symbol	Min.	Max.	Unit
Operating free air temperature range			–40	+85	°C
Storage temperature			–60	+150	°C
DC supply voltage	VDD18		–0.3	+1.95	V
	VDDIO		–0.3	+3.6	V
	VDD_USB		–0.3	+3.6	V
	LDO_IN		–0.3	+3.6	V
	LDOBAT_IN		–0.3	+3.6	V
	VBAT		–0.3	+3.6	V
DC input voltage	EM_DA0 to EM_DA15, P0, P3 to P7, P10, P11, P15, P28, P30, SIGHI, SIGLO, CLK23, XT_IN, TMS, TCK, TDI, NTRST, DBG_EN, LDO_EN, NRESET		–0.3	+1.95	V
	USB_DM, USB_DP		–0.3	+3.6	V
	P1, P2, P8, P9, P12 to P14, P16 to P27, P29, P31		–0.3	+5.0	V

Note: Minimum/maximum limits are at +25°C ambient temperature, unless otherwise specified

7. Thermal Resistance

Parameters	Symbol	Value	Unit
Junction ambient, according to JEDEC51-9	R_{thJA}	36.9	K/W

8. Electrical Characteristics - DC Characteristics

If no additional information is given in column Test Conditions, the values apply to a temperature range from –40°C to +85°C.

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
1.1	DC supply voltage core		VDD18	VDD18	1.65	1.8	1.95	V	D
1.2	DC supply voltage VDDIO domain(1)		VDDIO	VDDIO	1.65	1.8/3.3	3.6	V	D
1.3	DC supply voltage USB(2)		VDD_USB	VDDUSB	3.0	3.3	3.6	V	D
1.4	DC supply voltage backup domain(3)		VBAT18	VBAT18	1.65	1.8	1.95	V	D
1.5	DC output voltage VDD18			$V_{O,18}$	0		VDD18	V	D
1.6	DC output voltage VDDIO			$V_{O,IO}$	0		VDDIO	V	D
1.7	Low-level input voltage VDD18 domain	VDD18 = 1.65V to 1.95V		$V_{IL,18}$	–0.3		0.3 × VDD18	V	C
1.8	High-level input voltage VDD18 domain	VDD18 = 1.65V to 1.95V		$V_{IH,18}$	0.7 × VDD18		VDD18 + 0.3	V	C
1.9	Schmitt trigger threshold rising	VDD18 = 1.65V to 1.95V	CLK23	$V_{th+,CLK23}$			0.7 × VDD18	V	C
1.10	Schmitt trigger threshold falling	VDD18 = 1.65V to 1.95V	CLK23	$V_{th-,CLK23}$	0.3 × VDD18			V	C
1.11	Schmitt trigger hysteresis	VDD18 = 1.65V to 1.95V	CLK23	$V_{hyst,CLK23}$	0.2		0.55	V	C
1.12	Schmitt trigger threshold rising	VDD18 = 1.65V to 1.95V	NRESET	$V_{th+,NRESET}$	0.8		1.3	V	C
1.13	Schmitt trigger threshold falling	VDD18 = 1.65V to 1.95V	NRESET	$V_{th-,NRESET}$	0.46		0.77	V	C
1.14	Low-level input voltage VDDIO domain	VDDIO = 1.65V to 3.6V		$V_{IL,IO}$	–0.3		+0.41	V	C
1.15	High-level input voltage VDDIO domain	VDDIO = 1.65V to 3.6V		$V_{IH,IO}$	1.46		5.0	V	C
1.16	Low-level input voltage VBAT18 domain	VBAT18 = 1.65V to 1.95V	P9, P13, P22, P31	$V_{IL,BAT}$	–0.3		+0.41	V	C
1.17	High-level input voltage VBAT18 domain	VBAT18 = 1.65V to 1.95V	P9, P13, P22, P31	$V_{IH,BAT}$	1.46		5.0	V	C
1.18	Low-level input voltage USB	VDD_USB = 3.0V to 3.6V	DP, DM	$V_{IL,USB}$	–0.3		+0.8	V	C
1.19	High-level input voltage USB	VDD_USB = 3.0V to 3.6V, 39Ω source resistance + 27Ω external series resistor	DP, DM	$V_{IH,USB}$	2.0		4.6	V	C
1.20	Low-level output voltage VDD18 domain	I_{OL} = 1.5 mA, VDD18 = 1.65V		$V_{OL,18}$			0.4	V	A
1.21	High-level output voltage VDD18 domain	I_{OH} = –1.5 mA, VDD18 = 1.65V		$V_{OH,18}$	VDD18 – 0.45			V	A

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Notes:
1. VDDIO is the supply voltage for the following GPIO-pins: P1, P2, P8, P12, P14, P16, P17, P18, P19, P20, P21, P23, P24, P25, P26, P27 and P29
2. Values defined for operating the USB interface. Otherwise VDD_USB may be connected to ground
3. Supply voltage VBAT18 for backup domain is generated internally by the LDOBAT

8. Electrical Characteristics - DC Characteristics (Continued)

If no additional information is given in column Test Conditions, the values apply to a temperature range from –40°C to +85°C.

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
1.22	Low-level output voltage VDDIO domain	I_{OL} = 1.5 mA, VDDIO = 3.0V		$V_{OL,IO}$			0.4	V	A
1.23	High-level output voltage VDDIO domain	I_{OH} = –1.5 mA, VDDIO = 3.0V		$V_{OH,IO}$	VDDIO – 0.5			V	A
1.24	Low-level output voltage VBAT18 domain	I_{OL} = 1 mA	P9, P13, P22, P31	$V_{OL,BAT}$			0.4	V	A
1.25	High-level output voltage VBAT18 domain	I_{OH} = –1 mA	P9, P13, P22, P31	$V_{OH,BAT}$	1.2			V	A
1.26	Low-level output voltage USB	I_{OL} = 2.2 mA, VDD_USB = 3.0V to 3.6V, 27Ω external series resistors	DP, DM	$V_{OL,USB}$			0.3	V	A
1.27	High-level output voltage USB	I_{OH} = –0.2 mA, VDD_USB = 3.0V to 3.6V, 27Ω external series resistors	DP, DM	$V_{OH,USB}$	2.8			V	A
1.28	Input-leakage current (standard inputs and I/Os)	VDD18 = 1.95V V_{IL}=0 V		I_{LEAK}	–1		1	µA	C
1.29	Input capacitance			I_{CAP}			10	pF	D
1.30	Input pull-up resistor		NRESET	R_{PU}	0.7		1.8	kΩ	C
1.31	Input pull-up resistor		TCK, TDI, TMS	R_{PU}	7		18	kΩ	C
1.32	Input pull-up resistor		P9, P13, P22, P31	R_{PU}	100		235	kΩ	C
1.33	Input pull-down resistor		DBG_EN, NTRST,	R_{PD}	7		18	kΩ	C
1.34	Input pull-down resistor		P0, P15, P30, EM_DA[0:15]	R_{PD}	100		235	kΩ	C
1.35	Configurable input pull-up resistor	VDDIO = 3.6V V_{PAD} = 0V	P1, P2, P8, P12, P14, P[16-21], P[23-27], P29	R_{CPU}	50		160	kΩ	C
1.36	Configurable input pull-down resistor	VDDIO = 3.6V V_{PAD} = 3.6V	P1, P2, P8, P12, P14, P[16-21], P[23-27], P29	R_{CPD}	40		160	kΩ	C

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Notes:
1. VDDIO is the supply voltage for the following GPIO-pins: P1, P2, P8, P12, P14, P16, P17, P18, P19, P20, P21, P23, P24, P25, P26, P27 and P29
2. Values defined for operating the USB interface. Otherwise VDD_USB may be connected to ground
3. Supply voltage VBAT18 for backup domain is generated internally by the LDOBAT

8. Electrical Characteristics - DC Characteristics (Continued)

If no additional information is given in column Test Conditions, the values apply to a temperature range from –40°C to +85°C.

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
1.37	Configurable input pull-up resistor (idle state)		USB_DP	R_{CPU}	0.9		1.575	kΩ	C
1.38	Configurable input pull-up resistor (operation state)		USB_DP	R_{CPU}	1.425		3.09	kΩ	C
1.39	Input pull-down resistor		USB_DP USB_DM	R_{PD}	10		500	kΩ	C

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Notes:
1. VDDIO is the supply voltage for the following GPIO-pins: P1, P2, P8, P12, P14, P16, P17, P18, P19, P20, P21, P23, P24, P25, P26, P27 and P29
2. Values defined for operating the USB interface. Otherwise VDD_USB may be connected to ground
3. Supply voltage VBAT18 for backup domain is generated internally by the LDOBAT

9. Power Consumption

Table 9-1. Core Power Consumption

Mode	Conditions	Typ.	Unit	Type*
Sleep	At 1.8V, no CLK23	0.065	mA	C
Shutdown	RTC, backup SRAM and LDOBAT	0.007		C
Normal	Satellite acquisition	25		C
	Normal tracking on 6 channels with 1 fix/s; each additional active tracking channel adds 0.5 mA	14		C
	All channels disabled	11		C

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

10. ESD Sensitivity

The ATR0621P is an ESD sensitive device.

Observe precautions for handling.

Table 10-1. ESD- Sensitivity

Test Model	Max.	Unit
Human Body Model (HBM)	TBD	V

11. LDO18

The LDO18 is a built in low dropout voltage regulator which can be used if the host system does not provide the core voltage VDD18.

Table 11-1. Electrical Characteristics of LDO18

Parameter	Conditions	Min.	Typ.	Max.	Unit	Type*
Supply voltage LDO_IN		2.3		3.6	V	D
Output voltage (LDO_OUT)		1.65	1.8	1.95	V	A
Output current (LDO_OUT)				80	mA	A
Current consumption	After startup, no load, at room temperature			80	µA	A
Current consumption	Standby mode (LDO_EN = 0), at room temperature		1	5	µA	A

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

For well-defined start up of LDO18, LDO_IN needs to be connected to LDOBAT_IN.

12. LDOBAT and Backup Domain

The LDOBAT is a built in low dropout voltage regulator which provides the supply voltage VBAT18 for the RTC, backup SRAM, P9, P13, P22, P31, NSLEEP and NSHDN. The LDOBAT voltage regulator switches in battery mode if LDOBAT_IN falls below 1.5V.

Table 12-1. Electrical Characteristics of LDOBAT

Parameter	Conditions	Min.	Typ.	Max.	Unit	Type*
Supply voltage LDOBAT_IN		2.3		3.6	V	D
Supply voltage VBAT		1.5		3.6	V	D
Output voltage (VBAT18)	If switch connects to LDOBAT_IN.	1.65	1.8	1.95	V	A
Output current (VBAT18)	No external load allowed			1.5	mA	D
Current consumption LDOBAT_IN(1)	After startup (sleep/backup mode), at room temperature			15	µA	A
Current consumption VBAT(1)	After startup (backup mode and LDOBAT_IN = 0V), at room temperature			10	µA	A
Current consumption	After startup (normal mode), at room temperature			1.5	mA	C

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

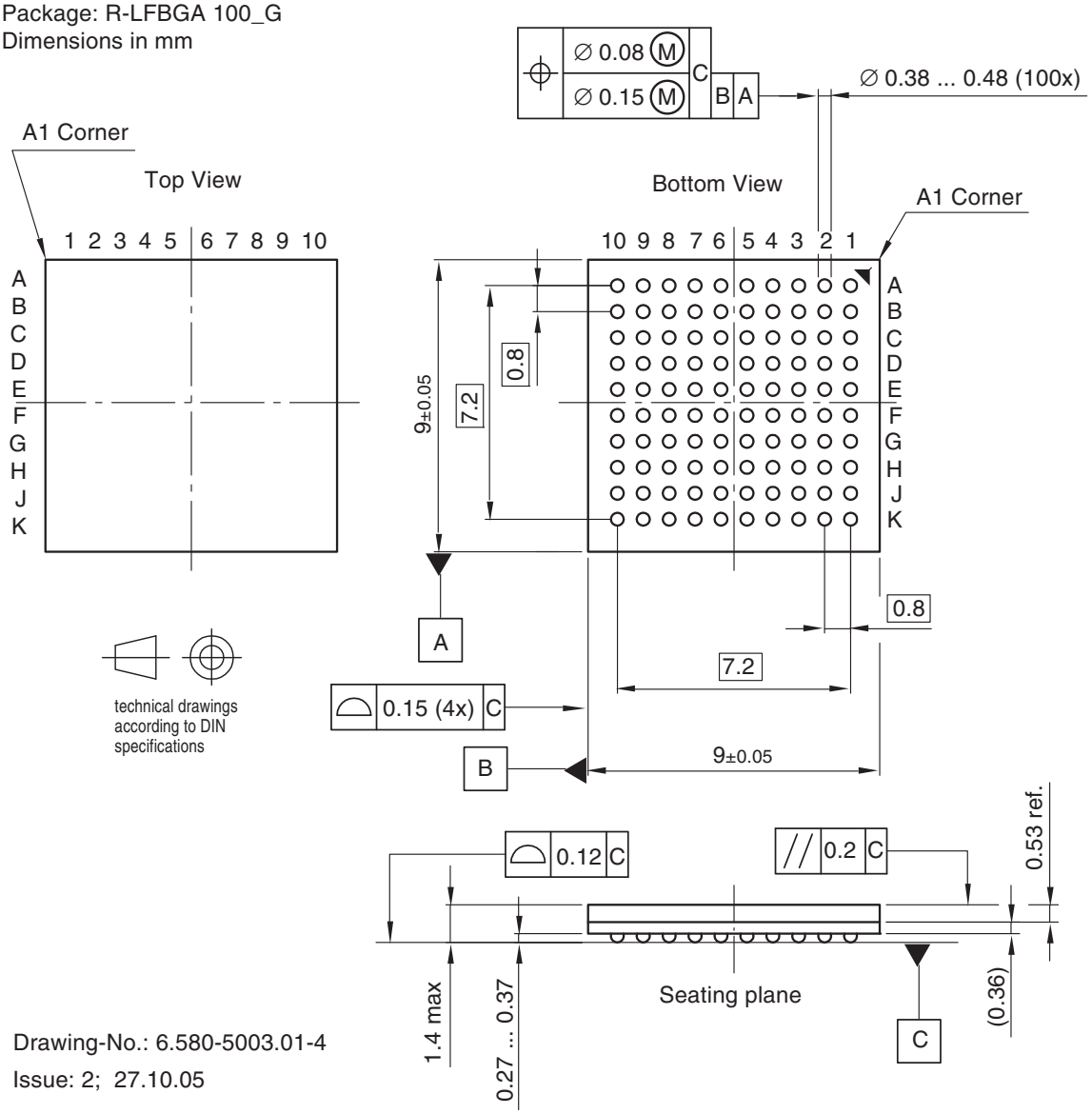
Note: 1. If no current is caused by outputs (pad output current as well as current across internal pull-up resistors)

13. Ordering Information

Extended Type Number	Package	MPQ	Remarks
ATR0621P-7FQY	LFBGA100	2000	9 mm × 9 mm, 0.80 mm pitch, ROM5, Pb-free, RoHS-compliant
ATR0621P-7FHW	LFBGA100	2000	9 mm × 9 mm, 0.80 mm pitch, ROM5, Pb-free, RoHS-compliant, green
ATR0622-EK1	-	1	Evaluation kit/road test kit
ATR0622-DK1	-	1	Development kit including example design information

14. Package LFBGA100

Package: R-LFBGA 100_G
Dimensions in mm



Drawing-No.: 6.580-5003.01-4
Issue: 2; 27.10.05

Moisture sensitivity level (MSL) = 3

15. Revision History

Please note that the following page numbers referred to in this section refer to the specific revision mentioned, not to this document.

Revision No.	History
4890H-GPS-08/08	• Section 8 “Electrical Characteristics - DC Characteristics” numbers 1.11, 1.34 and 1.35 on pages 25 to 26 changed
4890G-GPS-01/08	• Table 3-1 “ATR0621P Pinout” on page 5 changed • Section 13 “Ordering Information” on page 29 changed
4890F-GPS-09/07	• Table 3-1 “ATR0621P Pinout” on page 5 changed
4890E-GPS-06/07	• Section 8 “Electrical Characteristics” numbers 1.35 and 1.36 on page 26 changed
4890D-GPS-12/06	• All pages: Part number changed in ATR0621P • Page 24: Abs. Max. Ratings table: some changes • Page 25-27: El. Characteristics table: Type column added • Page 27: Power Consumption table: Type column added • Page 27: ESD Sensitivity table: Type column added • Page 28: LDO18 table: Type column added • Page 28: LDOBAT and Backup Domain table: Type column added
4890C-GPS-10/06	• Section 7 “Thermal Resistance” on page 24 added • Section 13 “Ordering Information” on page 29 changed
4890B-GPS-06/06	• Table 3-1 “ATR0621 Pinout” on pages 5-8 changed • Section 3.3 “Setting GPSMODE12” on page 11 changed • Table 3-4 “Enable Configuration with GPSMODE Pins” on page 11 changed • Section 3.3.2 “Sensitivity Settings” on page 12 changed • Table 3-5 “GPS Sensitivity Settings” on page 12 changed • Table 3-6 “Serial I/O Configuration” on page 12 changed • Table 3-12 “USB Power Modes” on page 14 changed • Table 3-14 “Antenna Detection I/O Settings” on page 15 changed • Figure 3.2 “Example of an External Connection” on page 16 changed • Table 3-15 “Recommended Pin Connection” on pages 17-18 changed • Section 7 “Electrical Characteristics - DC Characteristics” on pages 25-26 changed • Section 10 “LDO18” on page 27 changed

Headquarters

Atmel Corporation
2325 Orchard Parkway
San Jose, CA 95131
USA
Tel: 1(408) 441-0311
Fax: 1(408) 487-2600

International

Atmel Asia
Room 1219
Chinachem Golden Plaza
77 Mody Road Tsimshatsui
East Kowloon
Hong Kong
Tel: (852) 2721-9778
Fax: (852) 2722-1369

Atmel Europe
Le Krebs
8, Rue Jean-Pierre Timbaud
BP 309
78054
Saint-Quentin-en-Yvelines Cedex
France
Tel: (33) 1-30-60-70-00
Fax: (33) 1-30-60-71-11

Atmel Japan
9F, Tonetsu Shinkawa Bldg.
1-24-8 Shinkawa
Chuo-ku, Tokyo 104-0033
Japan
Tel: (81) 3-3523-3551
Fax: (81) 3-3523-7581

Product Contact

Web Site
www.atmel.com

Technical Support
gps@atmel.com

Sales Contact
www.atmel.com/contacts

Literature Requests
www.atmel.com/literature

4890H–GPS–08/08