
Features

- Operating Voltage: 5V
- Access Time: 40ns
- Very Low Power Consumption
 - Active: 440mW (Max)
 - Standby: 10mW (Typ)
- Wide Temperature Range: -55°C to +125°C
- 600 Mils Width Package: SB28
- TTL Compatible Inputs and Outputs
- Asynchronous
- No Single Event Latch-up below a LET Threshold of 80 MeV/mg/cm²@125°C
- Tested up to a Total Dose of 300 krad (Si) according to MIL STD 883 Method 1019
- ESD better than 4000V
- Deliveries at least equivalent to QML procurement according to MIL-PRF38535
- AT65609EHW is pin to pin compatible with MA9264 device from DYNEX

Description

The AT65609EHW is a very low power CMOS static RAM organized as 8192 x 8 bits. Using an array of six transistors (6T) memory cells, the AT65609EHW combines an extremely low standby supply current with a fast access time at 40 ns over the full military temperature range. The high stability of the 6T cell provides excellent protection against soft errors due to noise.

The AT65609EHW is processed according to the methods of the latest revision of the MIL PRF 38535.

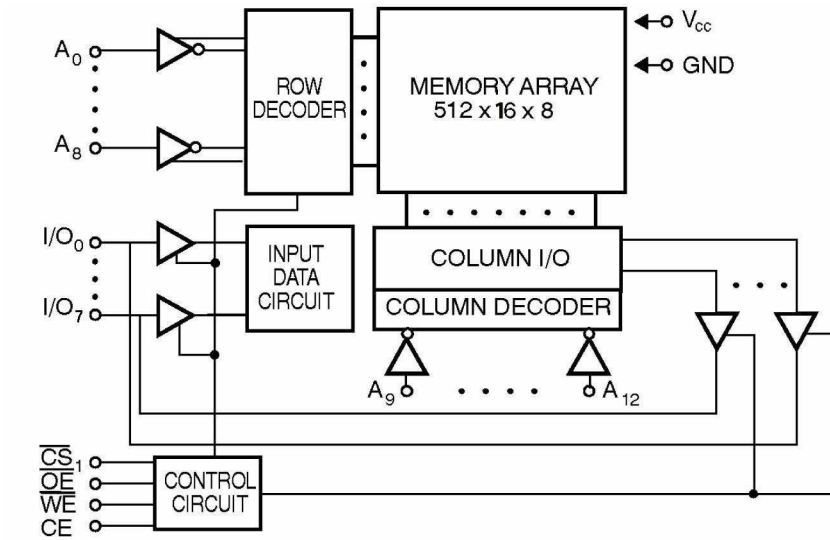
It is manufactured on the same process as the MH1RT RAD-hard sea of gates series.



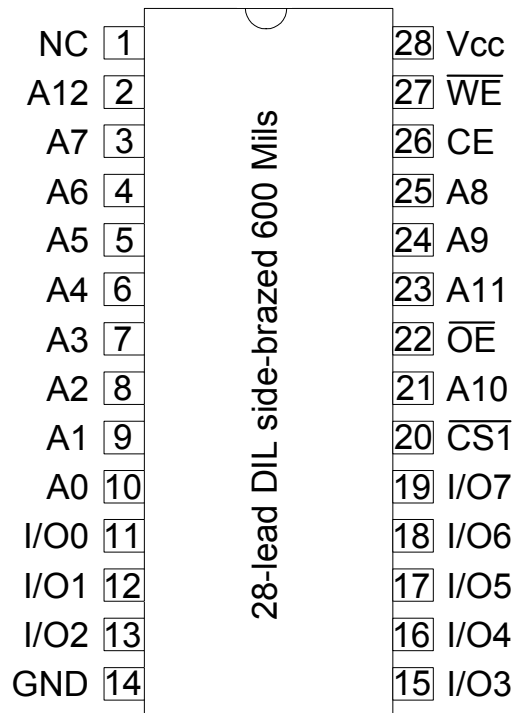
**Rad. Tolerant
8K x 8 - 5 volts
Very Low Power
CMOS SRAM**

AT65609EHW

Block Diagram



Pin Configuration



Note: NC pin is not bonded internally. So, it can be connected to GND or VCC.

Pin Description

Table 1. Pin Names

Names	Description
A0 - A12	Address inputs
I/O0 - I/O7	Data Input/Output
$\overline{\text{CS1}}$	Chip select
CE	Chip Enable
$\overline{\text{WE}}$	Write Enable
$\overline{\text{OE}}$	Output Enable
VCC	Power
GND	Ground

Table 2. Truth Table

$\overline{\text{CS1}}$	CE	$\overline{\text{WE}}$	$\overline{\text{OE}}$	Inputs/ Outputs	Mode
H	X	X	X	Z	Deselect / Power-down
X	L	X	X	Z	Deselect / power-down
L	H	H	L	Data Out	Read
L	H	L	X	Data In	Write
L	H	H	H	Z	Output Disable

Note: L = low, H = high, X = H or L, Z = high impedance.



Electrical Characteristics

Absolute Maximum Ratings

Supply voltage to GND potential:.....-0.5V + 7.0V	<p>*NOTE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure between recommended DC operating and absolute maximum rating conditions for extended periods may affect device reliability.</p>
DC input voltage:GND - 0.3V to VCC + 0.3	
DC output voltage high Z state:GND - 0.3V to VCC + 0.3	
Storage temperature:.....-65-C to +150-C	
Output current into outputs (low): 20 mA	
Electro Static Discharge voltage with HBM method (MIL STD 883D method 3015):..... > 4000V	
Electro Static Discharge voltage with Socketed CDM method (ANSI/ESD SP5.3.2-2004) :..... > 1000V	

Military Operating Range

Operating Voltage	Operating Temperature
5V ± 10%	-55°C to + 125°C

Recommended DC Operating Conditions

Parameter	Description	Minimum	Typical	Maximum	Unit
V _{CC}	Supply voltage	4.5	5.0	5.5	V
GND	Ground	0.0	0.0	0.0	V
V _{IL}	Input low voltage	GND - 0.3	0.0	0.8	V
V _{IH}	Input high voltage	2.2	–	VCC + 0.3	V

Capacitance

Parameter	Description	Minimum	Typical	Maximum	Unit
C _{in} ⁽¹⁾	Input low voltage	–	–	8	pF
C _{out} ⁽¹⁾	Output high voltage	–	–	8	pF

Note: 1. Guaranteed but not tested.

DC Parameters

DC Test Conditions TA = -55°C to + 125°C; Vss = 0V; V_{CC} = 4.5V to 5.5V

Symbol	Description	Minimum	Typical	Maximum	Unit
IIX ⁽¹⁾	Input leakage current	-10	–	10	μA
IOZ ⁽¹⁾	Output leakage current	-10	–	10	μA
VOL ⁽²⁾	Output low voltage	–	–	0.4	V
VOH ⁽³⁾	Output high voltage	2.4	–	–	V

1. GND < Vin < V_{CC}, GND < Vout < V_{CC} Output Disabled.
2. V_{CC} min. IOL = 8 mA
3. V_{CC} min. IOH = -4 mA.

Consumption

Symbol	Description	AT65609EHW	Unit	Value
ICCSB ⁽¹⁾	Standby supply current	5	mA	max
ICCSB1 ⁽²⁾	Standby supply current	3	mA	max
ICCOP ⁽³⁾	Dynamic operating current	80	mA	max

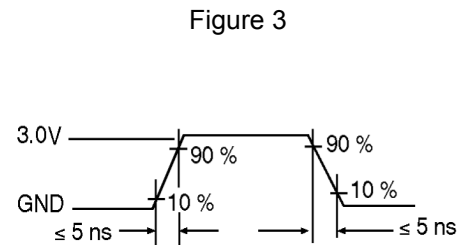
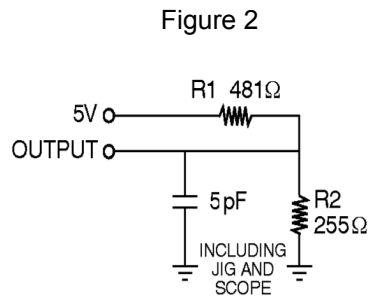
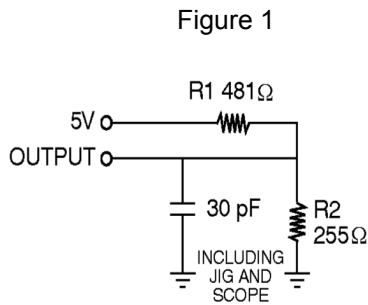
1. $\overline{CS1} > V_{IH}$ or $CE < V_{IL}$ and $\overline{CS1} < V_{IL}$.
2. $\overline{CS1} > V_{CC} - 0.3V$ or, $CE < GND + 0.3V$ and $\overline{CS1} < 0.2V$.
3. $F = 1/TAVAV$, $I_{out} = 0$ mA, $\overline{WE} = \overline{OE} = V_{CC}$, $V_{in} = GND$ or V_{CC} , V_{CC} max, $\overline{CS1} = V_{IL}$, $CE = V_{IH}$

AC Parameters

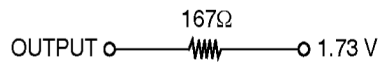
AC Test Conditions

Input Pulse Levels: GND to 3.0V
 Input Rise/Fall Times: 5 ns
 Input Timing Reference Levels: 1.5V
 Output loading IOL/IOH (see Figure 1 and Figure 2) 30 pF

AC Test Loads Waveforms



Equivalent to : THEVENIN EQUIVALENT

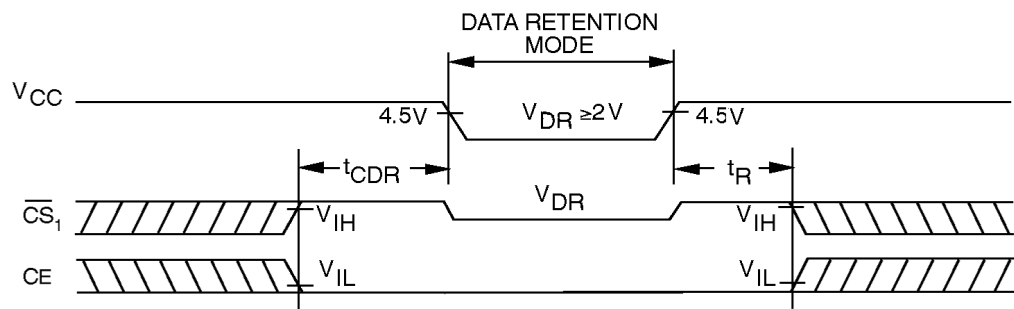


Data Retention Mode

Atmel CMOS RAM's are designed with battery backup in mind. Data retention voltage and supply current are guaranteed over temperature. The following rules ensure data retention:

1. During data retention chip select $\overline{CS1}$ must be held high within V_{CC} to $V_{CC} - 0.2V$ or, chip select CE must be held down within GND to $GND + 0.2V$.
2. Output Enable (\overline{OE}) should be held high to keep the RAM outputs high impedance, minimizing power dissipation.
3. During power up and power-down transitions $\overline{CS1}$ and \overline{OE} must be kept between $V_{CC} + 0.3V$ and 70% of V_{CC} , or with CE between GND and $GND - 0.3V$.
4. The RAM can begin operation $> TR$ ns after V_{CC} reaches the minimum operation voltages (4.5V).

Timing



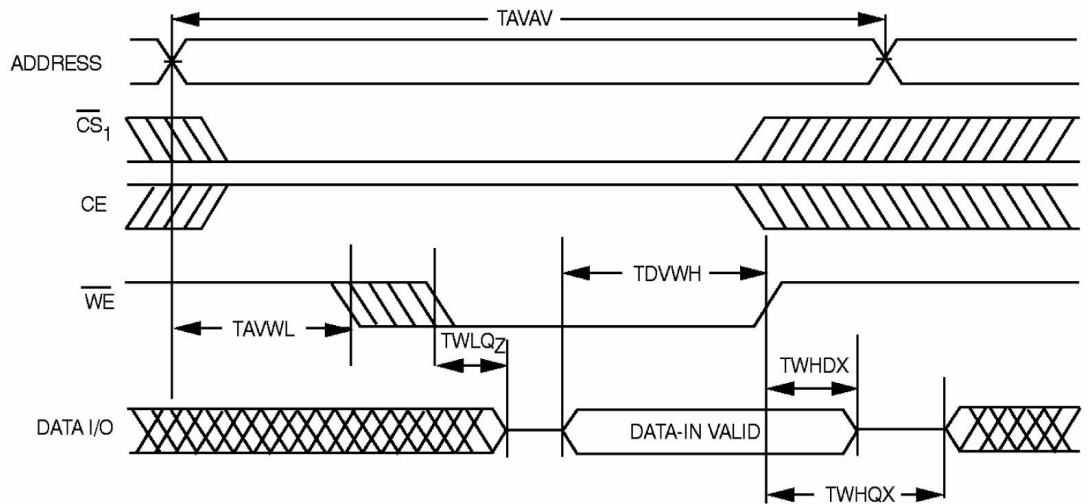
Data Retention Characteristics

Parameter	Description	Minimum	Typical TA = 25 °C	Maximum	Unit
VCCDR	V_{CC} for data retention	2.0	–	–	V
TCDR	Chip deselect to data retention time	0.0	–	–	ns
TR	Operation recovery time	TAVAV ⁽¹⁾	–	–	ns
ICCDR1 ⁽²⁾	Data retention current at 2.0V	–	1	1.5	mA
ICCDR2 ⁽²⁾	Data retention current at 3.0V	–	1.5	2	mA

Notes: 1. TAVAV = Read Cycle Time
 2. $\overline{CS1} = V_{CC}$ or $CE = \overline{CS1} = GND$, $V_{in} = GND/V_{CC}$, this parameter is only tested at $V_{CC} = 2V$.

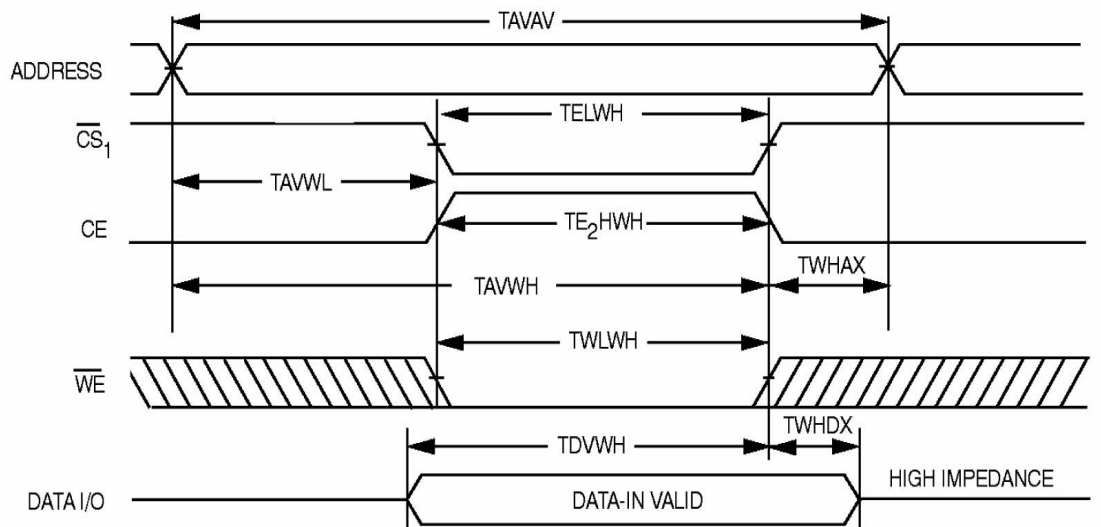
Write Cycle 2

$\overline{\text{WE}}$ Controlled, $\overline{\text{OE}}$ Low



Write Cycle 3

$\overline{\text{CS}}_1$ or CE Controlled



Note: The internal write time of the memory is defined by the overlap of $\overline{\text{CS}}_1$ Low and CE HIGH and $\overline{\text{WE}}$ LOW. Both signals must be activated to initiate a write and either signal can terminate a write by going in active. The data input setup and hold timing should be referenced to the activated edge of the signal that terminates the write. Data out is high impedance if $\overline{\text{OE}} = V_{IH}$.

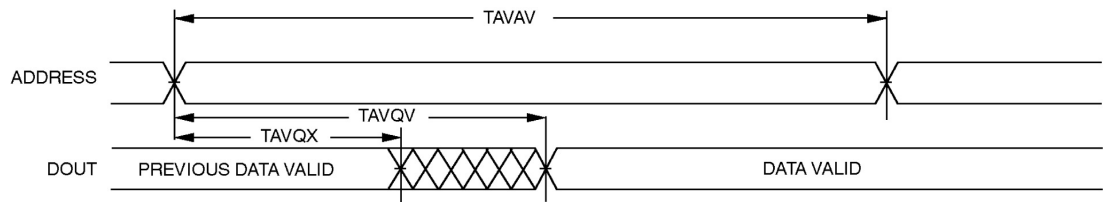
Read Cycle

Symbol	Parameter	AT65609EHW	Unit	Value
TAVAV	Read cycle time	40	ns	min
TAVQV	Address access time	40	ns	max
TAVQX	Address valid to low $Z^{(1)}$	3	ns	min
TE1LQV	Chip-select1 access time	40	ns	max
TE1LQX	$\overline{CS1}$ low to low $Z^{(1)}$	3	ns	min
TE1HQZ	$\overline{CS1}$ high to high $Z^{(1)}$	15	ns	max
TE2HQV	Chip-select2 access time	40	ns	max
TE2HQX	CE high to low $Z^{(1)}$	3	ns	min
TE2LQZ	CE low to high $Z^{(1)}$	15	ns	max
TGLQV	Output Enable access time	15	ns	max
TGLQX	\overline{OE} low to low $Z^{(1)}$	0	ns	min
TGHQZ	\overline{OE} high to high $Z^{(1)}$	10	ns	max

Note: 1. Parameters Guaranteed, not tested, with output loading 5 pF.

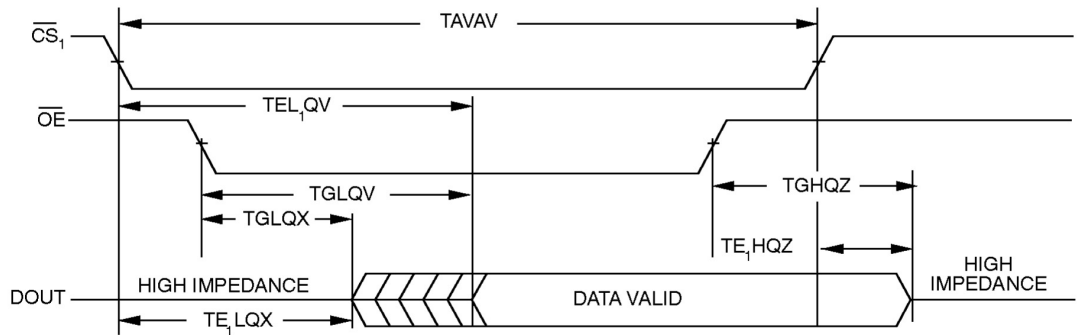
Read Cycle 1

Address Controlled ($\overline{CS1} = \overline{OE}$ Low, $CE = \overline{WE}$ High)



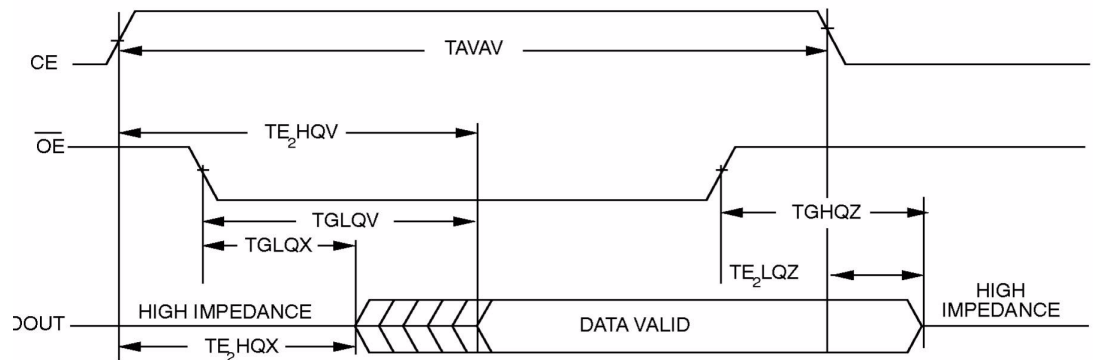
Read Cycle 2

$\overline{CS1}$ Controlled ($CE = \overline{WE}$ High)



Read Cycle 3

CE Controlled (\overline{WE} High, $\overline{CS1}$ Low)

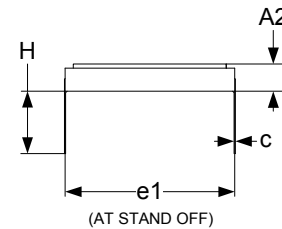
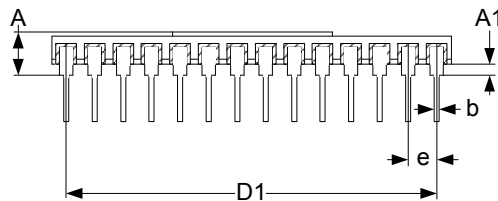
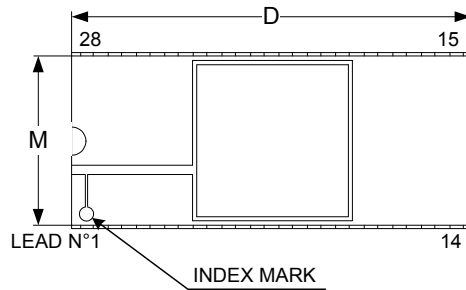


Ordering Information

Atmel Reference Part Number	Temperature Range	Speed	Package	Flow
AT65609EHW-CI40-E	25-C	40ns	SB28.6	Engineering Samples
AT65609EHW-CI40MQ	-55- to +125-C	40ns	SB28.6	Mil Level B
AT65609EHW-CI40SV	-55- to +125-C	40ns	SB28.6	Space Level B
AT65609EHW-CI40SR	-55- to +125-C	40ns	SB28.6	Space Level B RHA

Package Drawing

28-lead Side Braze 600 Mils



Ref	Millimeters			Inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	3.73	3.99	4.24	0.147	0.157	0.167
A1	1.02	1.27	1.52	0.040	0.050	0.060
A2	2.47	2.73	2.98	0.0974	0.1074	0.1174
b	0.41	0.46	0.51	0.016	0.018	0.020
c	0.23	0.25	0.30	0.009	0.010	0.012
D	35.20	35.56	35.92	1.386	1.400	1.414
D1	32.89	33.02	33.15	1.295	1.300	1.305
e	2.41	2.54	2.67	0.095	0.100	0.105
e1	14.99	15.24	15.49	0.590	0.600	0.610
H			5.51			0.217
M	14.86	15.11	15.37	0.585	0.595	0.605

Document Revision History

Changes from 7791A to 7791B

1. Page 1 : total dose value updated
2. Page 6 : note 3 of consumption table updated

Changes from 7791B to 7791C

1. Page 1 : ESD item added
2. Page 5 : ESD HBM improved and ESD Socketed CDM added
3. Page 13 : ordering Information section updated
4. page 14 : package drawing updated



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