

## Errata Description

The following is a known problem in revision **R and prior** of the AT89S8253 in SPI communication:

During a master-slave SPI communication, whenever the  $\overline{SS}$  input pin of the AT89S8253 acting as the slave device is pulled high during a transmission cycle, the internal SPI bit counter of the (slave) AT89S8253 does not get reset. If  $\overline{SS}$  goes high during a data transfer, all subsequent data will be corrupted in the slave. If  $\overline{SS}$  goes high in between transfers, the data remains unaffected.

### Workarounds:

1. Perform a hardware reset.
- or
2. Clear and then set the SPE bit in the SPCR register of the (slave) AT89S8253.



## AT89 Microcontrollers

### AT89S8253

### Rev. R

## Errata Sheet





## Headquarters

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**Atmel Corporation**  
2325 Orchard Parkway  
San Jose, CA 95131  
USA  
Tel: 1(408) 441-0311  
Fax: 1(408) 487-2600

## International

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**Atmel Asia**  
Room 1219  
Chinachem Golden Plaza  
77 Mody Road Tsimshatsui  
East Kowloon  
Hong Kong  
Tel: (852) 2721-9778  
Fax: (852) 2722-1369

**Atmel Europe**  
Le Krebs  
8, Rue Jean-Pierre Timbaud  
BP 309  
78054 Saint-Quentin-en-  
Yvelines Cedex  
France  
Tel: (33) 1-30-60-70-00  
Fax: (33) 1-30-60-71-11

**Atmel Japan**  
9F, Tonetsu Shinkawa Bldg.  
1-24-8 Shinkawa  
Chuo-ku, Tokyo 104-0033  
Japan  
Tel: (81) 3-3523-3551  
Fax: (81) 3-3523-7581

## Product Contact

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**Web Site**  
[www.atmel.com](http://www.atmel.com)

**Technical Support**  
[mcu@atmel.com](mailto:mcu@atmel.com)

**Sales Contact**  
[www.atmel.com/contacts](http://www.atmel.com/contacts)

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