Features

- **DC to DC Step Down 1.2 A, 0.9V (Dynamically Adjustable to 0.87V/1.1V/1.2V)**
- **DC to DC step Down 1.2 A, 1.2V (Dynamically Adjustable to 1.0V/1.1V/1.3V) or 1.75V (Dynamically Adjustable 1.65V/1.70V/1.80V)**
- **DC to DC Step Down 1.2 A, 1.8V (Dynamically Adjustable to 1.70V/1.75V/1.85V) or 2.5V (Dynamically Adjustable 2.3V/2.4V/2.6V)**
- **DC to DC Step Up/Down 520 mA, 3.3V (Dynamically Adjustable to 3.0V/3.1V/3.4V)**
- **Dual Battery Chargers: Li+ Precharge, Fast Charge, Top-up Charge, 4.1V (or Adjustable), Processor Tuned Algorithms**
  - **USB Trickle Charge: Precharge Flat Battery from USB Pre-enumeration, then Auto-wake of Processor at 3.8V Battery Level**
  - **Battery Charge Select: 25 mA to 500 mA**
  - **Real-time Charge Inhibit: Allows Charge Suspend (e.g. During TX Slots)**
- **Supply Monitor of Four Power Sources: Thermistors, Temperature, DC/DC Rails, all Supplied with Out-of-regulation Threshold Detection**
- **SIM Interface: SIM / USIM, 1.8V / 3.0V Standards, Integrated TX and RX Data FIFO**
- **SPI Control Interface: Up to 13 MHz; Tuned for SA1110/PXA250/PXA255 1.2 MHz SPI, 128 8-bit Registers**
- **Power on Reset: For SA1110/PXA250/PXA255 Architectures plus Additional Sequenced System Level Resets**
- **Voltage and Temperature Supervision**
- **Calibrated Voltage Reference**
- **8-bit ADC with 5-input Multiplexer**
- **Integrated Oscillator, Start-up and Self-protection Circuitry**
- **Off Power: 60 µA with External “Button Select” for Restart**
- **Applications Include: PDAs, PCMCIA Cards, SMART Phones, Pocket PCs, 3G Applications, Intel® XScale™ Powered Applications**

Description

The AT73C203 device provides an integrated solution to portable and handheld applications built around microprocessors requiring “smart” power management functions, such as PDAs, Palmtop computers, point-of-sales terminals, 3G modems, etc.

Its compact package outline and small size of external components make the AT73C203 suitable for PCMCIA card power management as well.

The AT73C203 integrates a power switch controller that, when connected to an external power switch, may be used for automatically selecting one of four possible power sources:

- Internal battery
- External battery
- Plugtop power supply unit 5V (PSU)
- PC Host USB supply

The power switch output (VDD-PSU line) is connected directly to external auxiliary components such as a radio or any other “current hungry” module.

The AT73C203 is also equipped with four digital rails from VDD-PSU to supply a baseband chip, a reset generator for the baseband chip, and a SPI interface to control the AT73C203 via an internal register set. The USIM interface allows the application processor to communicate with and control a USIM card. Charge control enables the application processor to charge the battery from the PSU or USB. A state machine can also determine whether to charge the internal battery through USB at start-up. Additionally, hardware monitoring gives information to the application processor when a voltage drop occurs (programmed via internal registers).

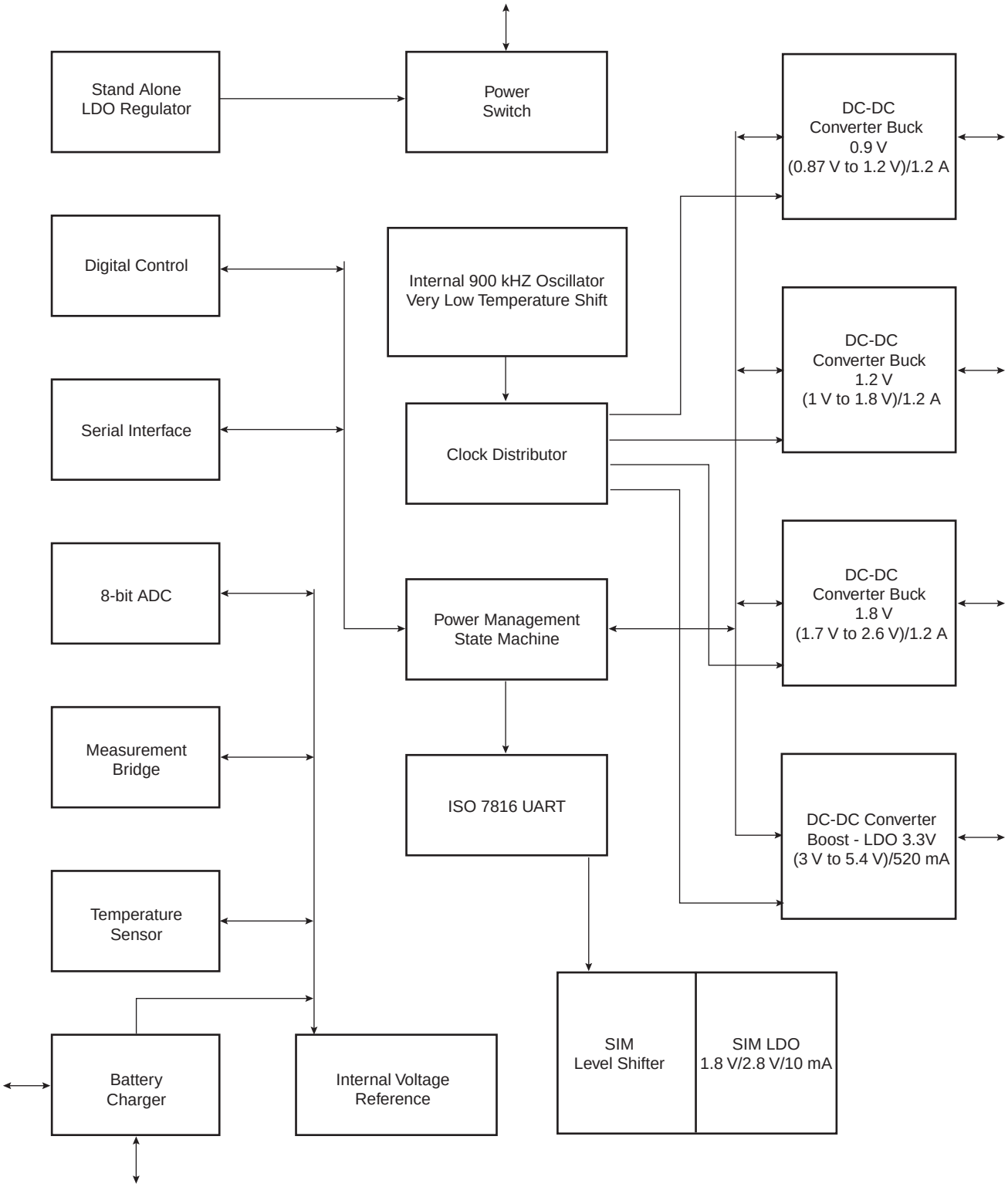
Power Management

AT73C203 Power Management IC for Datacom Platforms

2742B–PMGMT–03/04

Functional Diagram

Figure 1. AT73C203 Functional Diagram



Pin Description

Table 1. AT73C203 Pin Description

Signal Name	Pin Type	Pack Pin	Level	ESD Protection	Comments
AVSS	A-I	A1	AVSS		ESD Ground
SELDC175	D-I	B2	gnddig - vsauv	avss - vswin	Digital control
SELDC25	D-I	B1	gnddig - vsauv	avss - vswin	Digital control
nEN_RAIL3	D-I/O	A3	gnddig - vsauv	avss - vswin	Digital control
nEN_RAIL4	D-I/O	A2	gnddig - vsauv	avss - vswin	Digital control
nASIC_RESET	D-O	C3	gnddig - vout3	avss - vout3	RESET
nBOARD_RESET	D-O	C1	gnddig - vout3	avss - vout3	RESET
BOARD_RESET	D-O	C2	gnddig - vout3	avss - vout3	RESET
nPROC_RESET	D-O	D4	gnddig - vout3	avss - vout3	RESET
nPROC_RESET_OUT	D-I	D3	gnddig - vout3	avss - vout3	RESET
nASIC_RESET_REQUEST	D-I	D1	gnddig - vout3	avss - vout3	RESET
POWER_EN	D-I	D2	gnddig - vout3	avss - vout3	Digital control
SYST_CLK	D-I	A4	gnddig - vout3	avss - vout3	Digital control
nUSIM_INT	D-O	E1	gnddig - vout3	avss - vout3	Digital control
nINT	D-O	E2	gnddig - vout3	avss - vout3	Digital control
BUTTON_OUT	D-O	E3	gnddig - vout3	avss - vout3	Digital control
CHG_INHIBIT	D-I	F1	gnddig - vout3	avss - vout3	Digital control
TEST1	D-I/O	F2	gnddig - vsauv	avss – vsauv	TEST
TEST2	D-I/O	F3	gnddig - vsauv	avss - vsauv	TEST
IDBITS3	D-I/O	G1	gnddig - vout3	avss - vout3	Digital control
IDBITS2	D-I/O	F4	gnddig - vout3	avss - vout3	Digital control
IDBITS1	D-I/O	G2	gnddig - vout3	avss - vout3	Digital control
IDBITS0	D-I/O	H1	gnddig - vout3	avss - vout3	Digital control
SDO	D-I/O	G3	gnddig - vout3	avss - vout3	SPI
SDI	D-I	H2	gnddig - vout3	avss - vout3	SPI
SCLK	D-I	J1	gnddig - vout3	avss - vout3	SPI
nSEN	D-I	E5	gnddig - vout3	avss - vout3	SPI
GNDDIG	A-I	K1	GND	avss - gnddig	Digital ground
VOUT3	A-I	K2	gnddc3 - vout3	avss - vboost	DCDC rail3
VBOOST	A-I	J2	gnddc3 - vddpsu	PCboost	DCDC rail3
DH3	A-O	K3	gnddc3 - vddpsu	avss - vboost	DCDC rail3
GNDDC3	A-I	H3	GND	avss - gnddc3	DCDC rail3
DL3	A-O	J3	gnddc3 - vddpsu	avss - PCmax	DCDC rail3
VDDPSU3	A-I	G4	gnddc3 - vddpsu	avss - PCmax	DCDC rail3

Table 1. AT73C203 Pin Description (Continued)

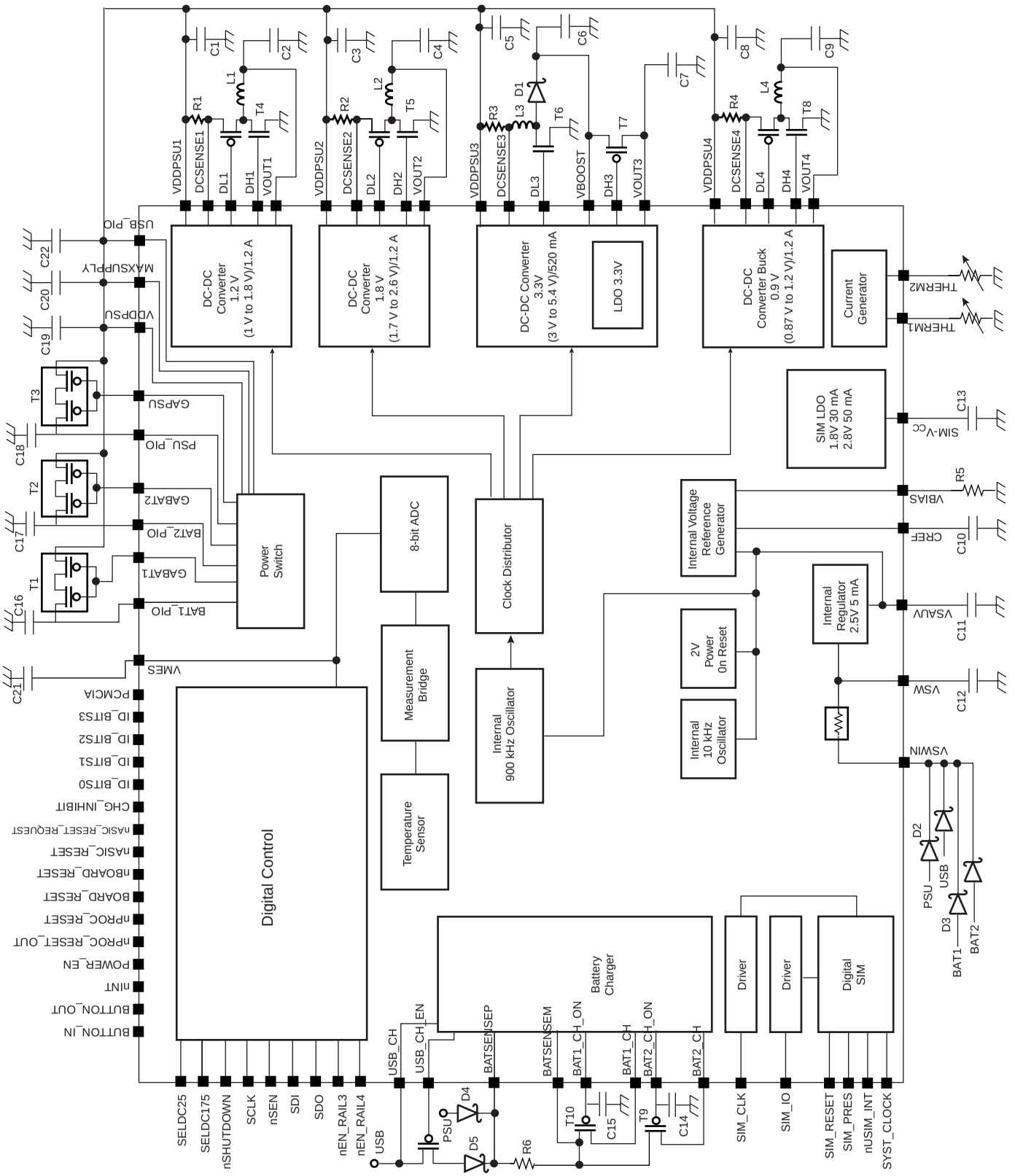
Signal Name	Pin Type	Pack Pin	Level	ESD Protection	Comments
DCSENSE3	A-I	H4	gnddc3 - vddpsu	avss - PCmax	DCDC rail3
VOUT2	A-I	K4	gnddc2 - vout2	avss - PCmax	DCDC rail2
DCSENSE2	A-I	H5	gnddc2 - vddpsu	avss - PCmax	DCDC rail2
DH2	A-O	K5	gnddc2 - vddpsu	avss - PCmax	DCDC rail2
VDDPSU2	A-I	G5	gnddc2 - vddpsu	avss - PCmax	DCDC rail2
GNDDC2	A-I	J4	GND	avss - gnddc2	DCDC rail2
DL2	A-O	J5	gnddc2 - vddpsu	avss - PCmax	DCDC rail2
VOUT1	A-I	K6	gnddc1 - vout1	avss - PCmax	DCDC rail1
DCSENSE1	A-I	H6	gnddc1 - vddpsu	avss - PCmax	DCDC rail1
DH1	A-O	K7	gnddc1 - vddpsu	avss - PCmax	DCDC rail1
VDDPSU1	A-I	G6	gnddc1 - vddpsu	avss - PCmax	DCDC rail1
GNDDC1	A-I	J6	GND	avss - gnddc1	DCDC rail1
DL1	A-O	J7	gnddc1 - vddpsu	avss - PCmax	DCDC rail1
VOUT4	A-I	J10	gnddc4 - vout4	avss - PCmax	DCDC rail4
DCSENSE4	A-I	K9	gnddc4 - vddpsu	avss - PCmax	DCDC rail4
DH4	A-O	K8	gnddc4 - vddpsu	avss - PCmax	DCDC rail4
VDDPSU4	A-I	K10	gnddc4 - vddpsu	avss - PCmax	DCDC rail4
GNDDC4	A-I	J9	GND	avss - gnddc4	DCDC rail4
DL4	A-O	J8	gnddc4 - vddpsu	avss - PCmax	DCDC rail4
SIM_CLK	D-O	H10	gnddig - vsim	avss - PCmax	SIM
SIM_RESET	D-O	H9	gnddig - vsim	avss - PCmax	SIM
SIM_IO	D-I/O	G7	gnddig - vsim	avss - PCmax	SIM
SIM_VCC	A-O	G8	gnddig - vsim	avss - PCmax	SIM regulator
GND_CH	A-I	E6	GND	avss - gndch	Charger
BAT2_CH	A-I	F7	gndch - maxsupply	avss - PCmax	Charger
BAT1_CH	A-I	F10	gndch - maxsupply	avss - PCmax	Charger
BAT2_CH_ON	A-O	F9	gndch - maxsupply	avss - PCmax	Charger
BAT1_CH_ON	A-O	F8	gndch - maxsupply	avss - PCmax	Charger
BATSENSEM	A-I	E10	gndch - maxsupply	avss - PCmax	Charger
BATSENSEP	A-I	E9	gndch - maxsupply	avss - PCmax	Charger
USB_CH_EN	A-O	E8	gndch - maxsupply	avss - PCmax	Charger
USB_CH	A-I	D10	gndch - maxsupply	avss - PCmax	Charger
GABAT1	D-O	E7	gnda1 - maxsupply	avss - PCmax	Power switch
GABAT2	D-O	D9	gnda1 - maxsupply	avss - PCmax	Power switch
GAPSU	D-O	C10	gnda1 - maxsupply	avss - PCmax	Power switch
VDDPSU	A-I	G10	gnda1 - vddpsu	avss - PCmax	Power switch

Table 1. AT73C203 Pin Description (Continued)

Signal Name	Pin Type	Pack Pin	Level	ESD Protection	Comments
BAT1_PIO	A-I	D8	gnda1 - bat1	avss - PCmax	Power switch
BAT2_PIO	A-I	C9	gnda1 - bat2	avss - PCmax	Power switch
PSU_PIO	A-I	B10	gnda1 - psu	avss - PCmax	Power switch
USB_PIO	A-I	D6	gnda1 - usb	avss - PCmax	Power switch
MAXSUPPLY	A-O	A10	gnda1 - maxsupply	PCmax	Power switch
GND_PIO	A-I	B9	GND	avss - gnda1	Power switch
VREFFUSE	A-I	A9	avss - 5.5v	avss-vswin	FUSES
VBIAS	A-O	C8	gnda - vsauv	avss - vswin	Reference generator
CREF	A-O	A8	gnda - vsauv	avss - vswin	Reference generator
VMES	A-O	B8	gnda - vsauv	avss - vswin	Measurement bridge
PORTEST	D-O	D7	gnda - vsauv	avss - vswin	Power on reset
THERM1	A-O	C7	gnda - vsauv	avss - vswin	Current generator
THERM2	A-O	A7	gnda - vsauv	avss - vswin	Current generator
GNDA	A-I	B7	GND	avss - gnda	Internal regulator
VSAUV	A-O	C6	gnda - vsauv	avss - vswin	Internal regulator
VSW	A-I	A6	gnda - vswin	avss - vswin	Internal regulator
VSWIN	A-I	B6	gnda - vswin	PCvswin	Internal regulator
SCAN_TEST_MD	D-I/O	C4	gnddig - vsauv	avss - vswin	TEST
SCAN_ENABLE	D-I/O	A5	gnddig - vsauv	avss - vswin	TEST
nSHUTDOWN	D-I	B5	gnddig - vsauv	avss - vswin	Digital control
PCMCIA	D-I	C5	gnddig - vsauv	avss - vswin	Digital control
SIM_PRES	D-I	G9	gnddig - vsauv	avss - vswin	Digital control
BUTTON_IN	D-I	D5	gnddig - vsauv	avss - vswin	Digital control
NC		B4			Not Connected
NC		E4			Not Connected
NC		H8			Not Connected
NC		H7			Not Connected
NC		F5			Not Connected
NC		B3			Not Connected
NC		F6			Not Connected

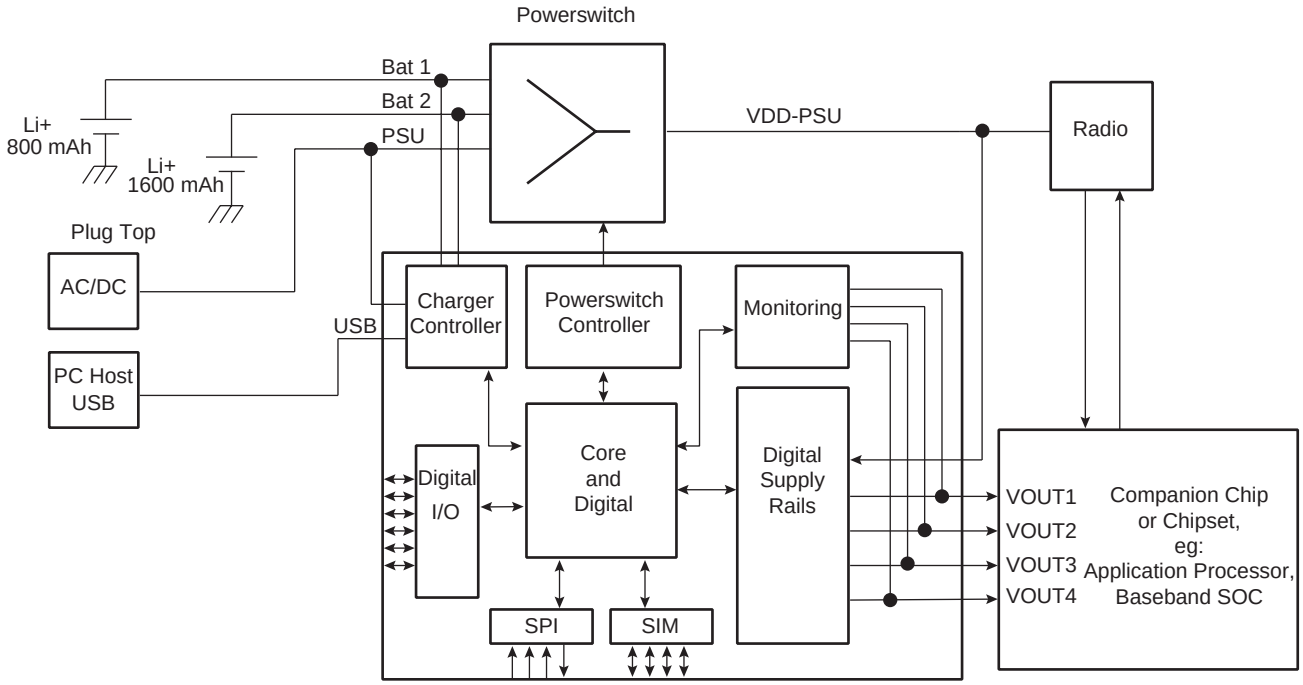
Application Schematic

Figure 2. AT73C203 Application Schematic



Architecture Overview

Figure 3. AT73C203 Architecture Overview



System Level Description

Several power sources may be used to power the AT73C203 circuitry including an internal or external battery, external PSU or USB. The internal battery is always physically present in the unit, but any or all of the other sources may be connected or disconnected at any time.

The AT73C203 enables one application to be powered up from the correct source of up to four possible power sources under hardware control. When powered, the external processor can monitor the input power sources and initiate battery charging as required via the SPI. The application processor is also able to enable/disable the circuit power rails and configure a low power sleep state.

An input-multiplexed 8-bit ADC is available that allows the application processor to monitor the presence of and measure the voltage of the power sources, batteries and rails. An associated threshold and comparator circuit may be used to indicate to the processor that an out-of limit event has occurred.

The battery charging circuitry is designed to allow charging from the PSU input and to allow current-limited 'supplement' charging from the USB input. In both cases, the chargers operate under processor control and monitoring with hardware safety lockout.

When the PSU is present, a power path is selected (e.g. from a DC jack) through the power switching circuitry to the external components (e.g. radio and companion chips or chipset, baseband chip etc.) This power path enables the application processor to boot up. A parallel path exists from the PSU input (e.g. jack) through current limiting devices to two battery chargers. The current switches only block reverse current when disabled so care must be taken when controlling them.

When a USB input is powered, a single power path exists through the current limiting devices to the two battery chargers. The hardware defaults to a current limit of 100 mA

but the application processor may set 500 mA after negotiation with the PC. This power should always be used to charge the batteries in the absence of the PSU power source.

SIM/USIM interface hardware is provided, allowing the application processor to communicate and control a SIM/USIM card according to the required analog and digital specifications.

Most of the blocks are switched on or off by the digital control block (not all the control lines are drawn on the block diagram).

Only the supply monitor, digital control, power on reset, 10 kHz internal oscillator and internal regulator are always on.

All these blocks are designed to have very low power consumption, capable of achieving three months standby time for the application.

Functional Integration

The AT73C203 integrates the following functions:

Supply Monitor

The supply monitor block enables the AT73C203 to correctly switch the four main supplies (two batteries, PSU and USB). All the outputs are sent to the digital control.

Internal Regulator

The internal regulator is a low drop out regulator generating V_{SAUV} at 2.5V with a maximum load of 5 mA. Its input is V_{SW}.

Power-on Reset

The internal power-on reset is supplied by V_{SAUV} and resets the AT73C203 digital circuitry at 2V.

10 kHz Internal Oscillator

The 10 kHz low power oscillator is the clock source for the AT73C203 digital circuitry. V_{SAUV} supplies it.

Digital Control

The digital block controls each block and drives the SPI interface and the different interrupts (external and internal). The controls, inputs and outputs are level shifted when necessary and protected to avoid current flowing between the blocks (not represented in the block diagram). A state machine controls the AT73C203 circuitry according the supplies and inputs states. A table of registers is accessible via SPI to command or read status of the AT73C203.

Reference Generator

The reference generator provides the AT73C203 with a precise bandgap voltage (V_{REF}) and current bias (I_{REF}) used by all analog blocks (DC/DC, ADC, charger) except the core blocks. It is turned off under digital control when necessary and is V_{SAUV} supplied.

900 kHz Oscillator and Clock Distribution

The 900 kHz oscillator provides the clock to all DC/DC converters. The clock distributor provides phased clocks to the DC/DC converters to avoid switching at the same time. The frequency of the oscillator is trimmed during production to optimize the DC/DC efficiency.

DC to DC Step Down 1.2 A, 0.9V

The DC to DC step Down 1.2A, 0.9V (dynamically adjustable to 0.87V/0.9V/1.1V/1.2V) is a programmable buck DC/DC converter dedicated to advanced sub-micron processors and SoC ASIC logic cores requiring dynamic power management at low voltages and high currents.

The default voltage is 0.9V for which the device is optimized.

The external components needed include a current sensing resistor, a dual PMOS-NMOS, an inductor and an output capacitor.

The application processor can change the output voltage via registers accessible by SPI.

When the cell is off, the output is in high impedance state.

If not used, this section can be permanently deactivated.

DC to DC Step Down 1.2A, 1.2V OR 1.75V

The DC to DC step Down 1.2A, 1.2V (dynamically adjustable to 1.0V/1.1V/1.2V/1.3V) is a programmable buck synchronous DC/DC converter dedicated to the application processor core and/or a “companion” ASIC SoC Processor Core. The default voltage is 1.2V. An external pin can select 1.75V output voltage with tuning: 1.80V, 1.70V or 1.65V. The entire cell is optimized for 1.2V. The application processor can change the output voltage as described above via registers accessible by SPI.

The external components needed include a current sensing resistor, a dual PMOS-NMOS, one inductor and one output capacitor.

When the cell is off, the output is pulled to ground.

If not used, this section can be permanently deactivated

DC to DC Step Down 1.2A, 1.8V OR 2.5V

The DC to DC step Down 1.2A, 1.8V (dynamically adjustable to 1.70V/1.75V/1.80V/1.85V) is a programmable buck synchronous DC/DC converter dedicated to the supply of recent and future Flash and SDRAM memories and their associated buses on the application processor I/O section as well as additional memory extension modules such as CF cards, MMCards, Memory Stick, etc. The default voltage is 1.8V. An external pin can select 2.5V output voltage with tuning: 2.6V, 2.4V and 2.3V. The entire cell is optimized for 1.8V. The application processor can change the output voltage as described above via registers accessible by SPI.

The external components needed include a current sensing resistor, a dual PMOS-NMOS, an inductor and an output capacitor.

A low quiescent current mode is implemented when a very low standby current is needed with a parallel voltage regulator.

When the cell is off, the output is in high impedance state.

DC to DC Step Up/ Down 520 mA, 3.3V

The DC to DC step Up/Down 520 mA, 3.3V (dynamically adjustable to 3.0V/3.1V/3.4V) is a boost DC/DC 3.6V converter followed by a linear drop out regulator. It is intended to supply 3.3V I/Os needed in the application (Audio Codec, LCD, Memories).

The external components needed include a current sensing resistor, an NMOS, a Schottky diode, an inductor and an output capacitor.

The default value of the LDO is 3.3V but three other values can be programmed: 3.1V, 3.2V and 3.4V. The entire cell is optimized for 3.3V. The application processor can change the output voltage as described above via registers accessible by SPI.

When the cell is off, the output is pulled to ground.

Power Switch Controller

The power switch controller drives an external PMOS switch to multiplex VDD-PSU from the internal or external battery or USB. The purpose of this cell is to guarantee a sufficient supply for VDD-PSU and to limit voltage drops even during switchover. In-rush current and current flow between the inputs must be avoided.

When this cell is off, VDD-PSU is left in high impedance.

Current Generators

Two accurate current generators allow the measurement of the resistance of two external battery thermistors. The outputs V_{THE1} and V_{THE2} go to the measurement bridge. The

current generators are supplied by V_{SAUV} and controlled by the digital control for use during battery charging.

Temperature Sensor

The temperature sensor voltage output depends linearly on temperature. It is supplied by V_{SAUV} and driven by the digital control. The temperature seen by the sensor is directly related to the chip activity and the power internally dissipated. To get a good indication of the ambient temperature, the software must take into account this offset.

Measurement Bridge/ Multiplexer

The measurement bridge provides adapted voltages of the internal and external batteries, DC/DC converter outputs, USB, VDD-PSU, V_{THE1} and V_{THE2} to the multiplexed input of the serial analog to digital converter.

Analog to Digital Converter

An 8-bit analog to digital converter is integrated into the AT73C203 to give information about voltage and temperature to the application processor via the SPI interface.

Li-Ion/Battery Chargers

The battery chargers both have stand-alone constant current (CC) precharge and microprocessor-controlled CC fast charge as well as top-off mode end-of-charge algorithm.

The digital block controls this cell. All current and voltage settings are programmable via registers.

The charger controller is divided into two similar parts, one for the internal battery and one for the external battery. Each charger multiplexes the source (USB or PSU) and limits the programmable current charge (via sense resistor). An external PMOS and a Schottky diode are needed for each charger.

The application processor must check that the temperature allows charging via the current generator, measurement bridge and ADC.

USIM Voltage Regulator

A regulator is provided to power up the USIM card. It is supplied directly from VDD_PSU. One of two different voltages can be selected:

- 2.8V (50 mA)
- 1.8V (30 mA)

By default, the regulator is in power-down mode.

The pins connected to the USIM (SIM_CLK, SIM_IO, SIM_PWR) must have driver specification according to ETS TS 102 221.

USIM Digital Section

The main part of the USIM digital section is an ISO7816 UART compatible interface.

Reset Generation

A reset is generated via the internal state machine. The timer for this internal reset generator is 150 ms (typical). The application processor can set the AT73C203 to off mode via the POWER_EN pin. The “internal” reset is active at low level.

Another way to generate a reset is to program it through the monitoring function (ADC with measurement bridge and data registers). The “monitoring” reset is active at low level.

A logical AND of the “internal” and the “monitoring” reset drives the reset of the external application processor (NPROC_RESET pin).

Other pins are used to generate separated resets for external “companion” chips such as baseband chips.

NSHUTDOWN forces the AT73C203 internal digital block to the reset state. This turns all the supplies off and then restarts the internal state machine.

Recommended External Components

Table 2. Recommended External Components

Schematic Reference	Component Reference
C1, C3, C5, C8, C16, C17, C18, C19	22 µF ceramic
C2, C4, C6, C7, C9	47 µF tantalum low ESR TPSW476M010R0150 or equivalent
C10, C20	100 nF XR5 ±10%
C11, C13, C22	2.2 µF X5R ± 10%
C12	330 nF X5R ± 10%
C14, C15	10 nF X5R ± 10%
C21	100 pF X5R ± 10%
L1, L4	4.7µH SMT3106-471M (Gowanda®) or equivalent
L2, L3	10 µH SMT3106-102M (Gowanda) or equivalent
D2, D3	Bat54C
D4, D5, D1	MBRA120LT3 (ON Semiconductor®) or equivalent
R1, R2, R4	100 mΩ± 2% 250mW
R3	100 mΩ ± 2% 250mW
R5	220 kΩ ± 1%
R6	200 mΩ ± 2% 50mW
T1, T2, T3	Si4965DY
T4, T5, T8	Si5513DC
T6	Si1400DL
T7, T9, T10	Si8401DL
T11	Si1405DL

Absolute Maximum Ratings

Operating Ambient Temperature.....-40°C to +85°C

Storage Temperature.....-55°C to + 150°C

BAT1_PIO, BAT2_PIO, PSU_PIO, USB_PIO,

USB_CH, BAT1_CH, BAT2_CH, VSW_IN
to ground Pins.....-0.3V to +6.5V

*NOTICE: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Table 3. Recommended Operating Conditions

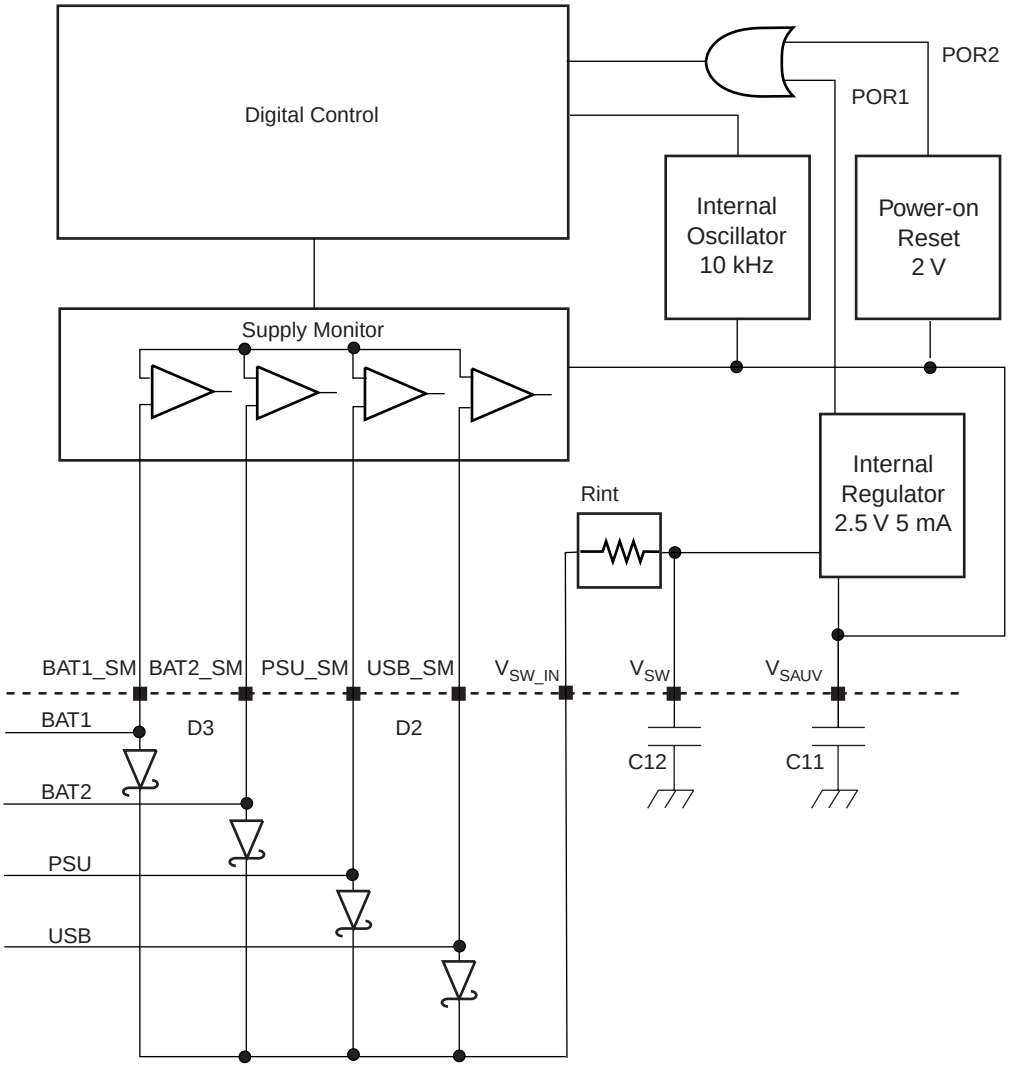
Parameter	Conditions	Min	Max	Unit
Operating Ambient Temperature		-40	+85	°C
Storage Temperature		-55	+150	°C
Signal to Ground Pins	BAT1_PIO, BAT2_PIO, PSU_PIO, USB_PIO, USB_CH, BAT1_CH, BAT2_CH, VSW_IN	-0.3	+5.5	V

System Overview

Startup and Off Mode

Most of the blocks are switched on or off by the digital block. Only the supply monitor, digital control, power-on reset, internal 10kHz oscillator and internal regulator are always on.

Figure 4. Start-up Overview



The system has two modes: Off and Active.

Off Mode: All the cells are off except the supply monitor, digital control, power-on reset, internal 10 kHz oscillator and internal regulator. These blocks are designed to consume very little power in order to achieve an off time of three months from a 600 mA fully charged battery.

Active Mode: The power switch and all the DC/DC controllers are on. All the other cells are controlled by software (via internal registers).

Startup Description

V_{SW_IN} is an analog OR of BAT1, BAT2, USB and PSU implemented using four external Schottky diodes. Schottky diodes are used to minimize the power source to the AT73C203 voltage drop in order to maximize battery life. See Figure 4 on page 13.

When at least one of these supplies are present, V_{SW_IN} tracks the highest voltage of the four inputs. An internal resistor (Rint) between V_{SW} and V_{SW_IN} limits the current flowing through the diodes and C12.

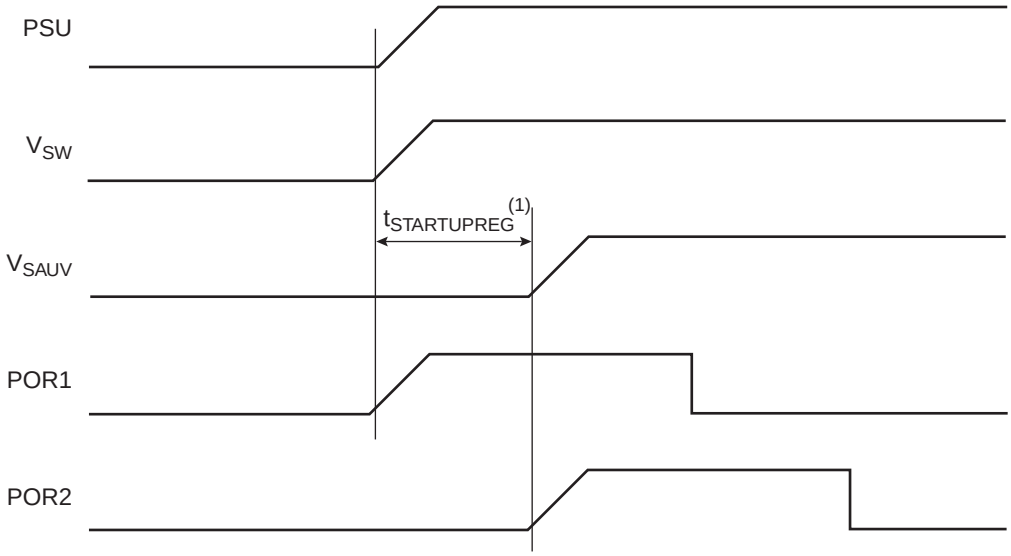
V_{SW} is the input of the internal regulator, which delivers the supply for the digital, oscillators, power-on reset, measurement bridge, reference generator, AD converter, temperature sensor, current generator and supply monitor blocks. Only a small current is supplied from V_{SW_IN} which minimizes the voltage drop across the Schottky diodes.

Power-on-reset Protection

Figure 5 below and Figure 6 on page 15 illustrate the start-up sequence of the AT73C203 under the following conditions.

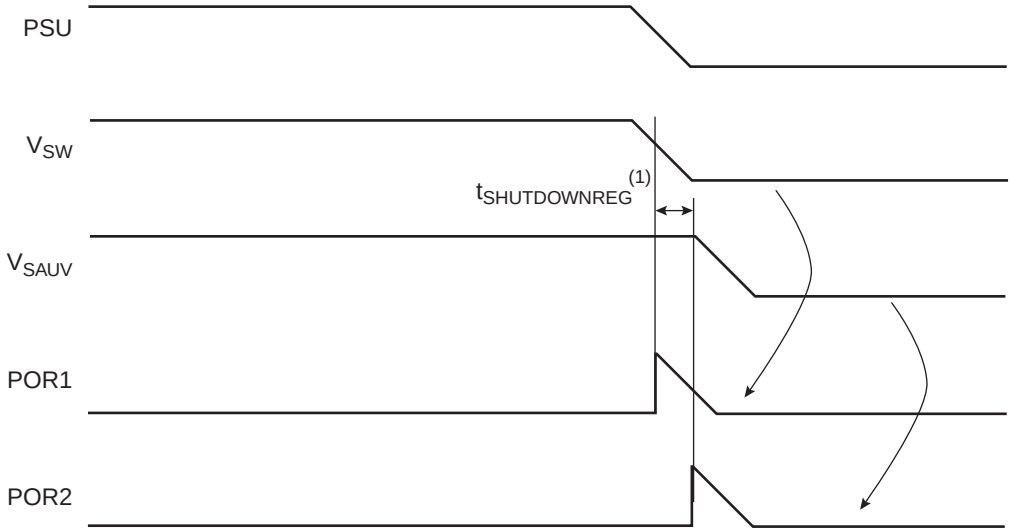
- One supply is present (PSU), the others are connected to ground or not present.
- POR1 supervises V_{SW}. It goes to low level after the start-up time of the internal regulator.
- POR2 supervises V_{SAUV}. It goes to low after V_{SAUV} reaches the correct value for the digital core to run.
- Both V_{SW} and V_{SAUV} must be stable for the digital block to operate correctly.
- The reset for the digital core is the logical OR of POR1 and POR2.

Figure 5. PSU Rising Sequence



Note: 1. $t_{STARTUPREG}$ = Startup time of the internal regulator.

Figure 6. PSU Drop Sequence



Note: 1. $t_{SHUTDOWNREG}$ = Shutdown time of the internal regulator.

State Machine Description

State machines for the start-up and off modes are described in the following pages.

The state machine is completely synchronous to the internal 10 kHz oscillator and all the signals connected to the analog blocks are level shifted as necessary and protected to allow a reliable level.

USB_FST is a digital flag. By default USB_FST is set at 0. If the digital core begins to precharge battery 1 from USB at startup, USB_FST is set to 1 by the internal digital block. The application processor can reset it to 0 via the SPI if needed by setting the USB_FCR flag. This flag acts to avoid digital oscillation when the charge through USB is the start condition. It is also used to inform the application processor that the AT73C203 has charged the internal battery from USB with a minimal amount of charge.

The digital core can also put the AT73C203 via USB_SCR register into a mode where the digital core is off and battery1 is charged (25 mA) through USB up to 4.1V. In this mode (see Figure 10 on page 19) and when battery1 is precharged by USB (see Figure 8 on page 17), a CTN thermistor must be connected to therm1. The CTN thermistor used must be equivalent to the thermistor 103JT-025 from SEMITEC®.

- Temperature to allow precharging through USB: 0°C to 60°C.
- Safety timer for the USB stand alone mode: 1 hour
- Safety timer for the USB Sleep mode: 24 hours

Figure 7. Startup State Machine (1of 3)

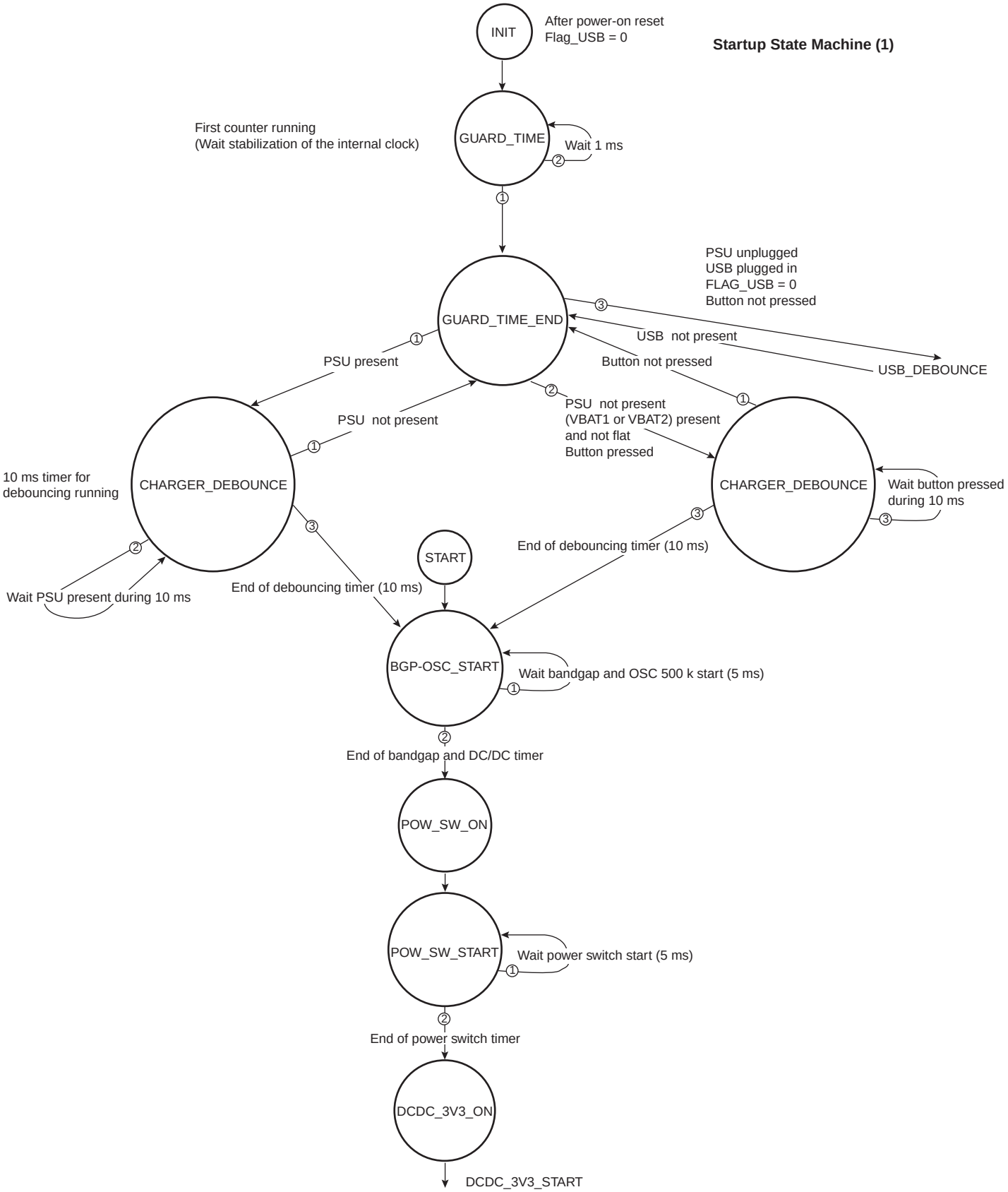


Figure 8. Startup State Machine (2 of 3)

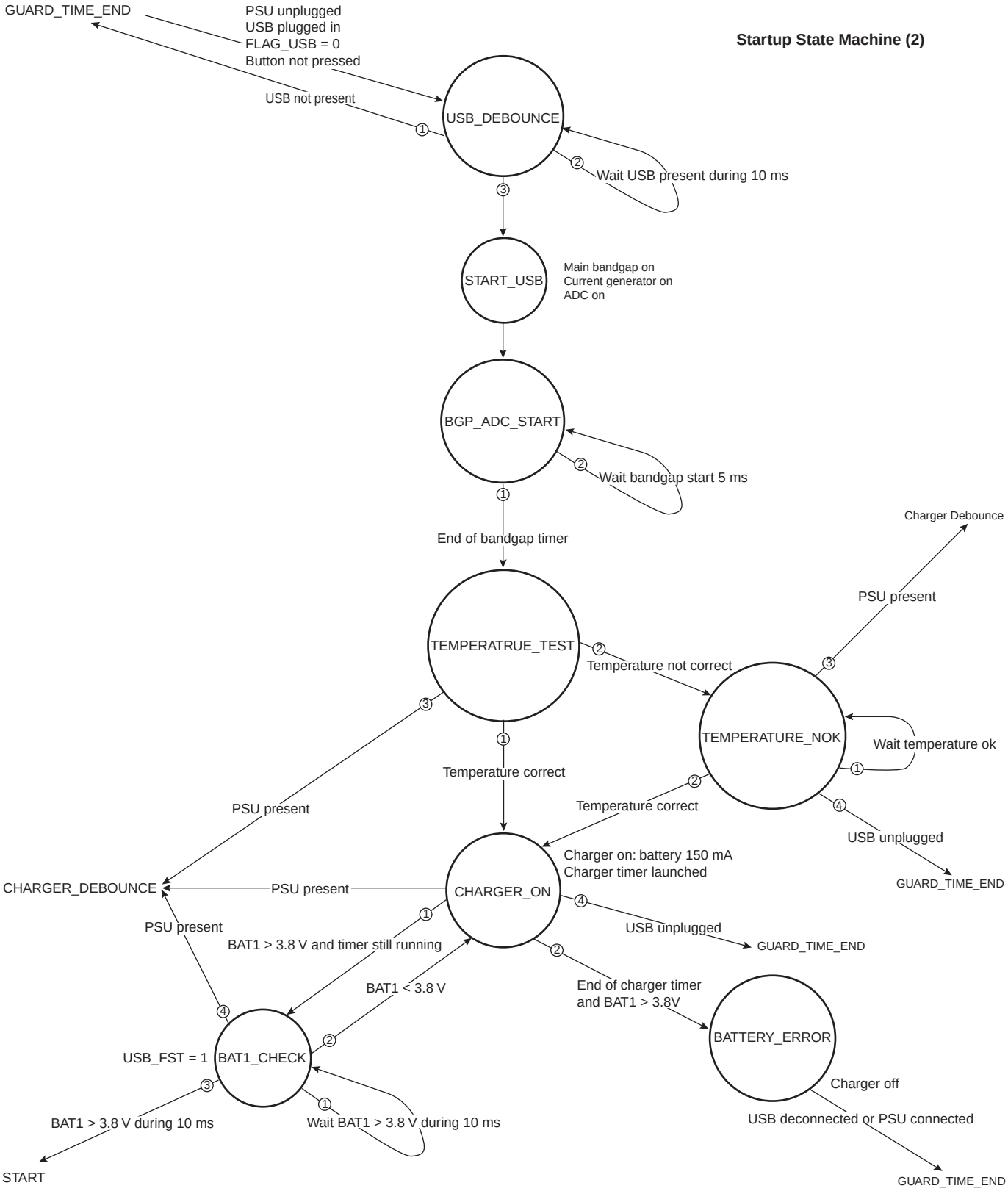


Figure 9. Startup State Machine (3 of 3)

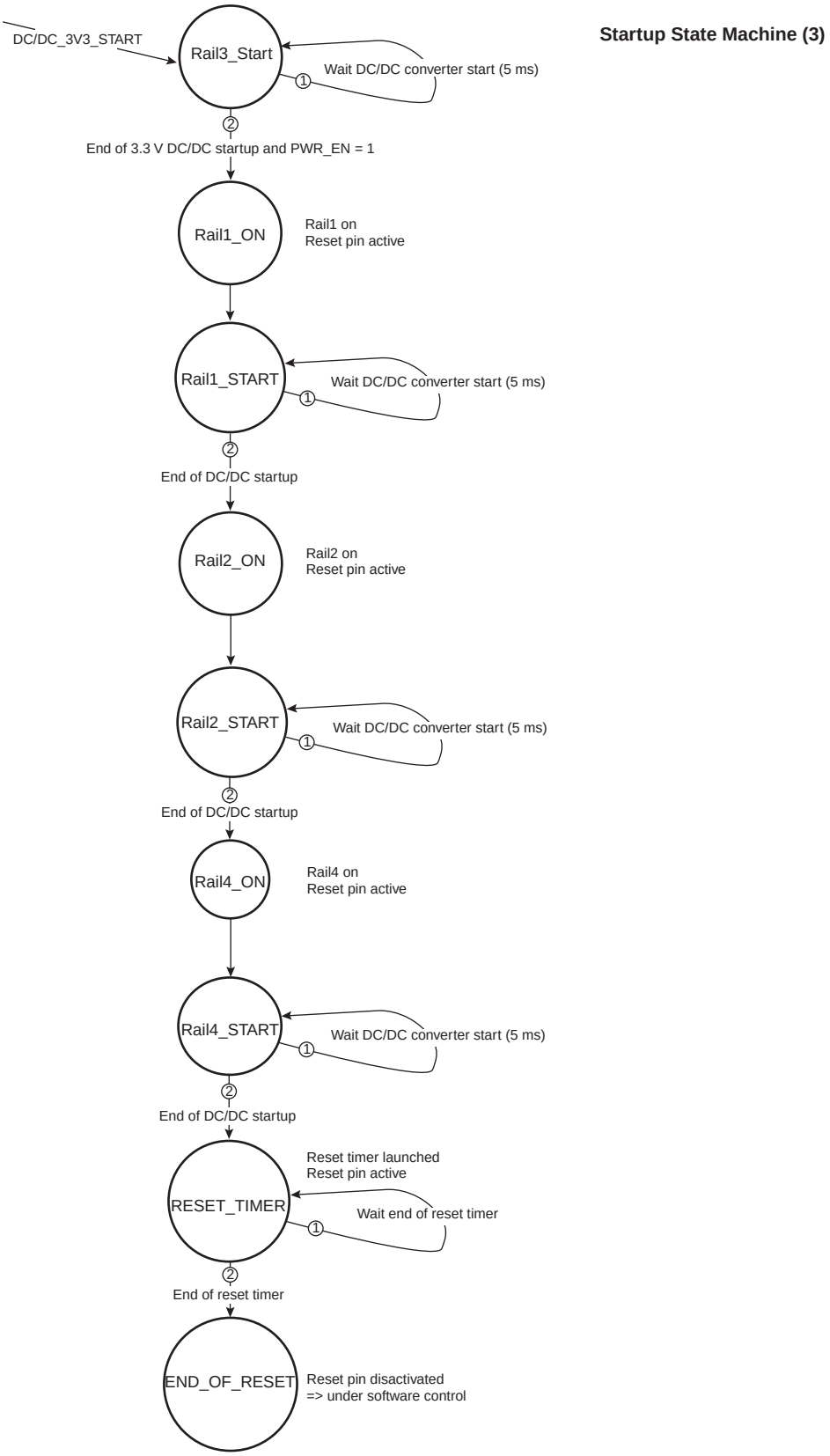


Figure 10. USB Sleep State Machine

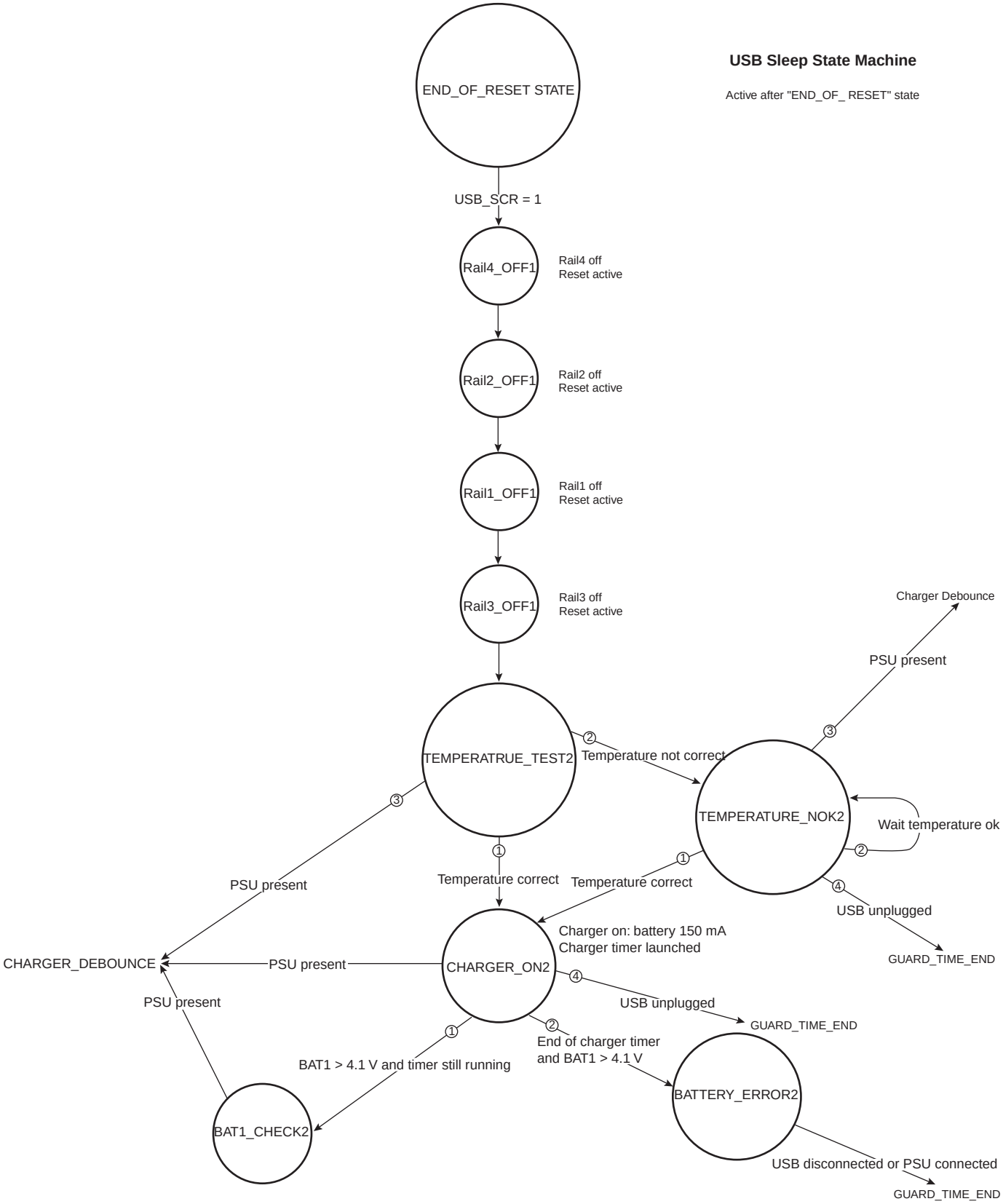
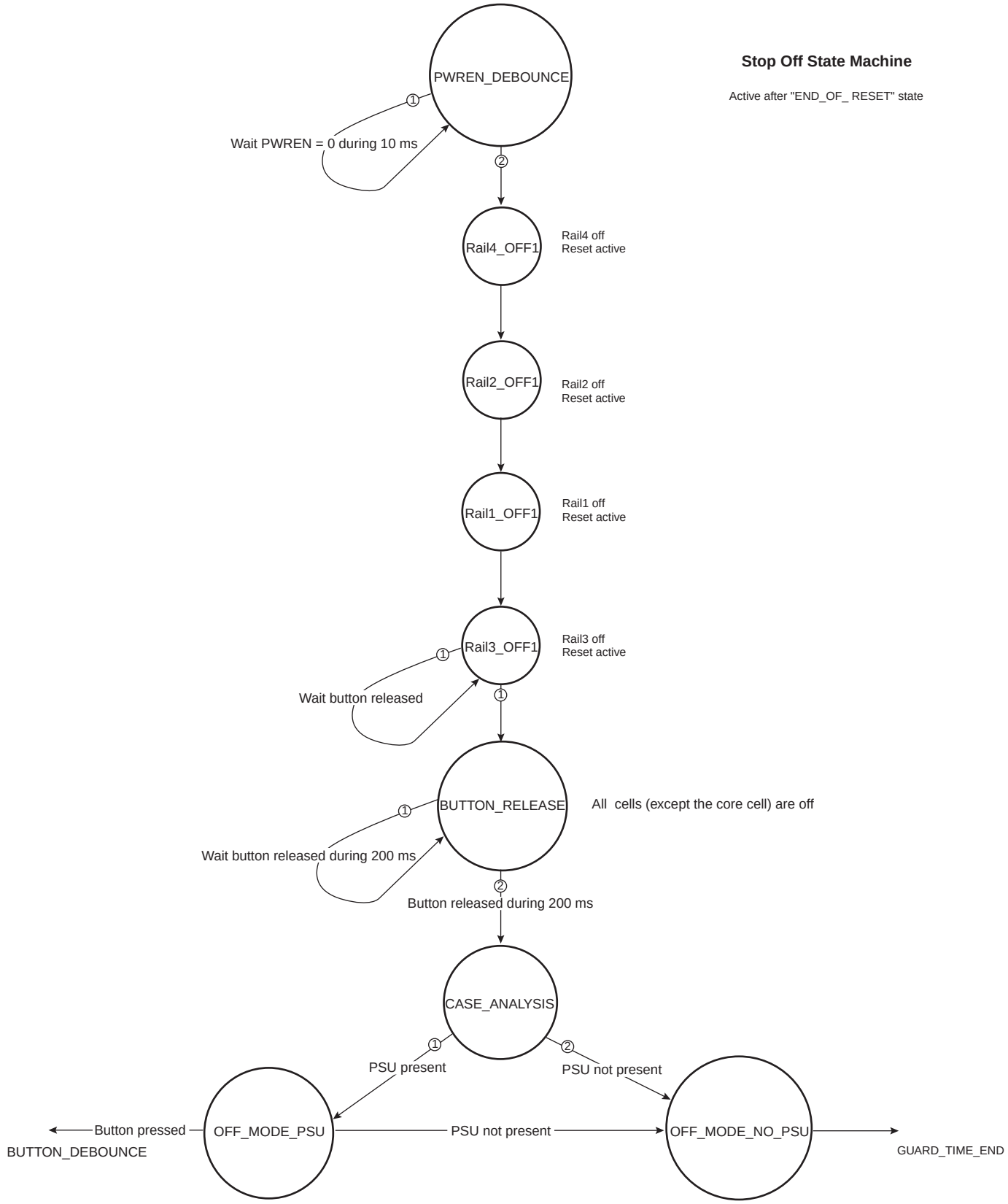


Figure 11. Stop Off State Machine



Reset Generation

A reset is generated via the internal state machine as described in Figure 7 on page 16, Figure 8 on page 17, Figure 9 on page 18 and Figure 11 on page 20. The timer for the internal reset generator is 150 ms (typical).

The application processor can set the AT73C203 to off mode via the POWER_EN pin (Figure 11 on page 20). This “internal” reset is active at low level.

Another way to generate a reset is to program it through the monitoring function. The “monitoring” reset is active at low level.

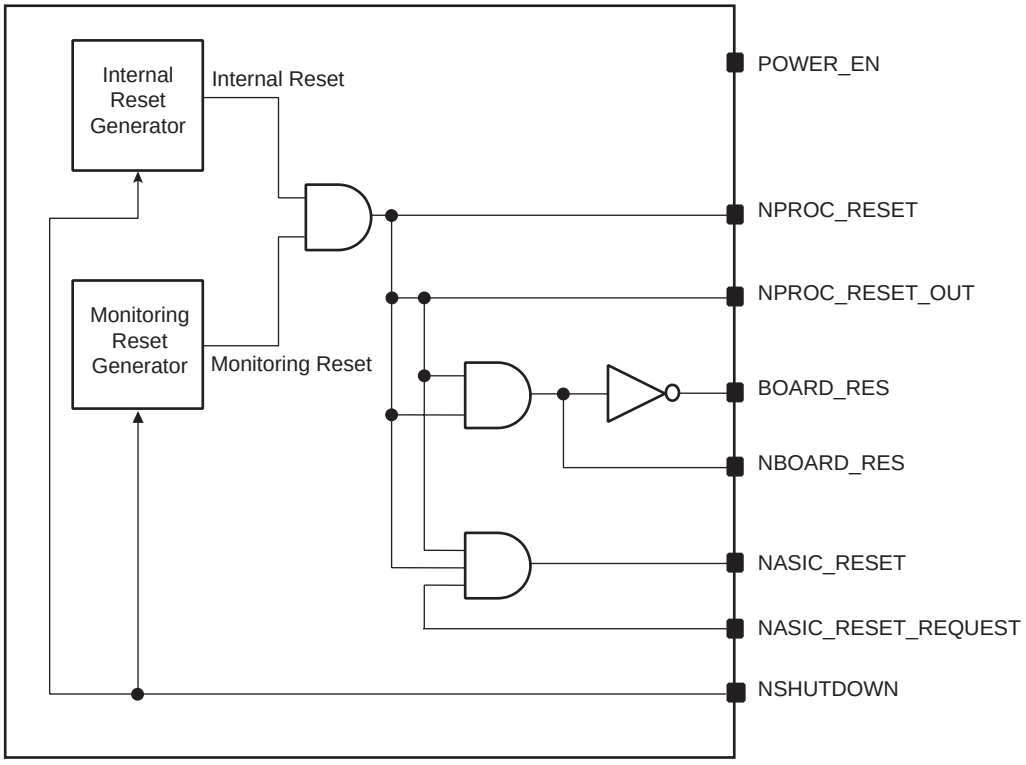
An logical AND of the “internal” reset and the “monitoring” reset drives the reset of the external microprocessor. It is connected to the NPROC_RESET pin and directly drives the external microprocessor.

Additional pins are used to generate separated resets for the baseband chips (see Figure 12 below).

NSHUTDOWN forces the AT73C203 internal digital block to the reset state. This turns all the supplies off and then restarts the internal state machine.

Power-on reset resets the internal state machine. nPROC_RESET resets all other digital parts, with the exception of the USIM interface which is reset via the nBOARD_RES pin.

Figure 12. Reset Generation Architecture



AT73C203 User Interface

Table 4. AT73C203 User Interface

Address	Register	Name	Access	Reset State
General-purpose Registers				
0x48	GP_IDENT	Chip Identification	Read-only	0xA0
0x4B	GP_GPIO_READ	GPIO status	Read-only	-
0x4A	GP_GPIO_WRITE	GPIO control	Read/Write	0x00
0x49	DC_TRIM	Digital rails trimming	Read/Write	0x00
0x4C	PWS_CR	Power switch control	Read/Write	0x00
0x4D	PWS_SR	Power switch status	Read-only	-
0x4F	USB_FST	USB flag status	Read-only	-
0x4E	USB_FCR	USB flag control	Write-only	-
USIM Interface Registers				
0x32	SIM_CSR	USIM channel status	Read-only	-
0x34	SIM_BSR	USIM buffer status	Read-only	0x00
0x36	SIM_MSR	USIM miscellaneous status	Read-only	-
0x37	SIM_IMR1	USIM interrupt mask 1	Read/Write	0x00
0x39	SIM_IMR2	USIM interrupt mask 2	Read/Write	0x00
0x35	SIM_MR	USIM mode	Read/Write	0x80
0x33	SIM_CR	USIM control	Write-only	-
0x3F	SIM_AR	USIM activation	Read/Write	0x00
0x38	SIM_RHR	USIM receiver holding	Read-only	-
0x31	SIM_THR	USIM transmitter holding	Write-only	-
0x3A	SIM_BDR	USIM baud divisor	Read/Write	0x0C
0x3E	SIM_CDR	USIM clock divisor	Read/Write	0x00
0x3B - 0x3C	SIM_RTOR	USIM receiver time-out	Read/Write	0x00
0x3D	SIM_TTGR	USIM transmitter time guard	Read/Write	0x00
0x30	SIM_NER	USIM number of errors	Read-only	0x00
Voltage and Temperature Monitoring Registers				
0x29	MON_CR	Monitoring Control	Read/Write	0x00
0x00	MON_VBAT1_MEAS	Monitoring VBAT1 measure	Read-only	0x00
0x01	MON_VBAT2_MEAS	Monitoring VBAT2 measure	Read-only	0x00
0x02	MON_USB_MEAS	Monitoring USB measure	Read-only	0x00
0x03	MON_VDDPSU_MEAS	Monitoring VDDPSU measure	Read-only	0x00
0x04	MON_VOUT1_MEAS	Monitoring VOUT1 measure	Read-only	0x00
0x05	MON_VOUT2_MEAS	Monitoring VOUT2 measure	Read-only	0x00
0x06	MON_VOUT3_MEAS	Monitoring VOUT3 measure	Read-only	0x00

Table 4. AT73C203 User Interface (Continued)

Address	Register	Name	Access	Reset State
0x07	MON_VOUT4_MEAS	Monitoring VOUT4 measure	Read-only	0x00
0x08	MON_VTE1_MEAS	Monitoring VTE1 measure	Read-only	0x00
0x09	MON_VTE2_MEAS	Monitoring VTE2 measure	Read-only	0x00
0x0A	MON_VTS_MEAS	Monitoring VTS measure	Read-only	0x00
0x16	MON_VBAT1_UNDL	Monitoring VBAT1 under limit	Read/Write	0x00
0x0B	MON_VBAT1_OVL	Monitoring VBAT1 over limit	Read/Write	0x00
0x17	MON_VBAT2_UNDL	Monitoring VBAT2 under limit	Read/Write	0x00
0x0C	MON_VBAT2_OVL	Monitoring VBAT2 over limit	Read/Write	0x00
0x18	MON_USB_ UNDL	Monitoring USB under limit	Read/Write	0x00
0x0D	MON_USB_OVL	Monitoring USB over limit	Read/Write	0x00
0x19	MON_VDDPSU_ UNDL	Monitoring VDDPSU under limit	Read/Write	0x00
0x0E	MON_VDDPSU_OVL	Monitoring VDDPSU over limit	Read/Write	0x00
0x1A	MON_VOUT1_UNDL	Monitoring VOUT1 under limit	Read/Write	0x00
0x0F	MON_VOUT1_OVL	Monitoring VOUT1 over limit	Read/Write	0x00
0x1B	MON_VOUT2_UNDL	Monitoring VOUT2 under limit	Read/Write	0x00
0x10	MON_VOUT2_OVL	Monitoring VOUT2 over limit	Read/Write	0x00
0x1C	MON_VOUT3_UNDL	Monitoring VOUT3 under limit	Read/Write	0x00
0x11	MON_VOUT3_OVL	Monitoring VOUT3 over limit	Read/Write	0x00
0x1D	MON_VOUT4_UNDL	Monitoring VOUT4 under limit	Read/Write	0x00
0x12	MON_VOUT4_OVL	Monitoring VOUT4 over limit	Read/Write	0x00
0x1E	MON_VTE1_UNDL	Monitoring VTE1 under limit	Read/Write	0x00
0x13	MON_VTE1_OVL	Monitoring VTE1 over limit	Read/Write	0x00
0x1F	MON_VTE2_UNDL	Monitoring VTE2 under limit	Read/Write	0x00
0x14	MON_VTE2_OVL	Monitoring VTE2 over limit	Read/Write	0x00
0x20	MON_VTS_UNDL	Monitoring VTS under limit	Read/Write	0x00
0x15	MON_VTS_OVL	Monitoring VTS over limit	Read/Write	0x00
0x21	MON_MR1	Monitoring Interrupt/reset mask 1	Read/Write	0x00
0x22	MON_MR2	Monitoring Interrupt/reset mask 2	Read/Write	0x00
0x23	MON_IR1	Monitoring Interrupt/reset selection 1	Read/Write	0x00
0x24	MON_IR2	Monitoring Interrupt/reset selection 2	Read/Write	0x00
0x25	MON_SR1	Monitoring Status 1	Read-only	0x00
0x26	MON_SR2	Monitoring Status 2	Read-only	0x00
0x27	MON_VTE1_CURR	Monitoring current DAC thermistor 1	Read/Write	0x00
0x28	MON_VTE2_CURR	Monitoring current DAC thermistor 2	Read/Write	0x00
Charge Control Registers				
0x47	CHA_MR	Charge mode	Write-only	0x00

Table 4. AT73C203 User Interface (Continued)

Address	Register	Name	Access	Reset State
0x41	CHA_SR	Charger status	Read-only	0x00
0x40	CHA_CR	Charge control	Write-only	0x00
0x42	CHA_STR_CR	Charger safety timer control	Write-only	0x00
0x43	CHA_STR_SR	Charger safety timer status	Read-only	0x00
0x44	CHA_TMINON	Charger minimum on time	Read/Write	0x00
0x45	CHA_TMINOFF	Charger minimum off time	Read/Write	0x00
0x46	CHA_TR	Charger trimming	Read/Write	0x00

General-purpose Registers

Chip Identification Register

Name: GP_IDENT

Access: Read-only

7	6	5	4	3	2	1	0
ATMEL_ID				VERSION_ID			

- **VERSION_ID: Version Identification**

These four bits correspond to device version.

For the first version, VERSION_ID = 0x0.

- **ATMEL_ID: ATMEL Identification**

These four bits give the company identification.

ATMEL_ID = 0xA

Note that GP_IDENT can only be changed by metal mask.

For 56H05A and 56H05B, GP_IDENT = 0xA0.

For 56H05C, GP_IDENT = 0xA2.

GPIO Status Register

Name: GP_GPIO_READ

Access: Read-only

7	6	5	4	3	2	1	0
-	-	-	-	GPIO_RD_3	GPIO_RD_2	GPIO_RD_1	GPIO_RD_0

- **GPIO_RD_0: Value of ID_BITS0 pin**

0: ID_BITS0 = 0

1: ID_BITS0 = 1

- **GPIO_RD_1: Value of ID_BITS1 pin**

0: ID_BITS1 = 0

1: ID_BITS1 = 1

- **GPIO_RD_2: Value of ID_BITS2 pin**

0: ID_BITS2 = 0

1: ID_BITS2 = 1

- **GPIO_RD_3: Value of ID_BITS3 pin**

0: ID_BITS3 = 0

1: ID_BITS3 = 1

GPIO Control Register

Name: GP_GPIO_WRITE

Access: Read/Write

7	6	5	4	3	2	1	0
GPIO_DO_3	GPIO_DO_2	GPIO_DO_1	GPIO_DO_0	GPIO_OE_3	GPIO_OE_2	GPIO_OE_1	GPIO_OE_0

- **GPIO_OE_0: Output enable for ID_BITS0 pin**

0: ID_BITS0 pin configures as input

1: ID_BITS0 pin configures as output

- **GPIO_OE_1: Output enable for ID_BITS1 pin**

0: ID_BITS1 pin configures as input

1: ID_BITS1 pin configures as output

- **GPIO_OE_2: Output enable for ID_BITS2 pin**

0: ID_BITS2 pin configures as input

1: ID_BITS2 pin configures as output

- **GPIO_OE_3: Output enable for ID_BITS3 pin**

0: ID_BITS3 pin configures as input

1: ID_BITS3 pin configures as output

- **GPIO_DO_0: Output data for ID_BITS0 pin**

0: ID_BITS0 pin sets to 0 (if GPIO_OE_0 = 1)

1: ID_BITS0 pin sets to 1 (if GPIO_OE_0 = 1)

- **GPIO_DO_1: Output data for ID_BITS1 pin**

0: ID_BITS1 pin sets to 0 (if GPIO_OE_1 = 1)

1: ID_BITS1 pin sets to 1 (if GPIO_OE_1 = 1)

- **GPIO_DO_2: Output data for ID_BITS2 pin**

0: ID_BITS2 pin sets to 0 (if GPIO_OE_2 = 1)

1: ID_BITS2 pin sets to 1 (if GPIO_OE_2 = 1)

- **GPIO_DO_3: Output data for ID_BITS3 pin**

0: ID_BITS3 pin sets to 0 (if GPIO_OE_3 = 1)

1: ID_BITS3 pin sets to 1 (if GPIO_OE_3 = 1)

Digital Rail Trimming Register

Name: DC _TRIM

Access: Read/Write

7	6	5	4	3	2	1	0
DC_TRIM_4		DC_TRIM_3		DC_TRIM_2		DC_TRIM_1	

- **DC_TRIM_1: Trimming for rail 1 output voltage**

If SELDC175 = 0:

DC_TRIM_1		
0	0	Rail 1 output voltage = 1.2V (default value)
0	1	Rail 1 output voltage = 1.3V
1	0	Rail 1 output voltage = 1.1V
1	1	Rail 1 output voltage = 1.5V

If SELDC175 = 1:

DC_TRIM_1		
0	0	Rail 1 output voltage = 1.75V (default value)
0	1	Rail 1 output voltage = 1.80V
1	0	Rail 1 output voltage = 1.70V
1	1	Rail 1 output voltage = 1.65V

- **DC_TRIM_2: Trimming for rail 2 output voltage**

If SELDC25 = 0:

DC_TRIM_2		
0	0	Rail 2 output voltage = 1.80V (default value)
0	1	Rail 2 output voltage = 1.85V
1	0	Rail 2 output voltage = 1.75V
1	1	Rail 2 output voltage = 1.70V

If SELDC25 = 1:

DC_TRIM_2		
0	0	Rail 2 output voltage = 2.50V (default value)
0	1	Rail 2 output voltage = 2.60V
1	0	Rail 2 output voltage = 2.40V
1	1	Rail 2 output voltage = 2.30V

- **DC_TRIM_3: Trimming for rail 3 output voltage**

DC_TRIM_3		
0	0	Rail 3 output voltage = 3.3V (default value)
0	1	Rail 3 output voltage = 3.1V
1	0	Rail 3 output voltage = 3.2V
1	1	Rail 3 output voltage = 3.4V

- **DC_TRIM_4: Trimming for rail 4 output voltage**

DC_TRIM_4		
0	0	Rail 4 output voltage = 0.9V (default value)
0	1	Rail 4 output voltage = 1.20V
1	0	Rail 4 output voltage = 0.87V
1	1	Rail 4 output voltage = 1.10V

Power Switch Control Register

Name: PWS _CR (0x4C)

Access: Read/Write

7	6	5	4	3	2	1	0
-	-	-	-	PWS_ENBAT2	PWS_ENBAT1	PWS_FORCE	

With PWS_FORCE, the microprocessor can force selection of an input source. This may be used to test the AT73C203 or by the microprocessor to force use of one of the batteries.

- **PWS_FORCE: Force an input source to be selected**

PWS_FORCE		Input Selected
0	0	Power switch runs automatically (default mode)
0	1	PSU
1	0	Battery 2
1	1	Battery 1

- **PWS_ENBAT1: Reset FLATBAT1 (refer to “Power Switch Status Register” on page 30)**

0: No action (default value)

1: FLATBAT1 is reset to 0

- **PWS_ENBAT2: Reset FLATBAT2 (refer to “Power Switch Status Register” on page 30)**

0: No action (default value)

1: FLATBAT2 is reset to 0

Power Switch Status Register

Name: PWS _SR

Access: Read-only

7	6	5	4	3	2	1	0
-	-	-	-	FLATBAT2	FLATBAT1	PWS_STATUS	

- **PWS_STATUS: Status of the power switch**

PWS_STATUS		Input Selected
0	0	Power switch off or no input selected
0	1	PSU
1	0	Battery 2
1	1	Battery 1

With PWS_STATUS (bits accessible via SPI), the microprocessor can read which supply is currently selected by the AT73C203.

- **FLATBAT1: BAT1 flat threshold indication**

0: Default and reset value

1: Bat1 voltage has reached flat threshold during selection (latched value). Bat1 cannot be used as input source (until reset by the microprocessor)

- **FLATBAT2: BAT2 flat threshold indication**

0: Default and reset value

1: Bat2 voltage has reached flat threshold during selection (latched value). Bat2 cannot be used as input source (until reset by the microprocessor)

USB Flag Status

Name: USB_FST

Access: Read-only

7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	USB_FST

- **USB_FST: USB flag status**

0: USB has not been used to precharge (stand alone mode)

1: USB has been used to precharge (stand alone mode)

Refer to “State Machine Description” on page 15.

USB Flag Control

Name: USB_FCR (0x4E)

Access: Write-only

7	6	5	4	3	2	1	0
-	-	-	-	-	-	USB_SCR	USB_FCR

- **USB_FCR: USB flag control**

0: No action

1: Resets USB_FST to 0

- **USB_SCR: USB sleep control**

0: No action

1: Enter in “USB SLEEP STATE MACHINE”

Refer to “State Machine Description” on page 15.

USIM Interface Registers

Channel Status Register

Name: SIM_CSR (0x32)

Access: Read-only

7	6	5	4	3	2	1	0
-	TXNACK	TXEMPTY	TXRDY	PARE	OVRE	RXFULL	RXRDY

- **RXRDY: Receiver Ready**

0: The receiver FIFO is empty.

1: At least one complete character has been received.

- **RXFULL: Receiver Full**

0: The receiver FIFO is not full.

1: The receiver FIFO is full.

- **OVRE: Overrun Error**

0: No byte has been transferred from the Receive Shift Register to the receiver FIFO when RXFULL was asserted since the last Reset Status Bits command.

1: At least one byte has been transferred from the Receive Shift Register to the receiver FIFO when RXFULL was asserted since the last Reset Status Bits command.

- **PARE: Parity Error**

0: No parity bit has been detected as false since the last Reset Status Bits command.

1: At least one parity bit has been detected as false since the last Reset Status Bits command.

- **TXRDY: Transmitter Ready**

0: The transmitter FIFO is full.

1: The transmitter FIFO is not full.

- **TXEMPTY: Transmitter Empty**

0: There are characters in either the transmitter FIFO or the Transmit Shift Register.

1: There are no characters in either the transmitter FIFO or the Transmit Shift Register. TXEMPTY is 1 after Parity, Stop Bit and Time-guard have been transmitted. TXEMPTY is 1 after stop bit has been sent, or after Time-guard has been sent if SIM_TTGR is not 0.

- **TXNACK: Non Acknowledge**

0: A Non Acknowledge has not been detected during a transmission

1: A Non Acknowledge has been detected during a transmission.

Buffer Status Register

Name: SIM_BSR

Access: Read-only

7	6	5	4	3	2	1	0
TXPTR				RXPTR			

- **RXPTR: Receiver buffer pointer**

Indicates the number of characters waiting to be read in the receiver FIFO. If RXPTR = 15 then if RXFULL is set, there are 16 characters in the FIFO, otherwise there are 15.

- **TXPTR: Transmitter buffer pointer**

Indicates the number of characters waiting to be transmitted from the transmitter FIFO. If TXPTR = 15 then if TXRDY is set, there are 15 characters in the FIFO, otherwise 16.

Miscellaneous Status Register

Name: SIM_MSR

Access: Read-only

7	6	5	4	3	2	1	0
-	-	-	-	-	PRES	ITERATION	TIMEOUT

- **TIMEOUT: Receiver Time-out**

0: There has not been a time-out since the last Start Time-out command or the Time-out Register is 0.

1: There has been a time-out since the last Start Time-out command.

- **ITERATION: Max number of Repetitions Reached**

Note: This bit will operate only in Protocol T: 0.

0: Max number of repetitions has not been reached.

1: Max number of repetitions has been reached.

A repetition consists of transmitted characters or successive NACK.

- **PRES: SIM card presence**

0: The SIM card is not present.

1: The SIM card is present.

Interrupt Mask Register 1

Name: SIM_IMR1 (0x37)

Access: Read/Write

7	6	5	4	3	2	1	0
-	TXNACK	TXEMPTY	TXRDY	PARE	OVRE	RXFULL	RXRDY

- **RXRDY: Enable RXRDY Interrupt**

0: Disables RXRDY Interrupt.

1: Enables RXRDY Interrupt.

- **RXFULL: Enable RXFULL Interrupt**

0: Disables RXFULL Interrupt.

1: Enables RXFULL Interrupt.

- **OVRE: Enable Overrun Error Interrupt**

0: Disables Overrun Error Interrupt.

1: Enables Overrun Error Interrupt.

- **PARE: Enable Parity Error Interrupt**

0: Disables Parity Error Interrupt.

1: Enables Parity Error Interrupt.

- **TXRDY: Enable TXRDY Interrupt**

0: Disables TXRDY Interrupt.

1: Enables TXRDY Interrupt.

- **TXEMPTY: Enable TXEMPTY Interrupt**

0: Disables TXEMPTY Interrupt.

1: Enables TXEMPTY Interrupt.

- **TXNACK: Enable Non Acknowledge Interrupt**

0: Disables Non Acknowledge Interrupt.

1: Enables Non Acknowledge Interrupt

Interrupt Mask Register 2

Name: SIM_IMR2 (0x39)

Access: Read/Write

7	6	5	4	3	2	1	0
-	-	-	TXHALF	RXHALF	PRES	ITERATION	TIMEOUT

- **TIMEOUT: Enable Time-out Interrupt**

0: Disables reception time-out interrupt.

1: Enables reception time-out interrupt.

- **ITERATION: Enable Iteration Interrupt**

Note: This will operate only in Protocol T: 0.

0: Disables ITERATION interrupt.

1: Enables ITERATION interrupt.

- **PRES: Enable Presence Interrupt**

0: Disables card presence interrupt.

1: Enables card presence interrupt.

- **RXHALF: Enable Reception Buffer Half Full Interrupt**

0: Disables reception buffer half full interrupt.

1: Enables reception buffer half full interrupt.

- **TXHALF: Enable Transmission Buffer Half Full Interrupt**

0: Disables transmission buffer half full interrupt.

1: Enables transmission buffer half full interrupt.

Mode Register

Name: SIM_MR (0x35)

Access: Read/Write

7	6	5	4	3	2	1	0
POLARITY	BIT_ORDER	MAX_ITERATION			DSRNACK	IRXNACK	TMODE

- **TMODE: Protocol Mode**

0: Protocol T: 0

1: Protocol T: 1

- **IRXNACK: Inhibit Reception Non Acknowledge**

0: The NACK is generated

1: The NACK is not generated

Note: This bit will be used only in protocol T: 0 receiver.

- **DSRXNACK: Disable Successive Reception NACK**

0: NACK is sent on the IO line as soon as a parity error occurs in the received character (unless IRXNACK is set).

1: Successive parity errors are counted up to the value specified in the MAX_ITERATION field. These parity errors generate a NACK on the IO line. As soon as this value is reached, no additional NACK is sent on the IO line. The flag ITERATION is asserted.

- **MAX_ITERATION: Number of Repetitions**

0 - 7 This will operate in Protocol T: 0 only

- **BIT_ORDER**

0: LSB first (direct convention)

1: MSB first (inverse convention)

- **POLARITY: Polarity**

0: Odd parity (odd number of 1 on character + parity bit) (inverse convention)

1: Even parity (even number of 1 on character + parity bit) (direct convention)

Control Register

Name: SIM_CR

Access: Write-only

7	6	5	4	3	2	1	0
RSTTX	RSTRX	RSTPRES	RETT	RSTNACK	RSTIT	STTO	RSTSTA

- **RSTSTA: Reset Status Bits**

0: No effect.

1: Resets the status bits PARE AND OVRE in the SIM_CSR.

- **STTO: Start Time-out**

0: No effect

1: Start. waiting for a character before clocking the time-out counter.

- **RSTIT: Reset Iterations**

0: No effect.

1: Resets the status bit Iteration.

- **RSTNACK: Reset Non Acknowledge**

0: No effect

1: Resets the status bit TXNACK.

- **RETTO: Rearm Time-out**

0: No effect

1: Restart. Time-out

- **RSTPRES: Reset Presence Interrupt**

0: No effect

1: Reset. SIM card presence interrupt.

- **RSTRX: Reset Receiver**

0: No effect

1: The receiver logic is reset and the receiver FIFO is emptied.

- **RSTTX: Reset Transmitter**

0: No effect

1: The transmitter logic is reset and the transmitter FIFO is emptied.

Activation Register

Name: SIM_AR (0x3F)

Access: Read/Write

7	6	5	4	3	2	1	0
-	-	-	VSEL		ACTIVE	CLKEN	SRESET

- **SRESET: SIM Reset Pin**

0: SIM Reset pin: 0.

1: SIM Reset pin: 1.

- **CLKEN: SIM Clock Enable**

0: SIM clock disabled (grounded).

1: SIM clock enabled.

- **ACTIVE: IO Line Activation**

0: IO line at ground.

1: IO line enabled.

- **VSEL: SIM Voltage Selection**

00: Disabled

01: Disabled

10: Regulator output equals 1.8V

11: Regulator output equals 2.8V

Receiver Holding Register

Name: SIM_RHR (0x38)

Access: Read-only

7	6	5	4	3	2	1	0
RHR							

First character received if RXRDY is set.

Transmitter Holding Register

Name: SIM_THR (0x31)

Access: Write-only

7	6	5	4	3	2	1	0
THR							

Next character to be transmitted. If transmitter FIFO is full, the last character is overwritten.

Baud Divisor Register

Name: SIM_BDR (0x3A)

Access: Read/Write

7	6	5	4	3	2	1	0
-	BDR						

The baud rate = f/(div1 x div2) where f is the SIM clock frequency.

div1 is coded on BDR[6].

BDR[6]	**0**	**1**
div1	31	32

div2 is coded on BDR[5:0].

BDR[5:0]	**0**	**1 - 63**
div2	64	BDR[5:0]

BDR reset value = b0001100. Initial baud rate = 372.

Clock Divisor Register

Name: SIM_CDR (0x3E)

Access: Read/Write

7	6	5	4	3	2	1	0
-	-	-	-	CDR			

The SIM clock is generated through a programmable divider. The division factor can be modified in this register.

CDR[3:0]	**0000**	**0001 to 1111**
Clock division factor	No clock	CDR[3:0]

CDR reset value = 0000.

Receiver Time-out Register

Name: SIM_RTOR (0x3B and 0x3C)

Access: Read/Write

15	14	13	12	11	10	9	8
RTOR							
7	6	5	4	3	2	1	0
RTOR							

0: Disables the RX Time-out function.

1 - 65535: The Time-out counter is loaded with RTOR (16 bits) when the Start Time-out command is given or when each new data character is received (after reception has started).

Transmitter Time Guard Register

Name: SIM_TTGR (0x3D)

Access: Read/Write

7	6	5	4	3	2	1	0
TTGR							

Time-guard duration = TG x Bit Period

0: Disables the TX Time-guard function.

1 - 255: IO line is inactive high after the transmission of each character for the time-guard duration.

Number of Errors Register

Name: SIM_NER (0x30)

Access: Read-only

7	6	5	4	3	2	1	0
NER							

NB_ERRORS: Error number during transfers

This 8-bit register presents the total amount of errors that occurred during a transfer. It is a read-only register and it is reset by reading the register.

Voltage and Temperature Monitoring Registers

Control Register

Name: MON_CR (0x29)

Access: Read/Write

7	6	5	4	3	2	1	0
-	-	-	-	-	-	IT_RESET	MON_ON

- **MON_ON: Enable bit of the monitoring function**

0: Monitoring function disabled

1: Monitoring function enabled

- **IT_RESET: Reset of the status register**

0: No action

1: Reset the status registers MON_SR1 and MON_SR2

VBAT1 Measure Register

Name: MON_VBAT1_MEAS (0x00)

Access: Read-only

7	6	5	4	3	2	1	0
MON_VBAT1_MEAS							

VBAT2 Measure Register

Name: MON_VBAT2_MEAS (0x01)

Access: Read-only

7	6	5	4	3	2	1	0
MON_VBAT2_MEAS							

USB Measure Register

Name: MON_USB_MEAS (0x02)

Access: Read-only

7	6	5	4	3	2	1	0
MON_USB_MEAS							

VDDPSU Measure Register

Name: MON_VDDPSU_MEAS (0x03)

Access: Read-only

7	6	5	4	3	2	1	0
MON_VDDPSU_MEAS							

VOUT1 Measure Register

Name: MON_VOUT1_MEAS (0x04)

Access: Read-only

7	6	5	4	3	2	1	0
MON_VOUT1_MEAS							

VOUT2 Measure Register

Name: MON_VOUT2_MEAS (0x05)

Access: Read-only

7	6	5	4	3	2	1	0
MON_VOUT2_MEAS							

VOUT3 Measure Register

Name: MON_VOUT3_MEAS (0x06)

Access: Read-only

7	6	5	4	3	2	1	0
MON_VOUT3_MEAS							

VOUT4 Measure Register

Name: MON_VOUT4_MEAS (0x07)

Access: Read-only

7	6	5	4	3	2	1	0
MON_VOUT4_MEAS							

VTE1 Measure Register

Name: MON_VTE1_MEAS (0x08)

Access: Read-only

7	6	5	4	3	2	1	0
MON_VTE1_MEAS							

VTE2 Measure Register

Name: MON_VTE2_MEAS (0x09)

Access: Read-only

7	6	5	4	3	2	1	0
MON_VTE2_MEAS							

VTS Measure Register

Name: MON_VTS_MEAS (0x0A)

Access: Read-only

7	6	5	4	3	2	1	0
MON_VTS_MEAS							

VBAT1 Under Limit Register

Name: MON_VBAT1_UNDL (0x16)

Access: Read/write

7	6	5	4	3	2	1	0
MON_VBAT1_UNDL							

VBAT1 Over Limit Register

Name: MON_VBAT1_OVL (0x1B)

Access: Read/write

7	6	5	4	3	2	1	0
MON_VBAT1_OVL							

VBAT2 Under Limit Register

Name: MON_VBAT2_UNDL (0x17)

Access: Read/write

7	6	5	4	3	2	1	0
MON_VBAT2_UNDL							

VBAT2 Over Limit Register

Name: MON_VBAT2_OVL (0x0C)

Access: Read/write

7	6	5	4	3	2	1	0
MON_VBAT2_OVL							

USB Under Limit Register

Name: MON_USB_UNDL (0x18)

Access: Read/write

7	6	5	4	3	2	1	0
MON_USB_UNDL							

USB Over Limit Register

Name: MON_USB_OVL (0x1D)

Access: Read/write

7	6	5	4	3	2	1	0
MON_USB_OVL							

VDDPSU Under Limit Register

Name: MON_VDDPSU_UNDL (0x19)

Access: Read/write

7	6	5	4	3	2	1	0
MON_VDDPSU_UNDL							

VDDPSU Over Limit Register

Name: MON_VDDPSU_OVL (0x0E)

Access: Read/write

7	6	5	4	3	2	1	0
MON_VDDPSU_OVL							

VOUT1 Under Limit Register

Name: MON_VOUT1_UNDL (0x1A)

Access: Read/write

7	6	5	4	3	2	1	0
MON_VOUT1_UNDL							

VOUT1 Over Limit Register

Name: MON_VOUT1_OVL (0x1F)

Access: Read/write

7	6	5	4	3	2	1	0
MON_VOUT1_OVL							

VOUT2 Under Limit Register

Name: MON_VOUT2_UNDL (0x1B)

Access: Read/write

7	6	5	4	3	2	1	0
MON_VOUT2_UNDL							

VOUT2 Over Limit Register

Name: MON_VOUT2_OVL (0x10)

Access: Read/write

7	6	5	4	3	2	1	0
MON_VOUT2_OVL							

VOUT3 Under Limit Register

Name: MON_VOUT3_UNDL (0x1C)

Access: Read/write

7	6	5	4	3	2	1	0
MON_VOUT3_UNDL							

VOUT3 Over Limit Register

Name: MON_VOUT3_OVL (0x11)

Access: Read/write

7	6	5	4	3	2	1	0
MON_VOUT3_OVL							

VOUT4 Under Limit Register

Name: MON_VOUT4_UNDL (0x1D)

Access: Read/write

7	6	5	4	3	2	1	0
MON_VOUT4_UNDL							

VOUT4 Over Limit Register

Name: MON_VOUT4_OVL (0x12)

Access: Read/write

7	6	5	4	3	2	1	0
MON_VOUT4_OVL							

VTE1 Under Limit Register

Name: MON_VTE1_UNDL (0x1E)

Access: Read/write

7	6	5	4	3	2	1	0
MON_VTE1_UNDL							

VTE1 Over Limit Register

Name: MON_VTE1_OVL (0x13)

Access: Read/write

7	6	5	4	3	2	1	0
MON_VTE1_OVL							

VTE2 Under Limit Register

Name: MON_VTE2_UNDL (0x1F)

Access: Read/write

7	6	5	4	3	2	1	0
MON_VTE2_UNDL							

VTE2 Over Limit Register

Name: MON_VTE2_OVL (0x14)

Access: Read/write

7	6	5	4	3	2	1	0
MON_VTE2_OVL							

VTS Under Limit Register

Name: MON_VTS_UNDL (0x20

Access: Read/write

7	6	5	4	3	2	1	0
MON_VTS_UNDL							

VTS Over Limit Register

Name: MON_VTS_OVL (0x15)

Access: Read/write

7	6	5	4	3	2	1	0
MON_VTS_OVL							

Interrupt/ Reset Mask Register 1

Name: MON_MR1 (0x21)

Access: Read/Write

7	6	5	4	3	2	1	0
VOUT4	VOUT3	VOUT2	VOUT1	VDDPSU	USB	VBAT2	VBAT1

- **VBAT1: Enable VBAT1 Interrupt or Reset**

0: Disables VBAT1 interrupt or global reset.

1: Enables VBAT1 interrupt or global reset.

- **VBAT2: Enable VBAT2 Interrupt**

0: Disables VBAT2 interrupt or global reset.

1: Enables VBAT2 interrupt or global reset.

- **USB: Enable USB Interrupt**

0: Disables USB interrupt or global reset.

1: Enables USB interrupt or global reset.

- **VDDPSU: Enable VDDPSU Interrupt**

0: Disables VDDPSU interrupt or global reset.

1: Enables VDDPSU interrupt or global reset.

- **VOUT1: Enable VOUT1 Interrupt**

0: Disables VOUT1 interrupt or global reset.

1: Enables VOUT1 interrupt or global reset.

- **VOUT2: Enable VOUT2 Interrupt**

0: Disables VOUT2 interrupt or global reset.

1: Enables VOUT2 interrupt or global reset.

- **VOUT3: Enable VOUT3 Interrupt**

0: Disables VOUT3 interrupt or global reset.

1: Enables VOUT3 interrupt or global reset.

- **VOUT4: Enable VOUT4 Interrupt**

0: Disables VOUT4 interrupt or global reset.

1: Enables VOUT4 interrupt or global reset.

Interrupt/ Reset Mask Register 2

Name: MON_MR2 (0x22)

Access: Read/Write

7	6	5	4	3	2	1	0
-	VOUT4COMP	VOUT3COMP	VOUT2COMP	VOUT1COMP	VTS	VTE2	VTE1

- **VTE1: Enable VTE1 Interrupt or Reset**

0: Disables VTE1 interrupt or global reset.

1: Enables VTE1 interrupt or global reset.

- **VTE2: Enable VTE2 Interrupt**

0: Disables VTE2 interrupt or global reset.

1: Enables VTE2 interrupt or global reset.

- **VTS: Enable VTS Interrupt**

0: Disables VTS interrupt or global reset.

1: Enables VTS interrupt or global reset.

- **VOUT1COMP: Enable VOUT1COMP Interrupt or Reset**

0: Disables VOUT1COMP interrupt or global reset.

1: Enables VOUT1COMP interrupt or global reset.

- **VOUT2COMP: Enable VOUT2COMP Interrupt or Reset**

0: Disables VOUT2COMP interrupt or global reset.

1: Enables VOUT2COMP interrupt or global reset.

- **VOUT3COMP: Enable VOUT3COMP Interrupt or Reset**

0: Disables VOUT3COMP interrupt or global reset.

1: Enables VOUT3COMP interrupt or global reset.

- **VOUT4COMP: Enable VOUT4COMP Interrupt or Reset**

0: Disables VOUT4COMP interrupt or global reset.

1: Enables VOUT4COMP interrupt or global reset.

Interrupt/ Reset Selection Register 1

Name: MON_IR1 (0x23)

Access: Read/Write

7	6	5	4	3	2	1	0
VOUT4	VOUT3	VOUT2	VOUT1	VDDPSU	USB	VBAT2	VBAT1

- **VBAT1: Select for VBAT1 Interrupt or Reset**

0: Interrupt selected for VBAT1

1: Global reset selected for VBAT1.

- **VBAT2: Select for VBAT2 Interrupt or Reset**

0: Interrupt selected for VBAT2

1: Global reset selected for VBAT2.

- **USB: Select for USB Interrupt or Reset**

0: Interrupt selected for USB

1: Global reset selected for USB.

- **VDDPSU: Select for VDDPSU Interrupt or Reset**

0: Interrupt selected for VDDPSU

1: Global reset selected for VDDPSU.

- **VOUT1: Select for VOUT1 Interrupt or Reset**

0: Interrupt selected for VOUT1

1: Global reset selected for VOUT1.

- **VOUT2: Select for VOUT2 Interrupt or Reset**

0: Interrupt selected for VOUT2

1: Global reset selected for VOUT2.

- **VOUT3: Select for VOUT3 Interrupt or Reset**

0: Interrupt selected for VOUT3

1: Global reset selected for VOUT3.

- **VOUT4: Select for VOUT4 Interrupt or Reset**

0: Interrupt selected for VOUT4

1: Global reset selected for VOUT4.

Interrupt/ Reset Selection Register 2

Name: MON_IR2 (0x24)

Access: Read/Write

7	6	5	4	3	2	1	0
-	VOUT4COMP	VOUT3COMP	VOUT2COMP	VOUT1COMP	VTS	VTE2	VTE1

- **VTE1: Select for VTE1 Interrupt or Reset**

0: Interrupt selected for VTE1

1: Global reset selected for VTE1.

- **VTE2: Select for VTE2 Interrupt or Reset**

0: Interrupt selected for VTE2

1: Global reset selected for VTE2.

- **VTS: Select for VTS Interrupt or Reset**

0: Interrupt selected for VTS

1: Global reset selected for VTS.

- **VOUT1COMP: Select for VOUT1COMP Interrupt or Reset**

0: Interrupt selected for VOUT1COMP

1: Global reset selected for VOUT1COMP.

- **VOUT2COMP: Select for VOUT2COMP Interrupt or Reset**

0: Interrupt selected for VOUT2COMP

1: Global reset selected for VOUT2COMP.

- **VOUT3COMP: Select for VOUT3COMP Interrupt or Reset**

0: Interrupt selected for VOUT3COMP

1: Global reset selected for VOUT3COMP.

- **VOUT4COMP: Select for VOUT4COMP Interrupt or Reset**

0: Interrupt selected for VOUT4COMP

1: Global reset selected for VOUT4COMP.

Status Register 1

Name: MON_SR1 (0x25)

Access: Read-only

7	6	5	4	3	2	1	0
VOUT4	VOUT3	VOUT2	VOUT1	VDDPSU	USB	VBAT2	VBAT1

- **VBAT1: VBAT1 Error**

0 = No out-of-limit event on VBAT1 since the last reset.

1 = An out-of-limit event on VBAT1 has occurred since the last reset.

- **VBAT2: VBAT2 Error**

0: No out-of-limit event on VBAT2 since the last reset.

1: An out-of-limit event on VBAT2 has occurred since the last reset.

- **USB: US Error**

0: No out-of-limit event on USB since the last reset.

1: An out-of-limit event on USB has occurred since the last reset.

- **VDDPSU: VDDPSU Error**

0: No out-of-limit event on VDDPSU since the last reset.

1: An out-of-limit event on VDDPSU has occurred since the last reset.

- **VOUT1: VOUT1 Error**

0: No out-of-limit event on VOUT1 since the last reset.

1: An out-of-limit event on VOUT1 has occurred since the last reset.

- **VOUT2: VOUT2 Error**

0: No out-of-limit event on VOUT2 since the last reset.

1: An out-of-limit event on VOUT2 has occurred since the last reset.

- **VOUT3: VOUT3 Error**

0: No out-of-limit event on VOUT3 since the last reset.

1: An out-of-limit event on VOUT3 has occurred since the last reset.

- **VOUT4: VOUT4 Error**

0: No out-of-limit event on VOUT4 since the last reset.

1: An out-of-limit event on VOUT4 has occurred since the last reset.

Status Register 2

Name: MON_SR2 (0x26)

Access: Read-only

7	6	5	4	3	2	1	0
-	VOUT4COMP	VOUT3COMP	VOUT2COMP	VOUT1COMP	VTS	VTE2	VTE1

- **VTE1: VTE1 Error**

0: No out-of-limit event on VTE1 since the last reset.

1: An out-of-limit event on VTE1 has occurred since the last reset

- **VTE2: VTE2 Error**

0: No out-of-limit event on VTE2 since the last reset.

1: An out-of-limit event on VTE2 has occurred since the last reset

- **VTS: VTS Error**

0: No out-of-limit event on VTS since the last reset.

1: An out-of-limit event on VTS has occurred since the last reset

- **VOUT1COMP: VOUT1COMP Error**

0: No out-of-limit event on VOUT1COMP since the last reset.

1: An out-of-limit event on VOUT1COMP has occurred since the last reset

- **VOUT2COMP: VOUT2COMP Error**

0: No out-of-limit event on VOUT2COMP since the last reset.

1: An out-of-limit event on VOUT2COMP has occurred since the last reset

- **VOUT3COMP: VOUT3COMP Error**

0: No out-of-limit event on VOUT3COMP since the last reset.

1: An out-of-limit event on VOUT3COMP has occurred since the last reset

- **VOUT4COMP: VOUT4COMP Error**

0: No out-of-limit event on VOUT4COMP since the last reset.

1: An out-of-limit event on VOUT4COMP has occurred since the last reset

Current DAC Thermistor 1 Register

Name: MON_VTE1_CURR (0x27)

Access: Read/Write

7	6	5	4	3	2	1	0
-	VTE1ON	VTE1CURR					

- **VTE1CURR: Current programming for thermistor 1**

See Table 5 on page 57.

- **VTE1ON: Enable current DAC for thermistor 1**

0: Disables current DAC for thermistor 1: THERM1 is in high impedance mode

1: Enables current DAC for thermistor 1

Current DAC Thermistor 2 Register

Name: MON_VTE2_CURR (0x28)

Access: Read/Write

7	6	5	4	3	2	1	0
-	VTE2ON	VTE2CURR					

- **VTE2CURR: Current programming for thermistor 2**

See Table 5 on page 57.

- **VTE2ON: Enable current DAC for thermistor 2**

0: Disables current DAC for thermistor 2: THERM1 is in high impedance mode

1: Enables current DAC for thermistor 2

Table 5. Current Source Control (VTExON = 1, x = 1 or 2)

	VTExCURR<5:0> x = 1 or 2	Typical Output Current (mA)		VTExCURR<5:0> x = 1 or 2	Typical Output Current (mA)
0	000000	567	12	001100	459
1	000001	558	13	001101	450
2	000010	549	14	001110	441
3	000011	540	15	001111	432
4	000100	531	16	010000	423
5	000101	522	17	010001	414
6	000110	513	18	010010	405
7	000111	504	19	010011	396
8	001000	495	20	010100	387
9	001001	486	21	010101	378
10	001010	477	22	010110	369
11	001011	468	23	010111	360

Table 5. Current Source Control (VTExON = 1, x = 1 or 2) (Continued)

	VTExCURR<5:0> x = 1 or 2	Typical Output Current (mA)		VTExCURR<5:0> x = 1 or 2	Typical Output Current (mA)
24	011000	351	44	101100	171
25	011001	342	45	101101	162
26	011010	333	46	101110	153
27	011011	324	47	101111	144
28	011100	315	48	110000	135
29	011101	306	49	110001	126
30	011110	297	50	110010	117
31	011111	288	51	110011	108
32	100000	279	52	110100	99
33	100001	270	53	110101	90
34	100010	261	54	110110	81
35	100011	252	55	110111	72
36	100100	243	56	111000	63
37	100101	234	57	111001	54
38	100110	225	58	111010	45
39	100111	216	59	111011	36
40	101000	207	60	111100	27
41	101001	198	61	111101	18
42	101010	189	62	111110	9
43	101011	180	63	111111	0

Charge Control Registers

Charger Mode Register

Name: CHA_MR (0x47)

Access: Write-only

7	6	5	4	3	2	1	0
	CHA_CURR		CHA_USB_PSU	CHA_PH			

- **CHA_PH: Charger phase control**

0: Sets the Charger control off.

1: Sets Battery1 to pre-conditioning charge phase.

2: Sets Battery2 to pre-conditioning charge phase.

3: Sets Battery1 and Battery2 to pre-conditioning charge phase.

4: Sets Battery1 to fast charge phase.

5: Sets Battery2 to fast charge phase.

6: Sets Battery1 to “pulsed” charge phase.

7: Sets Battery2 to “pulsed” charge phase.

8: Sets Battery1 to fast charge phase and Battery 2 to pre-conditioning charge phase.

9: Sets Battery2 to fast charge phase and Battery 1 to pre-conditioning charge phase.

A: Sets Battery1 to “pulsed” charge phase and Battery 2 to pre-conditioning charge phase.

B: Sets Battery2 to “pulsed” charge phase and Battery 1 to pre-conditioning charge phase.

C: Not used

D: Not used

E: Not used

F: Not used

- **CHA_USB_PSU: Charger USB/PSU selection**

0: PSU is selected.

1: USB is selected.

- **CHA_CURR: Charger current control**

0: Sets the current to 100mA.

1: Sets the current to 200mA.

2: Sets the current to 300mA.

3: Sets the current to 500mA.

Charger Status Register

Name: CHA_SR (0x41)

Access: Read-only

7	6	5	4	3	2	1	0
CH_ST_TIMER	CHA_CURR		CHA_USB_PSU	CHA_PH			

- **CHA_PH: Charger phase control**

0: The Charger control is off.

1: Battery1 in pre-conditioning charge phase.

2: Battery2 in pre-conditioning charge phase.

3: Battery1 and Battery2 in pre-conditioning charge phase.

4: Battery1 in fast charge phase.

5: Battery2 in fast charge phase.

6: Battery1 in “pulsed” charge phase.

7: Battery2 in “pulsed” charge phase.

8: Battery1 in fast charge phase and Battery 2 in pre-conditioning charge phase.

9: Battery2 in fast charge phase and Battery 1 in pre-conditioning charge phase.

A: Battery1 in “pulsed” charge phase and Battery 2 in pre-conditioning charge phase.

B: Battery2 in “pulsed” charge phase and Battery 1 in pre-conditioning charge phase.

C: Not used

D: Not used

E: Not used

F: Not used

- **CHA_USB_PSU: Charger USB/PSU selection**

0: PSU selected.

1: USB selected.

- **CHA_CURR: Charger current control**

0: Current selected: 100mA.

1: Current selected: 200mA.

2: Current selected: 300mA.

3: Current selected: 500mA.

- **CHA_ST_TIMER: Charger safety timer status**

0: No interrupt or timer disabled.

1: An interrupt (end of timer) has occurred.

Charger Control Register

Name: CHA_CR (0x40)

Access: Write-only

7	6	5	4	3	2	1	0
-	-	-	-	RES_CHA_IT	RES_TIM_IT	STA_TIM	REA_WDOG

- **REA_WDOG: Rearm the watchdog**

0: No action

1: Rearms the watchdog

- **STA_TIM: Start the safety timer**

0: No action

1: Starts the safety timer

- **RES_TIM_IT: Reset the safety timer interrupt**

0: No action

1: Resets the safety timer interrupt

- **RES_CHA_IT: Reset the charger interrupt**

0: No action

1: Resets the charger interrupt

Charger Safety Timer Control Register

Name: CHA_STR_CR (0x42)

Access: Write-only

7	6	5	4	3	2	1	0
CHA_STR							

- **CHA_STR_CR: Charger safety timer control register**

Safety timer = CHA_STR_PR x 210 sec.

Writing 0x00 in this register disables the safety timer. Thus the safety timer can be programmed from 0 to 53477 sec. (14h 51min).

Charger Safety Timer Status Register

Name: CHA_STR_SR (0x43)

Access: Read-only

7	6	5	4	3	2	1	0
CHA_STR_SR							

- **CHA_STR_SR: Charger safety timer register**

Safety timer = CHA_STR_SR x 210 sec. It gives the status of the internal counter from 0 to 53477 sec. (14h 51min).

Charger Minimum On Time Register

Name: CHA_TMINON (0x44)

Access: Read/Write

7	6	5	4	3	2	1	0
CHA_TMINON							

- **CHA_TMINON: Minimum on time for pulsed charge phase**

Minimum on-time = CHA_TMINON *2 ms

Thus the minimum on-time can be tuned from 0 to 510 ms.

Charger Minimum Off Time Register

Name: CHA_TMINOFF (0x45)

Access: Read/Write

7	6	5	4	3	2	1	0
CHA_TMINOFF							

- **CHA_TMINOFF: Minimum on time for pulsed charge phase**

Minimum on-time = CHA_TMINOFF *2 ms

Thus the minimum off-time can be tuned from 0 to 510 ms.

Charger Trim Register

Name: CHA_TR (0x46)

Access: Read/Write

7	6	5	4	3	2	1	0
-	-	CHA_DUTY			CHA_VOLT_TRIM		

- **CHA_VOLT_TRIM: Charger voltage trimming**

0: Set the regulation voltage to 4.20V (typical).

1: Set the regulation voltage to 4.17V (typical).

2: Set the regulation voltage to 4.13V (typical).

3: Set the regulation voltage to 4.10V (typical).

4: Set the regulation voltage to 4.23V (typical).

5: Set the regulation voltage to 4.26V (typical).

6: Set the regulation voltage to 4.30V (typical).

7: Set the regulation voltage to 4.07V (typical).

- **CHA_DUTY: Charger duty cycle for pulsed charge phase**

Duty ratio threshold of “on” cycles to “off” cycles

0: Duty cycle threshold: 1/4

1: Duty cycle threshold: 1/8

2: Duty cycle threshold: 1/16

3: Duty cycle threshold: 1/32

4: Duty cycle threshold: 1/64

5: Duty cycle threshold: 1/128

6: Duty cycle threshold: 1/256

7: Duty cycle threshold: 1/512

Block Description

Table 6. Digital Pin Description List

Name	Input/Output	POR State	Level	Current Capability (mA)	Description
SCLK	Input		gnddig - vout3		SPI clock input
nSEN	Input with 100 k pull-up		gnddig - vout3		SPI clock select 0: SPI selected 1: SPI unselected
SDI	Input		gnddig - vout3		SPI data input
SDO	Output	hiz	gnddig - vout3	2	SPI data output
BUTTON_OUT	Output	gnd	gnddig - vout3	1	State of the button sent to the microprocessor 0: button unpressed or global reset active 1: button pressed
BUTTON_IN	Input with 100 k pull-down		gnddig - vsauv		Input connecting to the button 0: button unpressed 1: button pressed
POWER_EN	Input		gnddig - vout3		Input coming from the microprocessor to put off the AT73C203 0: AT73C203 forced in off mode (ignored during global reset) 1: no action
nINT	Output	vout3	gnddig - vout3	1	Interrupt output to warn the microprocessor 0: an interrupt occurred 1: no interrupt occurred
CHG_INHIBIT	Input		gnddig - vout3		Inhibit charger input. 0: no action 1: charger is stopped
nSHUTDOWN	Input with 100 k pull-up		gnddig - vsauv		Asynchronous reset 0: AT73C203 in reset (including the digital block) 1: no action
nPROC_RESET	Output	gnd	gnddig - vout3	1	Reset output for the microprocessor 0: Reset active 1: Reset inactive
nPROC_RESET_OUT	Input		gnddig - vout3		Reset input
BOARD_RESET	Output	vout3	gnddig - vout3	1	Reset output
nBOARD_RESET	Output	gnd	gnddig - vout3	1	Reset output
nASIC_RESET	Output	gnd	gnddig - vout3	1	Reset output
nASIC_RESET_REQUEST	Input		gnddig - vout3		Reset input

Table 6. Digital Pin Description List

Name	Input/Output	POR State	Level	Current Capability (mA)	Description
IDBITS0	Input/Output with 100 k pull-down		gnddig - vout3	1	By default: used as input (must be connected to gnd or vout3) Can be configured as output
IDBITS1	Input/Output with 100 k pull-down		gnddig - vout3	1	By default: used as input (must be connected to gnd or vout3) Can be configured as output
IDBITS2	Input/Output with 100 k pull-down		gnddig - vout3	1	By default: used as input (must be connected to gnd or vout3) Can be configured as output
PORTEST	Output		avss-vswin		Pin used for test POR MUST BE LEFT UNCONNECTED
IDBITS3	Input/Output with 100 k pull-down		gnddig - vout3	1	By default: used as input (must be connected to gnd or vout3) Can be configured as output
SELDC25	Input		gnddig - vsauv		Voltage rail 2 selection
SELDC175	Input		gnddig - vsauv		Voltage rail 1 selection
nEN_RAIL3	Input		gnddig - vsauv		Enable rail 3 (read at start-up) 0: Rail 3 enabled 1: Rail 3 disabled
nEN_RAIL4	Input		gnddig - vsauv		Enable rail 4 (read at start-up) 0: Rail 4 enabled 1: Rail 4 disabled
PCMCIA	Input		gnddig - vsauv		Input to configure the threshold of the power switch controller to consider PSU to be present 0: threshold = 4.7 - 4.3V 1: threshold = 2.9V - 2.7V see section 4.2.
SIM_PRES	Input with 100 k pull-down		gnddig - vsauv		Card presence detection contact input To be used with a normally open presence switch 0: no card connected 1: card connected
nUSIM_INT	Output		gnddig - vout3	1	USIM interrupt output 0: an USIM interrupt occurred 1: no USIM interrupt occurred
SYST_CLK	Input with 100 k pull-down		gnddig - vout3		Clock input from the microprocessor. The frequency of syst_clk must be at least two times superior to sclk. Maximum frequency: 13 MHz. SYST_CLK duty cycle must be better than 30%-70%.

Table 6. Digital Pin Description List

Name	Input/Output	POR State	Level	Current Capability (mA)	Description
SIM_IO	Input/Output	Off	gnddig - vsim	respects the ETS TS 102 221 V4.2.0 standard	USIM bidirectional interface line
SIM_RESET	Output		gnddig - vsim	respects the ETS TS 102 221 V4.2.0 standard	USIM reset line
SIM_CLK	Output	Off	gnddig - vsim	respects the ETS TS 102 221 V4.2.0 standard	USIM clock line
VREFFUSE	Input with 550 k pull-down		avss-vswin		Pin used for test mode and to blow up fuses. MUST BE CONNECTED TO GROUND
SCAN_TEST_MD	Input with 100 k pull-down		gnddig - vsauv		Pin for test. MUST BE CONNECTED TO GROUND
SCAN_ENABLE	Input with 100 k pull-down		gnddig - vsauv		Pin for test. MUST BE CONNECTED TO GROUND
TEST1	Input/Output (Input only in functional mode)		gnddig - vsauv		Pin used for test. But also: TEST1 = 0: RAIL1 ENABLED TEST1 = 1: RAIL1 DISABLED
TEST2	Input/Output (Input only in functional mode)		gnddig - vsauv		Pin used for test. But also: TEST2 = 0: RAIL2 ENABLED TEST2 = 1: RAIL2 DISABLED

Table 7. For Digital Pins Referred to VOUT3

Symbol	Parameter	Conditions	V_{DD}	Min	Max	Units
V_{IL}	Low level Input Voltage	Guaranteed input low Voltage	From 3.0V to 3.5V	-0.3	0.3 x V_{DD}	V
V_{IH}	High level Input Voltage	Guaranteed input high Voltage	From 3.0V to 3.5V	0.7 x V_{DD}	V_{DD}+ 0.3	V
V_{OL}	Low level Output Voltage	I_{OL} = 1 mA or 2 mA depending on the pin (see Table 6)	From 3.0V to 3.5V		0.4	V
V_{OH}	High level Output Voltage	I_{OH} = 1 mA or 2 mA depending on the pin (see Table 6)	From 3.0V to 3.5V	2.4		V

Table 8. For Digital Pins Referred to VSAUV

Symbol	Parameter	Conditions	V_{DD}	Min	Max	Units
V_{IL}	Low level Input Voltage	Guaranteed input low Voltage	From 2.4V to 2.6V	-0.3	0.3 x V_{DD}	V
V_{IH}	High level Input Voltage	Guaranteed input high Voltage	From 2.4V to 2.6V	0.7 x V_{DD}	V_{DD}+ 0.3	V
V_{OL}	Low level Output Voltage	I_{OL} = 1 mA or 2 mA depending on the pin (see Table 6)	From 2.4V to 2.6V		0.4	V
V_{OH}	High level Output Voltage	I_{OH} = 1 mA or 2 mA depending on the pin (see Table 6)	From 2.4V to 2.6V	1.6		V

Power Switch

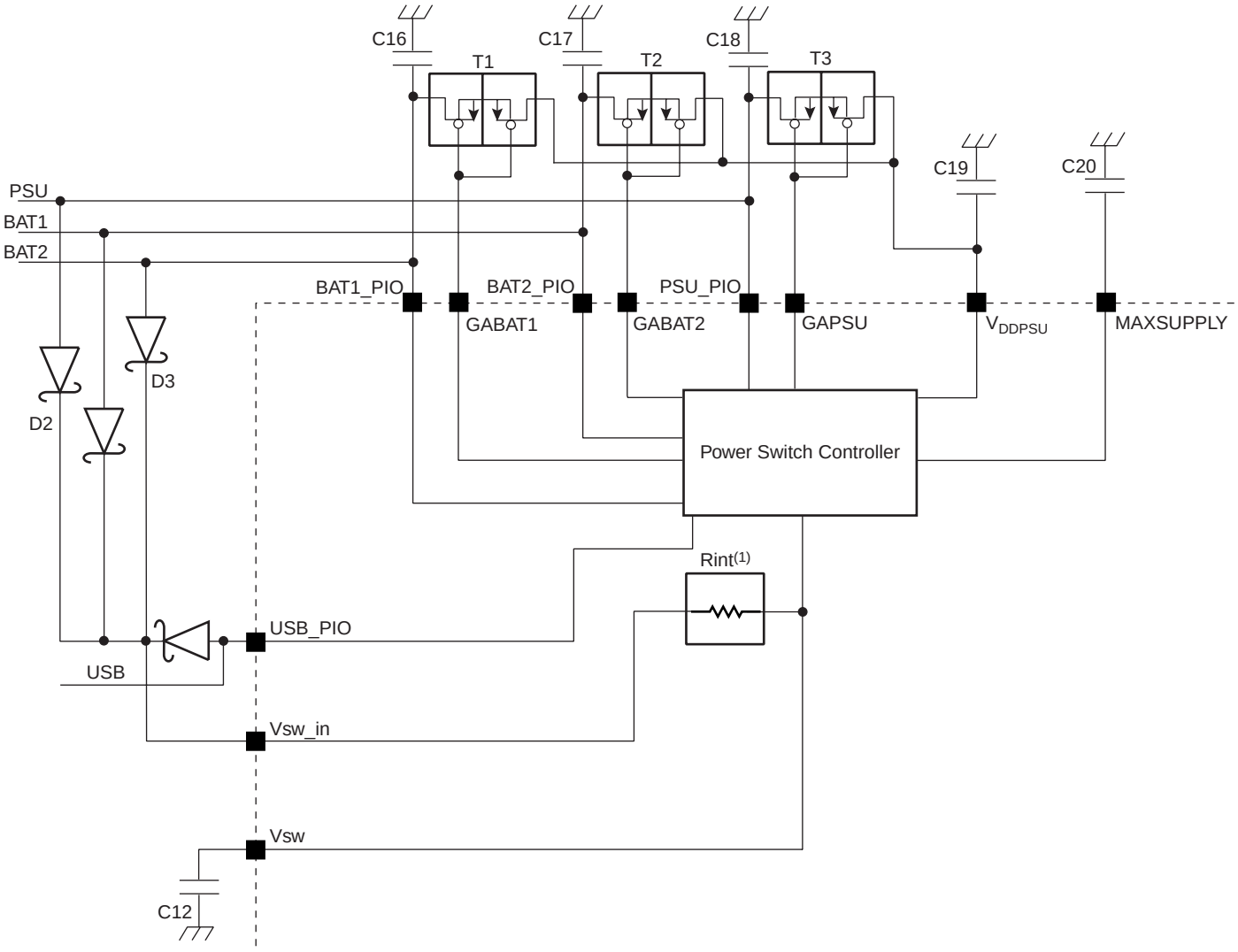
The power switch control block drives external dual PMOS devices to multiplex V_{DDPSU} from battery 1 (BAT1), battery 2 (BAT2) and an AC/DC Power supply unit (PSUIN).

The purpose of this cell is to guarantee a sufficient supply for V_{DDPSU} and to limit drops even during switchover.

Inrush current from source to V_{DDPSU} must be avoided.

Back powering from a selected power source to all other power sources must be avoided.

Figure 13. Power Switch Controller



Note: 1. Print is internal to the AT73C203.

Automatic Selection

When the power switch digital control block is off, V_{DDPSU} is set to the high impedance state. The supply of this cell comes from an analog OR done with four external Schottky diodes connected to BAT_1PIO, BAT2_PIO, PSU_PIO and USB_IN.

The system should respect the “Universal Serial Bus Specification”, especially section 7.2.4.1, which specifies that the maximum equivalent load seen by the USB is 10 µF in parallel with 44 ohms.

When the cell is on, the power switch must automatically select the correct power source.

PSU is a non current-limited 5V supply output. BAT2 is a Lithium Ion battery and can be removed. BAT1 is a Lithium Ion battery and is always soldered to the PCB.

A selection priority rule is used:

PSU > BAT2 > BAT1

When the PSU is plugged in, it is selected by default.

If the PSU is not plugged in, BAT2 is used if it is present and has enough voltage.

If PSU is not plugged in, and BAT2 is unplugged or below the flat threshold, BAT1 is used if BAT1’s voltage is high enough.

For a critical situation on any of the power sources, the automatic switching shall ensure that V_{DDPSU} stays within specifications. This means that the automatic supply selection FETs must be switched as quickly as possible, ideally with a maximum switchover of 1 µs (max: 5 µs) and guarantee that the already enabled FETs are switched off before the newly selected FETs are switched on.

The faster the switching, the smaller the capacitance required to hold up V_{DDPSU} (target: 100 µF max).

To handle all cases, fast analog comparators on each input with appropriate hysteresis (in voltage and in time) must be used within the AT73C203.

To meet the 5 µs requirement, the comparator must be fast enough to detect when a source is disconnected (or a low voltage threshold is reached) but slow enough when detecting that a new source is plugged in (depending on contact bounce during the insertion/removal of a power source). The slow delay is done with the 10 kHz internal oscillator.

At start-up, the cell is off and is turned on by the internal digital block.

With PWS_CR register (bits accessible via SPI), the application processor can force an input source to be selected. This may be used for testing the AT73C203 or by the application processor to force use of one of the batteries.

Using PWS_SR register, the application processor can read which supply is currently selected by the AT73C203.

If one input is not used (PSU, BAT1 or BAT2), it can be grounded. The corresponding unused output (GAPSU, GABAT1 or GABAT2) can be left unconnected in this case.

Power Switch Controller Electrical Specifications

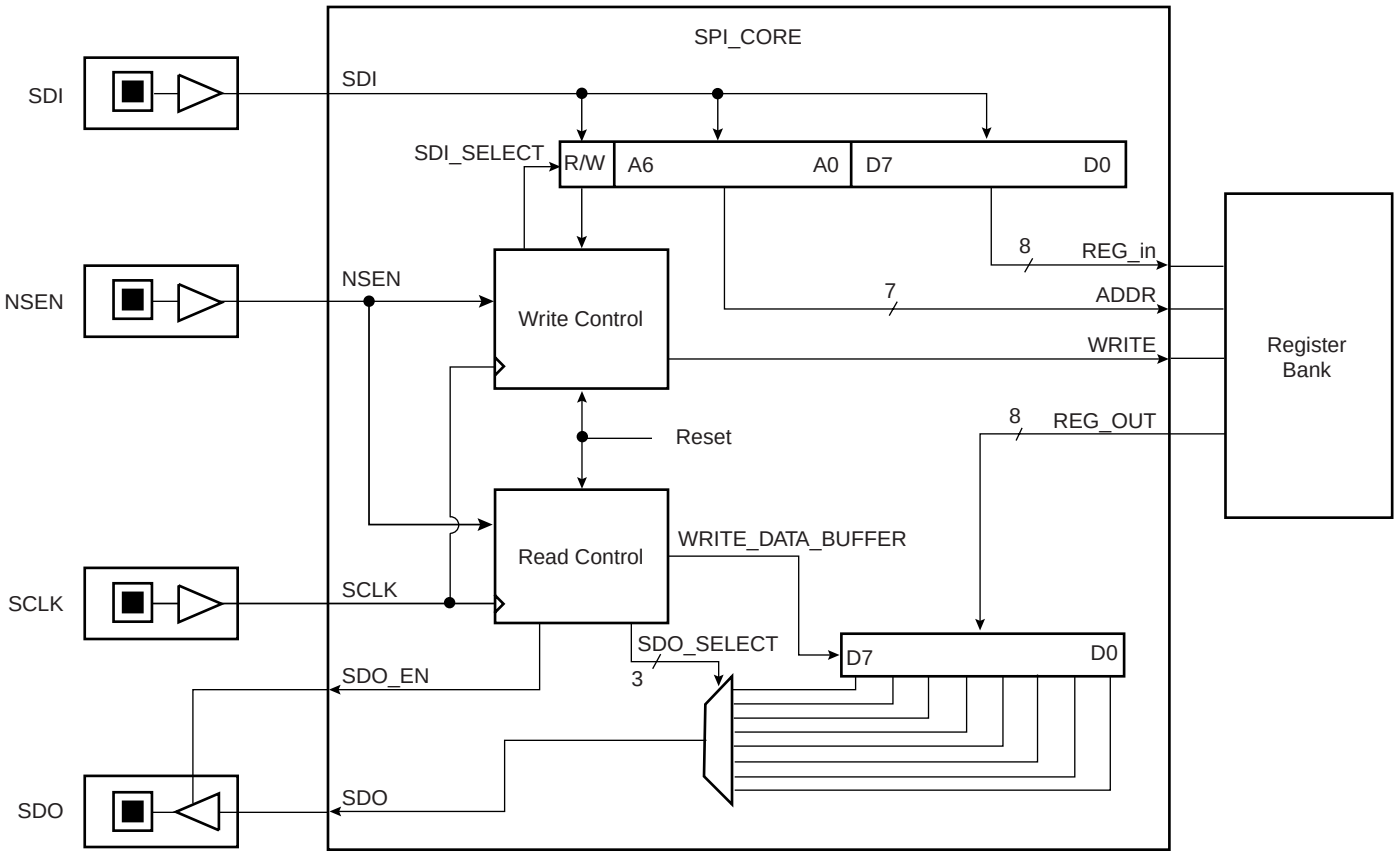
Table 9. Power Switch Controller Electrical Specifications

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Top	Operating temperature		-20		+85	°C
Psupio	Charger supply voltage			5	5.5	V
B_{AT2PIO}	Battery 2 supply voltage			3.6	4.35	V
B_{AT1PIO}	Battery 1 supply voltage			3.6	4.35	V
I_{PSU}	Current load on V_{DDPSU}				2	A
I_{CC}	Current consumption	onpio = 1, psupio = 5.5V, B_{AT2PIO} = 4.35V and B_{AT1PIO} = 4.35V.			500	uA
I_{OFF}	Off current	onpio = 0 and precharg = 0			30	µA
t_{SW}	Switching time between two sources			1	5	µs
$V_{DDPSUMIN}$	Minimum voltage on V_{DDPSU}	onpio = 1, input selected = 3.1V	2.85			V
$t_{STARTUP}$	Time to start			50	100	µs
$t_{PRECHAREGE}$	Time to precharge the V_{DDPSU} capacitor	onpio = 0 and precharg = 1, external load on V_{DDPSU} = 100 µA			100	ms
t_{DEBOUN_PSU}	Time for debouncing the PSU presence				100	ms
t_{DEBOUN_BAT2}	Time for debouncing the bat2 presence				100	ms
Psupio_r1	Voltage to consider PSU plugged in	Rising, V_{BG} = 1.23V, Pcmcia = 0		3.43		V
Psupio_f1	Voltage to consider PSU removed	Falling, V_{BG} = 1.23V, Pcmcia = 0		2.96		V
Psupio_hy1	PSU hysteresis	Input hysteresis, Pcmcia = 0		470		mV
Psupio_r2	Voltage to consider PSU plugged in	Rising, V_{BG} = 1.23V, Pcmcia = 1		3.05		V
Psupio_f2	Voltage to consider PSU removed	Falling, V_{BG} = 1.23V, Pcmcia = 1		2.80		V
Psupio_hy2	PSU hysteresis	Input hysteresis, Pcmcia = 1		250		mV
Bat2pio_r	Voltage to consider BAT2 available	Rising, V_{BG} = 1.23V		3.20		V
Bat2pio_f	Voltage to consider BAT2 removed or flat	Falling, V_{BG} = 1.23V		2.95		V
Bat2pio_hy	BAT2 hysteresis	Input hysteresis		250		mV
Bat1pio_r	Voltage to consider bat1 available	Rising, V_{BG} = 1.23V		3.20		V
Bat1pio_f	Voltage to consider bat1 removed or flat	Falling, V_{BG} = 1.23V		2.95		V
Bat1pio_hy	BAT1 hysteresis	Input hysteresis		250		mV

Serial Peripheral Interface (SPI)

The SPI interface between the system and the AT73C203 is detailed in Figure 14.

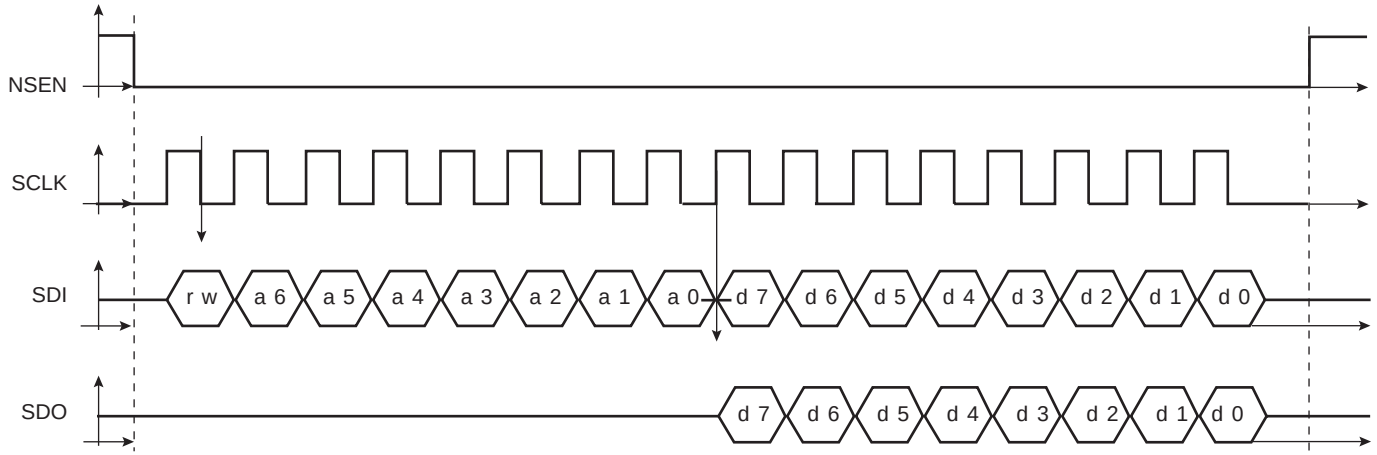
Figure 14. SPI Architecture



Protocol

The SPI is a 4-wire bidirectional asynchronous serial link providing 128 x 8 register access by the microprocessor. The SPI operates in slave mode only. The SPI protocol is shown in Figure 15.

Figure 15. SPI Protocol



On SDI, the first bit is read/write. “0” indicates a write operation while “1” denotes a read operation. The seven following bits are used for the register address and the eight that follow are the write data. For both address and data, the most significant bit is the first one.

In case of a read operation, SDO first provides the contents of the read register, MSB.

The transfer is enabled by the NSEN signal active low. When the SPI is not operating, SDO output is set to high impedance to allow sharing of the CPU serial interface with other devices. The interface is reset at every rising edge of NSEN in order to return to an idle state, even if the transfer does not succeed.

The SPI is synchronized with the serial clock SCLK. Falling edge latches SDI input and rising edge shifts SDO output bits.

Timing for SPI Interface SPI interface timings are shown in Figure 16.

Figure 16. SPI Interface Timing Diagram

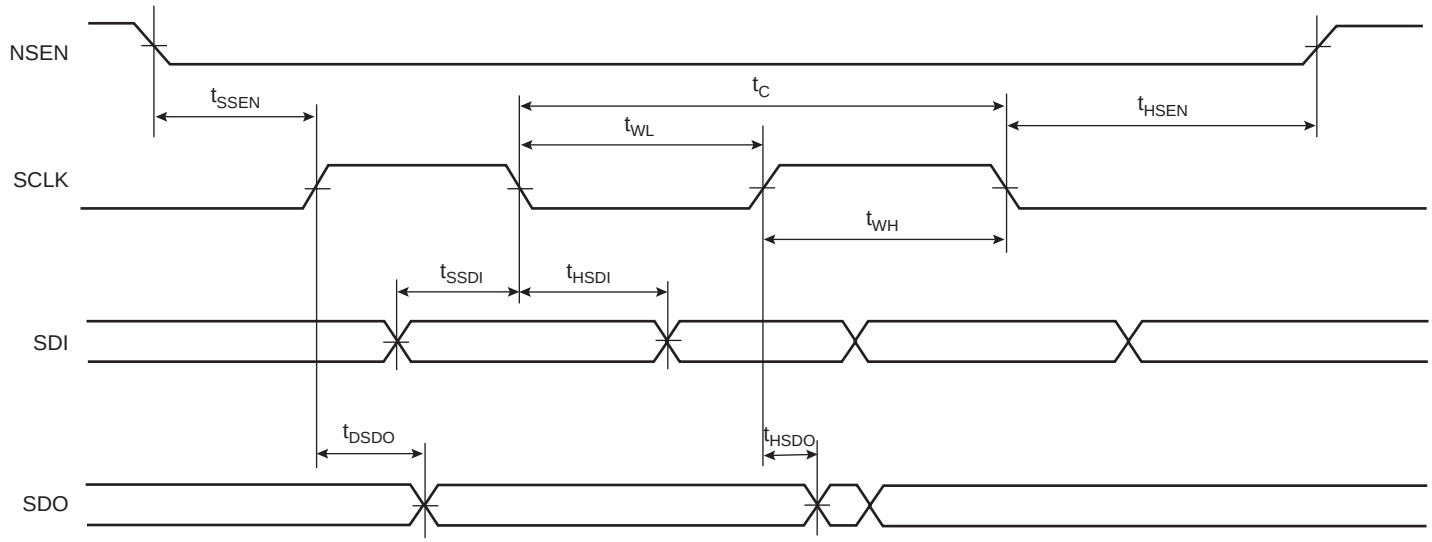


Table 10. SPI Timing Parameters

Timing Parameter	Description	Min	Max
t_C	SCLK min period	(1)t_{SYSCLK}/2	
t_{WL}	SCLK min pulse width low	50 ns	-
t_{WH}	SCLK min pulse width high	50 ns	-
t_{SSEN}	Setup time SEN falling to SCLK rising	50 ns	-
t_{HSEN}	Hold time SCLK falling to SEN rising	t_{SYSCLK}	-
t_{SSDI}	Setup time SDI valid to SCLK falling	20 ns	-
t_{HSDI}	Hold time SCLK falling to SDI not valid	20 ns	-
t_{DSDO}	Delay time SCLK rising to SDO valid	-	20 ns
t_{HSDO}	Hold time SCLK rising to SDO not valid	0 ns	-

Note: 1. t_{SYSCLK} = system clock period.

The frequency of SYS_CLK must be at least two times superior to that of SCLK.

After the end of reset (nPROC_RESET = 1), SYS_CLK must run at least during 500 µs before the first SPI access.

The minimum time for the USIM is one system clock period (t_{SYSCLK}).

As the clock domain is 900 kHz, to monitor function registers, two consecutive accesses at the same register must be superior to the 900 kHz period. Otherwise, only the second access will be taken into account.

The same approach is used for the charger registers but with 10 kHz.

RAIL1 DC/DC Converter 1.20V, 1.2A

Rail1 is a programmable buck DC/DC converter dedicated to the application processor core supply. The default voltage is 1.20V. Three other values can be programmed: 1.3V, 1.1V and 1.5V.

An external pin can select 1.75V (SELDC175) output voltage with tuning: 1.80V, 1.70V and 1.65V. The entire cell is optimized for 1.20V.

When the cell is off, the output is pulled to ground.

The application processor can change the output voltage, as stated above, via registers accessible by the SPI.

Figure 17. Rail1 Schematic

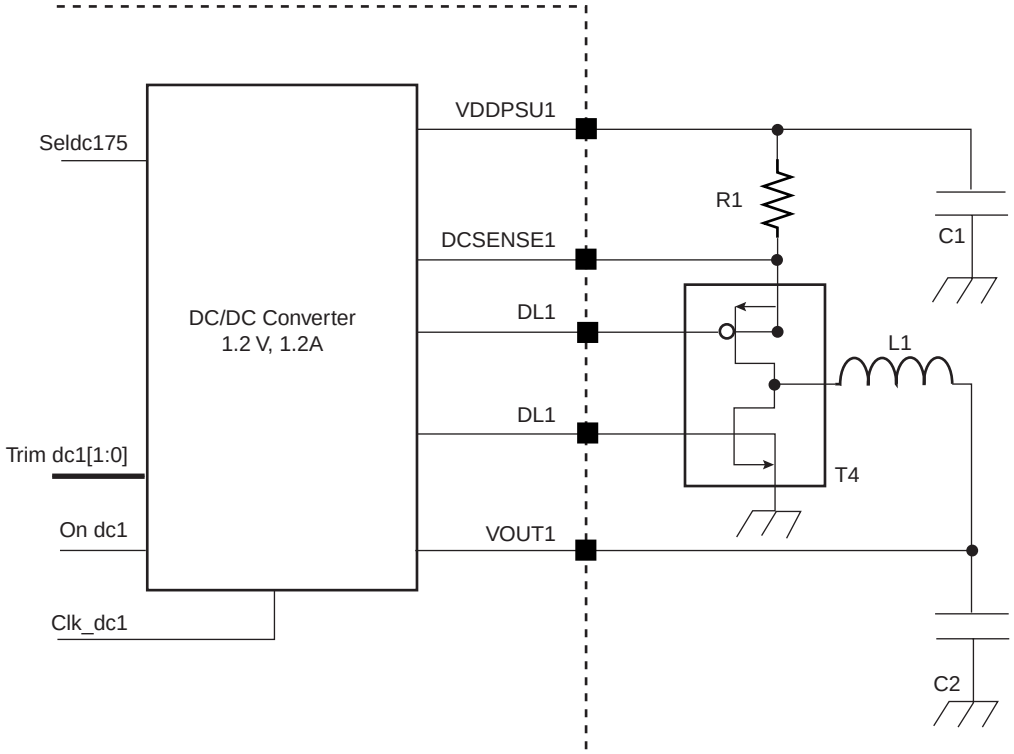


Table 11. Rail1 External Components

Schematic Reference	Reference
C1	22 µF Ceramic capacitor
C2	47 µF tantalum low ESR TPSW476M010R0150 capacitor or equivalent
L1	4.7 µH: SMT3106-471M (Gowanda)
R1	100 mΩ ± 2% 250 mW
T4	Si5513DC

Rail1 Electrical Specifications

Rail1 can operate up to a load of 1.5 A if the R1 resistor is replaced by 80 mΩ ± 2%. Rail 1 can also operate at V_{IN} = 2.85V.

Table 12. Rail1 Electrical Specifications

Symbol	Parameter	Condition (1.2V Selected)	Min	Typ	Max	Unit
V_{IN}	Operating Supply Voltage		2.97		5.5	V
	Temperature Range		-20		85	°C
V_{OUT}	Output Voltage	0 < I_{LOAD} < 1200 mA, 3V < V_{IN} < 5.5V		1.2		V
I_{OUT}	Output Current				1200	mA
	Ripple Voltage			40		mV
Eff36	Efficiency	V_{IN} = 3.6V, I_{LOAD} = 600 mA		83		%
Eff50	Efficiency	V_{IN} = 5V, I_{LOAD} = 600 mA		85		%
	Static line regulation	t_R = t_F = 5 µs, V_{IN} from 3V to 5.5V I_{LOAD} = 1200 mA		25		mV
	Static load regulation	t_R = t_F = 5 µs, V_{IN} = 3V and V_{IN} =5.5V I_{LOAD} from 0 to 1200 mA		10		mV
	Transient line regulation	t_R = t_F = 5 µs, V_{IN} from 3V to 5.5V I_{LOAD} = 1200 mA		35		mV
	Transient load regulation	t_R = t_F = 5 µs, V_{IN} = 3V and V_{IN} = 5.5V I_{LOAD} from 0 to 1200 mA		80		mV
I_{CC}	Powerdown Current	V_{IN} = 5.5V			1	µA
t_R	Rise Time	I_{LOAD} = 400 mA	0.01		10	ms
t_{R1200}	Rise Time	I_{LOAD} = 1200 mA	0.01		15	ms
t_{SETTLE}	Settling time for programmed voltage switching	Full load, 0.85V to 1.3V condition		70		µs
I_{SC}	Limitation current	3V < V_{IN} < 5.5V	1.2			A

Rail2 DC/DC Converter 1.8V, 1.2 A

Rail2 is a programmable buck DC/DC converter dedicated to digital supply. The default voltage is 1.8V. Three other values can be programmed: 1.85V, 1.75V and 1.70V. An external pin can select 2.5V output voltage (SELDC25) tuning: 2.6V, 2.4V and 2.3V. The entire cell is optimized for 1.8V

When the cell is off, the output is in high impedance state.

The application processor can change the output voltage, as stated above, via registers accessible by the SPI.

Figure 18. Rail2 Schematic

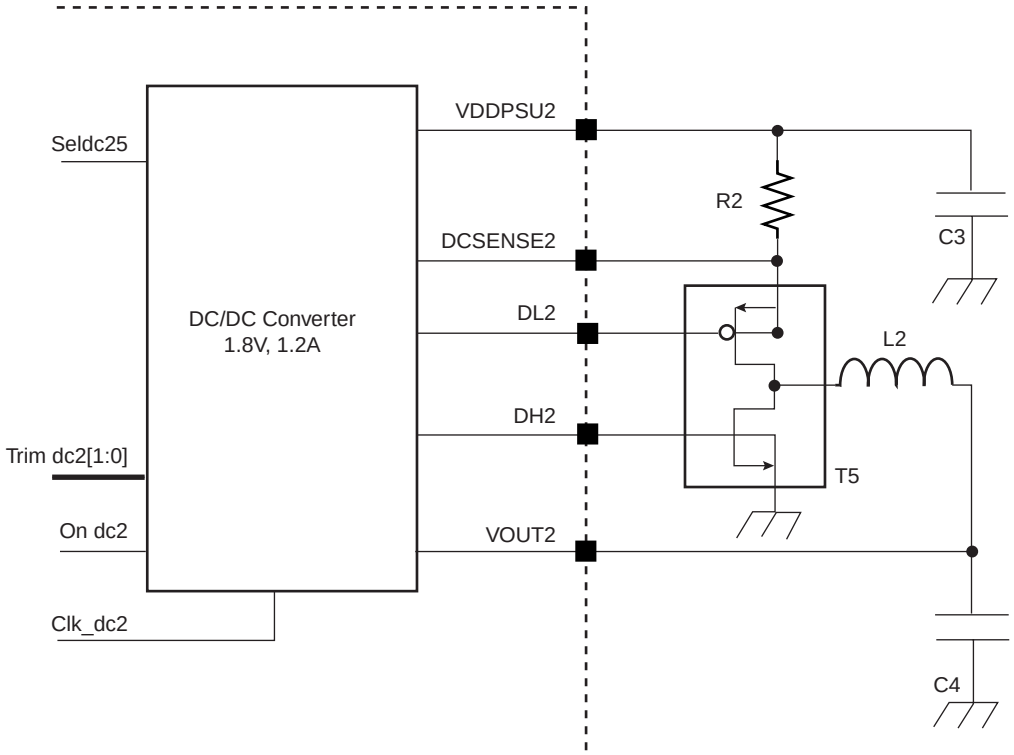


Table 13. Rail2 External Components

Schematic Reference	Reference
C3	22 µF Ceramic capacitor
C4	47 µF tantalum low ESR TPSW476M010R0150 capacitors or equivalent
L2	10 µH: SMT3106-102M (Gowanda)
R2	100 mΩ ± 2% 250 mW
T5	Si5513DC

Rail2 Electrical Specifications

Rail 2 can also operate at V_{IN} = 2.85V.

Table 14. Rail2 Electrical Specifications

Symbol	Parameter	Condition (1.2V Selected)	Min	Typ	Max	Unit
V_{IN}	Operating Supply Voltage		2.97		5.5	V
	Temperature Range		-20		85	°C
V_{OUT}	Output Voltage	$0 < I_{LOAD} < 1200$ mA, $3V < V_{IN} < 5.5V$		1.8		V
I_{OUT}	Output Current				1200	mA
	Ripple Voltage	I_{LOAD} = 1.2 A, V_{IN} = 3.6V		200		mV
Eff36	Efficiency	V_{IN} = 3.6V, I_{LOAD} = 600 mA		85		%
Eff50	Efficiency	V_{IN} = 5V, I_{LOAD} = 600 mA		87		%
	Static line regulation	$t_R = t_F$ = 5 µs, V_{IN} from 3V to 5.5V, I_{LOAD} = 1200 mA		25		mV
	Static load regulation	$t_R = t_F$ = 5 µs, V_{IN} = 3V and V_{IN} = 5.5V, I_{LOAD} from 0 to 1200 mA		10		mV
	Transient line regulation	$t_R = t_F$ = 5 µs, V_{IN} from 3V to 5.5V, I_{LOAD} = 1200 mA		35		mV
	Transient load regulation	$t_R = t_F$ = 5 µs, V_{IN} = 3V and V_{IN} = 5.5V, I_{LOAD} from 0 to 1200 mA		80		mV
I_{CC}	Powerdown Current	V_{IN} = 5.5V			1	µA
t_R	Rise Time	I_{LOAD} = 1200 mA			1000	ms
t_{SETTLE}	Settling time for programmed voltage switching	Full load, 0.85V to 1.3V condition		50		µs
I_{SC}	Limitation current	$3V < V_{IN} < 5.5V$	1.2	2		A

Rail3 DC/DC Converter 3.3V, 520 mA

Rail3 is a programmable buck DC/DC converter followed by a linear drop out regulator. The default value of the LDO is 3.3V. Three other values can be programmed: 3.1V, 3.2V and 3.4V. The entire cell is optimized for 3.3V.

When the cell is off, the output is pulled to ground.

The application processor can change the output voltage, as stated above, via registers accessible by the SPI.

Figure 19. Rail3 Schematic

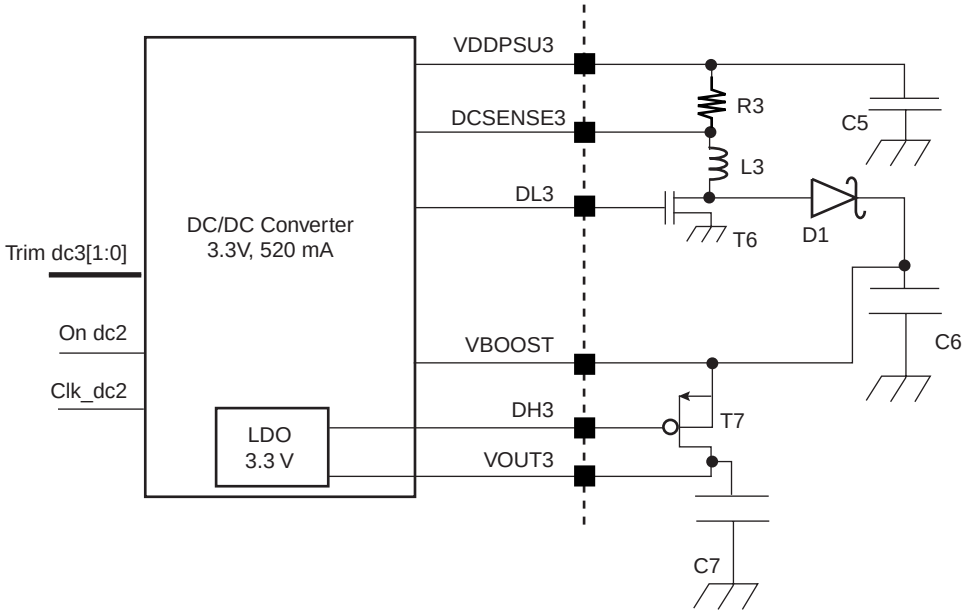


Table 15. Rail3 External Components

Schematic Reference	Reference
C5,	22 µF ceramic capacitor
C6, C7	47 µF tantalum low ESR TPSW476M010R0150 capacitor or equivalent
D1	Schottky diode: MBRA120LT3 (ON Semiconductor)
L3	10 µH: SMT3106-102M (Gowanda)
R3	100 mΩ ± 2% 250 mW
T6	Si1400DL
T7	Si8401DL

Rail3 Electrical Specifications

Rail 3 can also operate at V_{IN} = 2.85V.

Table 16. Rail3 Electrical Specifications

Symbol	Parameter	Condition (3.3V Selected)	Min	Typ	Max	Unit
V_{IN}	Operating Supply Voltage		2.97		5.5	V
	Temperature Range		-20		85	°C
V_{OUT}	Output Voltage	$0 < I_{LOAD} < 520$ mA, $3V < V_{IN} < 5.5V$			520	V
I_{OUT}	Output Current				1200	mA
	Ripple Voltage			70		mV
Eff36	Efficiency	V_{IN} = 3.6V, I_{LOAD} = 430 mA		73		%
Eff50	Efficiency	V_{IN} = 5V, I_{LOAD} = 430 mA		65		%
	Static line regulation	$t_R = t_F$ = 5 µs, V_{IN} from 3V to 5.5V, I_{LOAD} = 430 mA		30		mV
	Static load regulation	$t_R = t_F$ = 5 µs, V_{IN} = 3V and V_{IN} = 5.5V, I_{LOAD} from 52 to 468 mA		20		mV
	Transient line regulation	$t_R = t_F$ = 5 µs, V_{IN} from 3V to 5.5V, I_{LOAD} = 300 mA		80		mV
	Transient load regulation	$t_R = t_F$ = 5 µs, V_{IN} = 3V and V_{IN} = 5.5V, I_{LOAD} from 0 to 300 mA		70		mV
I_{CC}	Powerdown Current	V_{IN} = 5.5V			1	µA
t_R	Rise Time	I_{LOAD} = 400 mA	0.01		100	ms
t_{SETTLE}	Settling time for programmed voltage switching	Full load, 3.1V to 3.4V condition		500		µs
I_{SC}	Limitation current	$3V < V_{IN} < 5.5V$	520	850		mA

Rail 4 DC/DC Converter 0.9V, 1.2A

Rail4 is a programmable buck DC/DC converter dedicated to the supply of advanced core processing units. The default voltage is 0.9V. Three other values can be programmed: 1.2V, 0.87V and 1.1V. The entire cell is optimized for 0.9V.

When the cell is off, the output is in high impedance state.

The application processor can change the output voltage, as stated above, via registers accessible by the SPI.

Figure 20. Rail4 Schematic

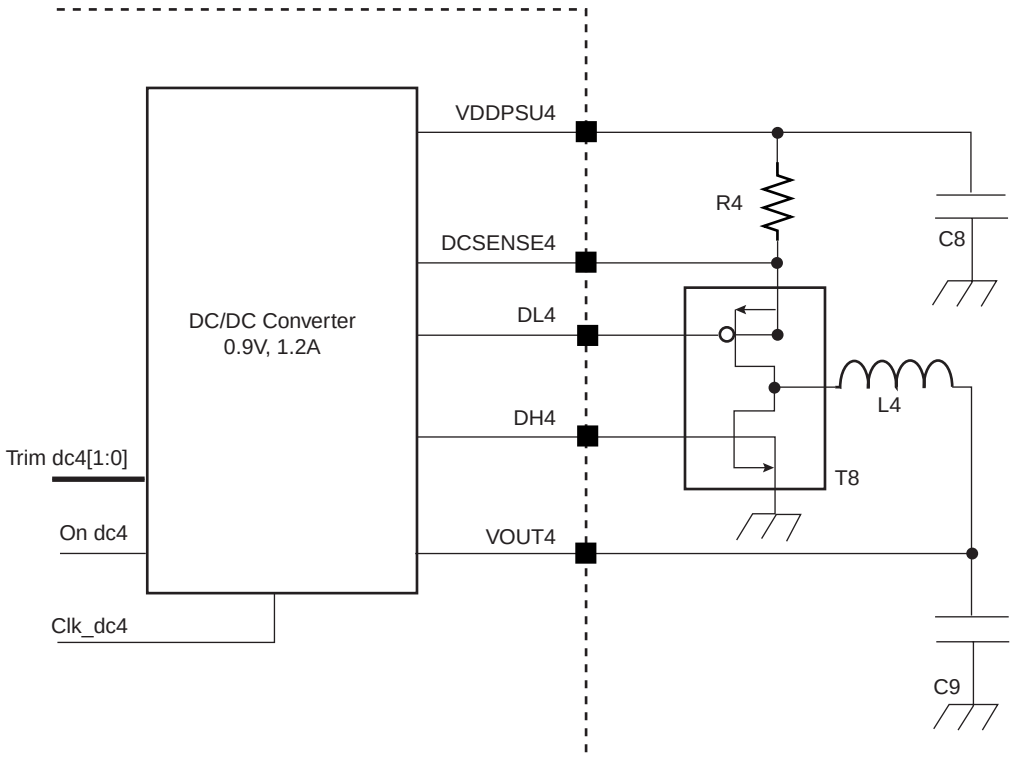


Table 17. Rail4 External Components

Schematic Reference	Reference
C8,	22 µF ceramic capacitor
C9	47 µF tantalum low ESR TPSW476M010R0150 capacitor or equivalent
L4	4.7 µH: SMT3106-47M (Gowanda)
R4	100 mΩ ± 2% 250 mW
T8	Si5513DC

Rail4 Electrical Specifications

Rail 4 can also operate at V_{IN} = 2.85V.

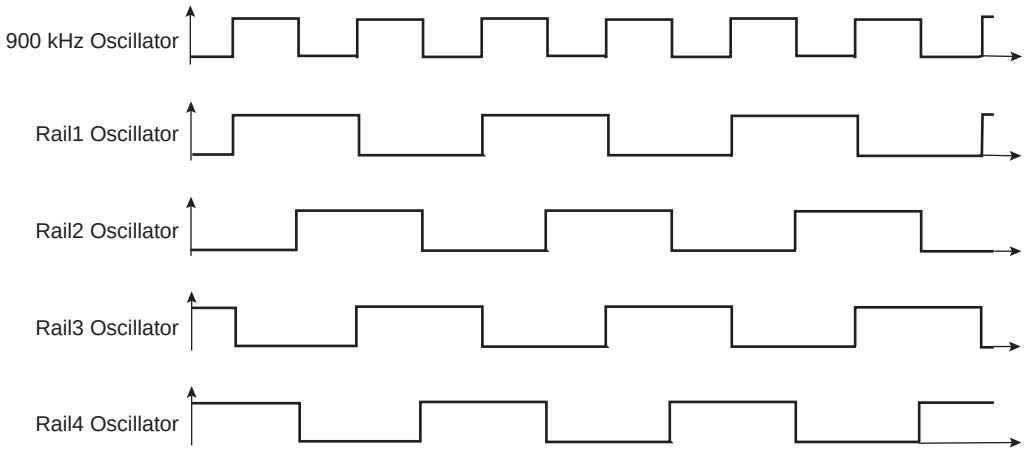
Table 18. Rail4 Electrical Specifications

Symbol	Parameter	Condition (0.9V Selected)	Min	Typ	Max	Unit
V_{IN}	Operating Supply Voltage		2.97		5.5	V
	Temperature Range		-20		85	°C
V_{OUT}	Output Voltage	$0 < I_{LOAD} < 1200$ mA, $3V < V_{IN} < 5.5V$		0.9		V
I_{OUT}	Output Current				1200	mA
	Ripple Voltage	I_{LOAD} = 1.2 A, V_{IN} = 3.6V		35		mV
Eff36	Efficiency	V_{IN} = 3.6V, I_{LOAD} = 600 mA		78		%
Eff50	Efficiency	V_{IN} = 5V, I_{LOAD} = 600 mA		80		%
	Static line regulation	$t_R = t_F$ = 5 µs, V_{IN} from 3V to 5.5V, I_{LOAD} = 1200 mA		20		mV
	Static load regulation	$t_R = t_F$ = 5 µs, V_{IN} = 3V and V_{IN} = 5.5V, I_{LOAD} from 120 to 1200 mA		10		mV
	Transient line regulation	$t_R = t_F$ = 5 µs, V_{IN} from 3V to 5.5V, I_{LOAD} = 1200 mA		35		mV
	Transient load regulation	$t_R = t_F$ = 5 µs, V_{IN} = 3V and V_{IN} = 5.5V, I_{LOAD} from 120 to 1200 mA		85		mV
I_{CC}	Powerdown Current	V_{IN} = 5.5V			1	µA
t_R	Rise Time	I_{LOAD} = 1200 mA			3000	µs
tsettle	Settling time for programmed voltage switching	Full load, 0.84V to 0.93V condition		50		µs
I_{SC}	Limitation current	$3V < V_{IN} < 5.5V$	1200	2		mA

900 kHz Oscillator and Clock Distribution

The 900 kHz oscillator provides the clock to all DC/DC converters. The clock distributor provides phased clocks to the DC/DC converters to avoid them switching at the same time.

Figure 21. 900 kHz Oscillator Distribution

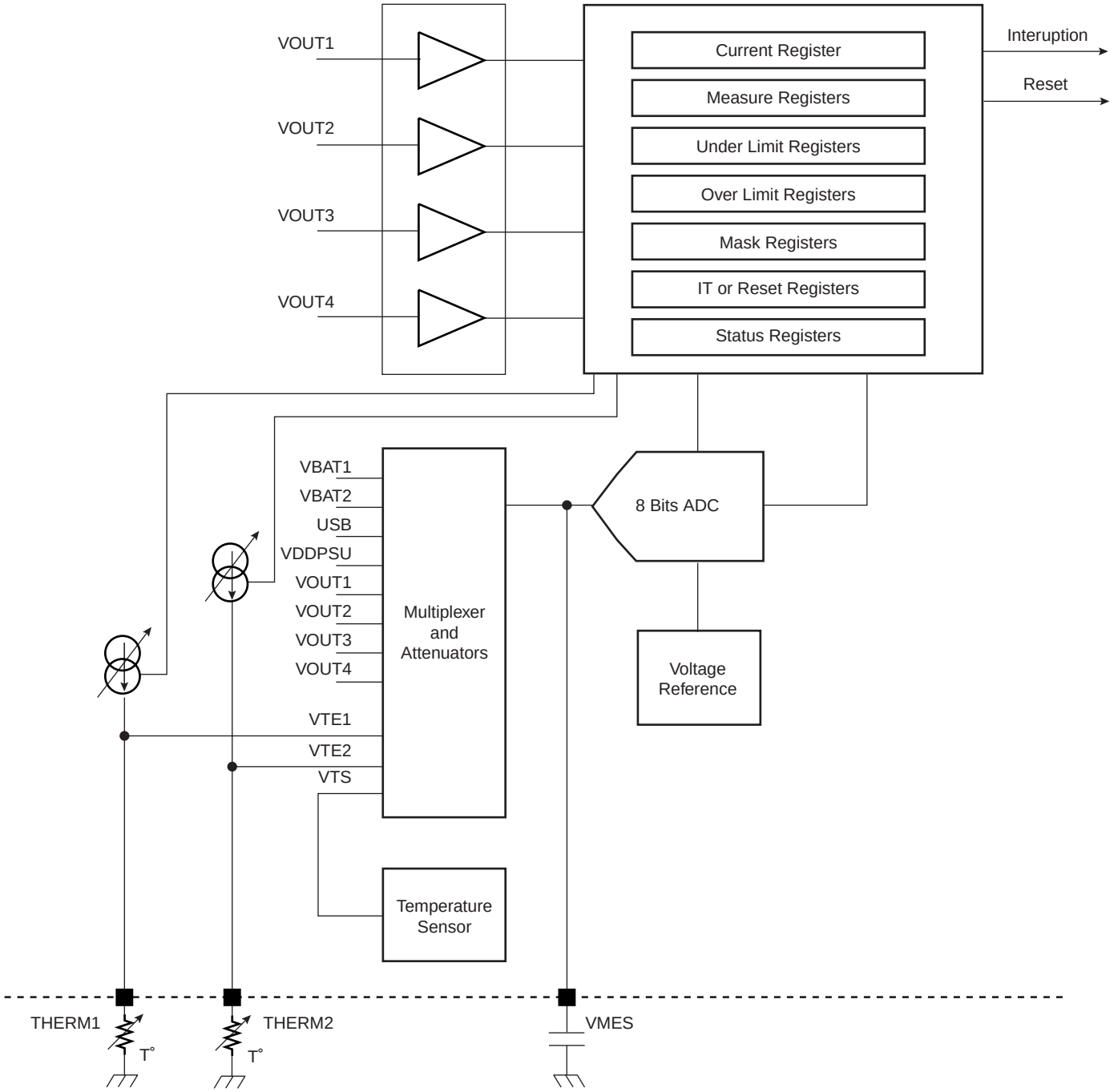


Voltage and Temperature Monitoring Function

The AT73C203 integrates voltage monitoring and temperature monitoring functionalities, thus enabling the application processor to know when an under-voltage or over-temperature error condition occurs. The application processor can control this situation by changing the thresholds and programming an interrupt or a reset in the event an error condition occurs.

All the controls are performed via registers accessed via the SPI.

Figure 22. Voltage and Temperature Monitoring Architecture



Analog to Digital Converter and Multiplexer

An internal 8-bit analog to digital converter is used to measure the different voltages. The analog to digital converter has eleven internal inputs listed as follows:

- V_{BAT1} (internal battery)
- V_{BAT2} (external battery)
- USB (USB supply)
- V_{DDPSU} (output of the power switch)
- V_{OUT1} (output of Rail1)
- V_{OUT2} (output of Rail2)
- V_{OUT3} (output of Rail3)
- V_{OUT4} (output of Rail4)
- V_{TE1} (voltage on thermistor 1)
- V_{TE2} (voltage on thermistor 2)
- V_{TS} (output of the internal temperature sensor)

An external capacitor (C21) on V_{MES} pin enables filtering of the ADC input and provides immunity to high frequency noise.

These inputs are multiplexed into the analog to digital converter. This has a resolution of eight bits. The basic input range is 0.6V to 2.25V (typical) but the inputs have built-in attenuators to allow measurements without external components.

Take note that no attenuator is present for V_{OUT1}, V_{OUT4}, V_{TE1}, V_{TE2} and V_{TS}.

Voltage and Temperature Monitoring Electrical Characteristics

All bridge resistance values are given with ± 30% of global variations and mismatch values of less than 1%. All ratios will be confirmed during the design process.

Table 19. Bridge Monitoring (Attenuators) Electrical Specifications

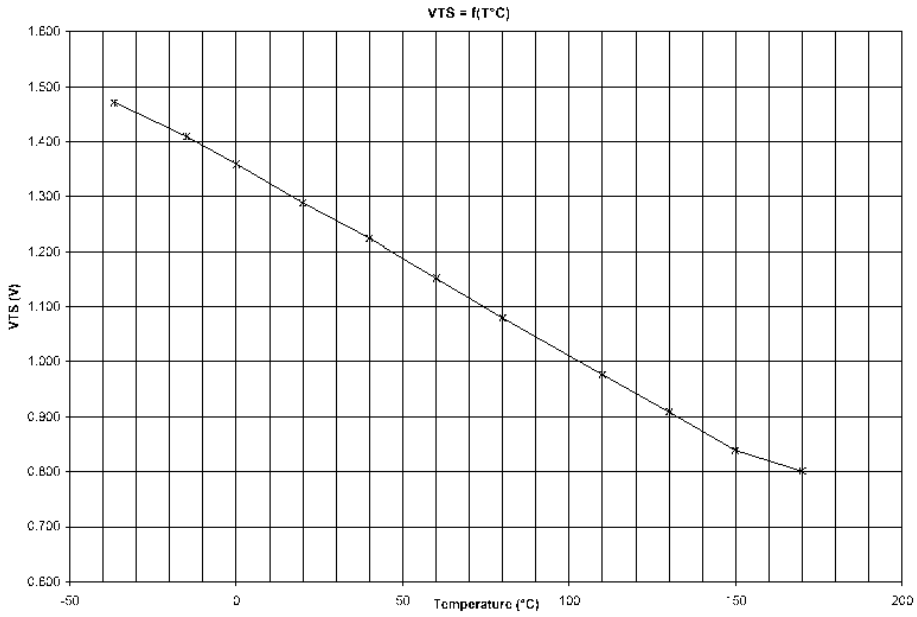
Symbol	Parameter	Condition	Min	Typ	Max
R_{ATBAT1}	Ratio V_{BAT1}	0V ÷ 5.5V		2.5	
R_{ATBAT2}	Ratio V_{BAT2}	0V ÷ 5.5V		2.5	
R_{ATUSB}	Ratio USB	0V ÷ 5.5V		2.5	
R_{VDDPSU}	Ratio V_{DDPSU}	0V ÷ 2.5V		2.5	
R_{OUT2}	Ratio V_{OUT2}	0V ÷ 3.4V		2.0	
R_{OUT3}	Ratio V_{OUT3}	0V ÷ 5.5V		2.0	

Typical sensor characteristic law: $V(T) = 1.31 - 3.6 \times 10^{-3} \times (T - 27)$

Table 20. Temperature Sensor Electrical Specifications

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{CC}	Supply Voltage		2.4	2.5	2.6	V
I_{CC}	Supply current	V_{CC} = 2.5V			100	µA
DJ	Temperature sense dynamic		0		80	°C
εT	Absolute error	ϑ = 55°C			±10	°C
ΔT/Δϑ	Differential error	10% - 90%, Δϑ = [45°C, 55°C]			±5%	
V/ϑ	Voltage dynamic range	10% - 90%, Δϑ = [0°C, 80°C]			1	V
ΔV/Δϑ	Sensor voltage sensitivity		1		20	mV/°C
V_{TNOM}	Sensor output voltage @27°C	ϑ = 27°C	1.23		1.33	V

Figure 23. Typical Sensor Characteristics



Digital Core Function

By default, the digital core function is disabled. To enable it, the MON_ON bit in register MON_CR must be set to 1. A transition from 0 to 1 of MON_ON resets all the internal registers.

When the digital core function is on, the internal digital core automatically starts the monitoring sequence. It cycles sequentially through the measurement of the analog inputs. Eight measurements are taken, then the digital core computes the average of these eight values to reduce noise before moving to the next input.

Average values from these inputs are stored in value registers. See Table 21.

These can be read out through the SPI bus. Measurements are updated every 2 ms (approximate).

Table 21. Value Registers

MON_VBAT1_MEAS	MON_VOUT3_MEAS
MON_VBAT2_MEAS	MON_VOUT4_MEAS
MON_USB_MEAS	MON_VTE1_MEAS
MON_VDDPSU_MEAS	MON_VTE2_MEAS
MON_VOUT1_MEAS	MON_VTS_MEAS
MON_VOUT2_MEAS	

To assure better accuracy, a calibration should be made during the printed circuit board test by injecting an accurate voltage into the analog inputs and checking the voltage read by the ADC. By comparing the voltage read by the ADC to the theoretical value stored in an external flash memory, the software can remove the internal offset.

An automatic comparison is launched when the monitoring function is enabled. The digital core compares the measurement with programmed limits stored in the limit registers. See Table 22.

Table 22. Limit Registers

MON_VBAT1_UNDL	MON_VBAT1_OVL
MON_VBAT2_UNDL	MON_VBAT2_OVL
MON_USB_UNDL	MON_USB_OVL
MON_VDDPSU_UNDL	MON_VDDPSU_OVL
MON_VOUT1_UNDL	MON_VOUT1_OVL
MON_VOUT2_UNDL	MON_VOUT2_OVL
MON_VOUT3_UNDL	MON_VOUT3_OVL
MON_VOUT4_UNDL	MON_VOUT4_OVL
MON_VTE1_UNDL	MON_VTE1_OVL
MON_VTE2_UNDL	MON_VTE2_OVL
MON_VTS_UNDL	MON_VTS_OVL

The results of out-of-limit comparisons are stored in the status registers (see Table 23 on page 87), which can be read over the SPI to flag an out-of-limit condition.

Table 23. Status Registers

MON_SR1	MON_SR2

When an out-of-limit comparison occurs, an interrupt or a reset can be programmed via mask and interrupt/reset registers. See Table 24.

Table 24. Mask and Interrupt /Reset Registers

MON_MR1	MON_IR1
MON_MR2	MON_IR2

Thermistor Measurement

Two external NTC thermistors are used to measure the temperature of the battery. The resistance of the NTC is proportional to the temperature.

To measure the resistance and determine the temperature two 6-bit current DACs are integrated into the AT73C203.

The software can program the current flowing through thermistors 1 and 2 via MON_VTE1_CURR and MON_VTE2_CURR registers and can then read back the voltage through MON_VTE1_MEAS and MON_VTE2_MEAS registers. The temperature can then be estimated by the microprocessor.

Current DAC Electrical Specifications

The 6-bit DAC parameters are shown in Table 25 below.

Table 25. Current DAC Electrical Specifications

Symbol	Parameter	Condition	Min	Typ	Max	Units
$V_{TEXCURR<0>}$	$V_{TEXCURR<0>}$		6	7.5	9	µA
$V_{TEXCURR<1>}$	$V_{TEXCURR<1>}$		12	15	18	µA
$V_{TEXCURR<2>}$	$V_{TEXCURR<2>}$		24	30	36	µA
$V_{TEXCURR<3>}$	$V_{TEXCURR<3>}$		48	60	72	µA
$V_{TEXCURR<4>}$	$V_{TEXCURR<4>}$		96	120	144	µA
$V_{TEXCURR<5>}$	$V_{TEXCURR<5>}$		192	240	288	µA
Lincurr	Linearity I_{OUT} = f(Rl)	Rl: resistive load to ground V_{OUT} = 0 to 2.35V			2	%

Comparator Electrical Specifications

In parallel to the DAC, a comparator for each digital core supply rail (V_{OUT1}, V_{OUT2}, V_{OUT3} and V_{OUT4}) is used as a real time supply rail brownout detector for a drop.

The value of the comparator is not programmable but the threshold moves according to the voltage chosen. (Refer to the DC/DC converter specifications specific to each supply rail.)

Table 26. Comparator Electrical Specifications

Symbol	Parameter	Condition	Min	Typ	Max	Units
$V_{OUT1COMP}$	V_{OUT1} Threshold			8		%
$V_{OUT2COMP}$	V_{OUT2} Threshold			8		%
$V_{OUT3COMP}$	V_{OUT3} Threshold			7		%
$V_{OUT4COMP}$	V_{OUT4} Threshold			8		%

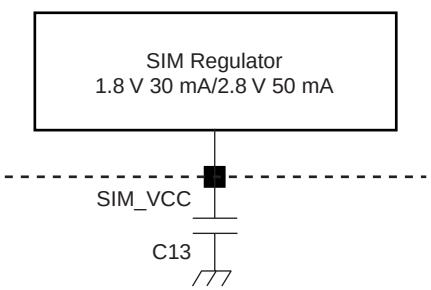
USIM Interface

A Low Drop Out (LDO) voltage regulator provides an accurate power supply to the SIM card. Two nominal values can be programmed: 1.8V or 2.8V. It is supplied by V_{DDPSU}.

When the cell is off, the output is pulled to ground.

The application processor can change the output voltage, as stated above, via registers accessible by the SPI.

Figure 24. USIM Regulator



External components: 2.2 µFX5R ± 10% output capacitor

USIM 1.8V Regulator Electrical Specifications

The USIM 1.8V regulator complies with ETS TS 102 221, sections 5 and 6.

Table 27. USIM 1.8V Regulator Electrical Specifications

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{DDSIM}	Operating Supply Voltage		2.97		5.5	V
	Temperature Range		-20		85	°C
V_{SIM}	Output Voltage	$0 < I_{LOAD} < 30$ mA, $3V < V_{DDSIM} < 5.5V$	1.75	1.80	1.85	V
I_{OUT}	Output Current				30	mA
V_{DROP}	Min Supply for SIM_VCC > 1.75V	I_{LOAD} = 50 mA	1.90			V
	Transient Line Regulation	$t_R = t_F$ = 5 µs, V_{DDSIM} from 3V to 5.5V, I_{LOAD} = 30 mA			40	mV
	Transient Load Regulation	$t_R = t_F$ = 5 µs, V_{IN} = 2.97V, I_{LOAD} from 3 to 27 mA			40	mV
I_{CC}	Quiescent Current	V_{DDSIM} = 5.5V			50	µA
I_{CC}	Powerdown Current	V_{DDSIM} = 5.5V			1	µA
t_R	Rise Time	I_{LOAD} = 30 mA 10% - 90% V_{OUT}			500	µs
I_{SC}	Limitation Current	$3V < V_{DDSIM} < 5.5V$	30			mA
V_N	Output Noise	BW: 10 Hz to 100 kHz Including bandgap noise			1	mVrms

USIM 2.8V Regulator Electrical Specifications

The USIM 2.8V regulator complies with ETS TS 102 221, sections 5 and 6.

Table 28. USIM 2.8V Regulator Electrical Specifications

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{DDSIM}	Operating Supply Voltage		2.97		5.5	V
	Temperature Range		-20		85	°C
V_{SIM}	Output Voltage	$0 < I_{LOAD} < 30$ mA, $3V < V_{DDSIM} < 5.5V$	2.77	2.8	2.83	V
I_{OUT}	Output Current				30	mA
V_{DROP}	Min Supply for SIM_VCC > 1.75V	I_{LOAD} = 50 mA	2.85			V
	Transient Line Regulation	$t_R = t_F$ = 5 µs, V_{DDSIM} from 3V to 5.5V, I_{LOAD} = 30 mA			30	mV
	Transient Load Regulation	$t_R = t_F$ = 5 µs, V_{IN} = 2.97V, I_{LOAD} from 3 to 27 mA			30	mV
I_{CC}	Quiescent Current	V_{DDSIM} = 5.5V			50	µA
I_{CC}	Powerdown Current	V_{DDSIM} = 5.5V			1	µA
t_R	Rise Time	I_{LOAD} = 30 mA 10% - 90% V_{OUT}			500	µs
I_{SC}	Limitation Current	$3V < V_{DDSIM} < 5.5V$	50			mA
V_N	Output Noise	BW: 10 Hz to 100 kHz Including bandgap noise			1	mVrms

USIM Digital Interface

The SIM interface conforms to the ETSI technical specification ETSI TS 102 221 V4.2.0 (2001-04) based on the ISO/IEC 7816 standard. Both T = 0 and T = 1 protocols are supported.

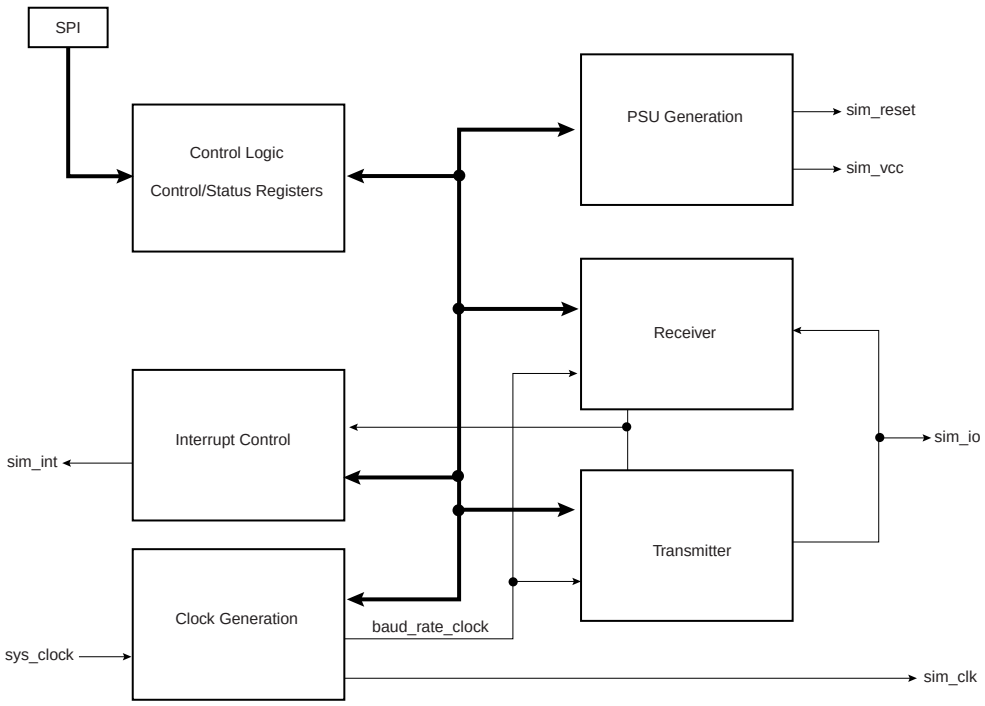
The terminal is configured and controlled via several registers:

- Control Register (SIM_CR)
- Channel Status Register (SIM_CSR)
- Buffer Status Register (SIM_BSR)
- Miscellaneous Status Register (SIM_MSR)
- Interrupt Mask Register 1 (SIM_IMR1)
- Interrupt Mask Register 2 (SIM_IMR2)
- Receiver Time Out Register (SIM_RTOR)
- Baud Divisor Register (SIM_BDR)
- Receiver Holding Register (SIM_RHR)
- Transmitter Holding Register (SIM_THR)
- Transmitter Time Guard Register (SIM_TTGR)
- Number Errors register (SIM_NER)
- Clock Divider Register (SIM_CDR)
- Activation Register (SIM_AR)

All these registers are detailed in Table 4, “AT73C203 User Interface,” on page 22.

Figure 25 shows the major blocks required in the interface.

Figure 25. USIM Interface Digital Architecture



Operating Conditions

Clock

The clock applied to the SIM card is generated by the terminal from the system clock sys_clock (see “SIM Clock Generation” on page 92).

The clock signal can be enabled or disabled by register CLKEN.

CLKEN	0	1
SIM Clock	Disabled	Enabled

Voltage

Both class B and C are supported (ETSI 102.221 section 5.2, 5.3). They correspond to 3V and 1.8V nominal voltage, respectively.

The operating class is selected by register VSEL.

VSEL	00	01	10	11
Selected Voltage	Disabled	Disabled	1.8V	2.8V

The first operating condition applied to the card by the terminal should be class C (1.8V). If the card does not provide an Answer-To-Reset (ATR), class B (3V) should be applied to the card (ETSI 102.221 section 6.2). This should be managed by software.

Presence

The presence of card status is written in the register PRES.

PRES	0	1
Presence of the SIM Card	Not present	Present

An interrupt is generated if the bit PRES is changing. This interrupt can be masked in the interrupt mask register. This interrupt is reset with the RSTPRES bit in control register SIM_CR.

Initial Communication Establishment Procedures

Reset

The reset register SRESET is directly connected to output pin sim_reset.

Cold Reset and Activation

In order to activate the SIM card, electrical circuits should be activated in the following order:

1. SIM card voltage should be chosen with VSEL (SIM_MR).
2. SIM clock should be started by writing 1 to CLKEN (SIM_CR).
3. I/O line should be activated by setting ACTIVE in Control Register SIM_CR.
4. After a minimum of 400 sim_clock cycles, the application should rise SRESET.

The application should be able to detect an absence of ATR after 40000 sim_clock cycles. This can be done by using the timer with an initial value of 108 (108 x 372 = 40176 where 372 is the default baud rate divisor).

Warm Reset

A warm reset is done by writing to register SRESET (SIM_CR). The application has to respect a minimum of 400 sim_clock cycles between falling and rising edges of the pin sim_reset.

As for a cold reset, the absence of ATR should be managed by the application.

Clock Stop

A clock stop can be done by writing 0 on the register CLKEN. The application should ensure that no activity occurs 1860 sim_clock cycles before the clock is stopped. This is done by using the time-out counter.

Deactivation

In order to deactivate the SIM card, electrical circuits should be deactivated in the following order:

1. Write 0 to SRESET.
2. SIM clock should be stopped by writing 0 to CLKEN.
3. I/O line should be deactivated by resetting ACTIVE in Control Register SIM_CR.
4. SIM card voltage should be disabled with register VSEL.

Answer to Reset (ATR)

After reset, the terminal expects a default bit rate = 1/372 f, where f is the SIM clock frequency. This value can be changed afterwards (see below).

The initial waiting time (see specification ISO 7816-3 section 6.3.2) should be programmed in the timer by the application. The required value is 9600 ETUs.

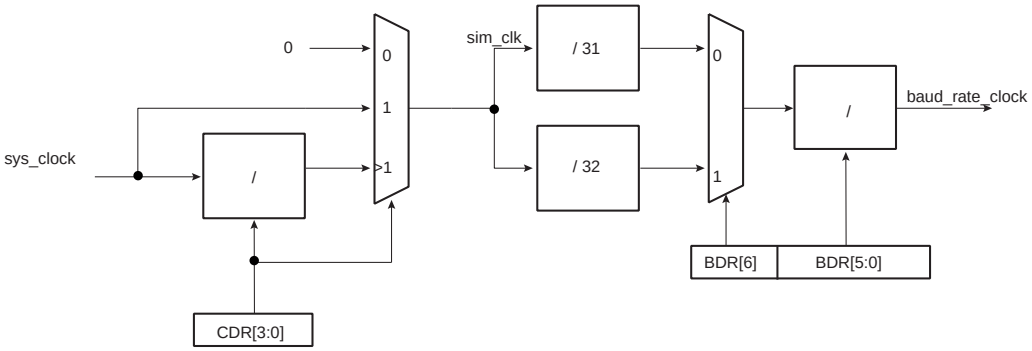
The ATR must be checked by software.

SIM Clock Generation

The SIM clock is generated through a programmable divider. The division factor can be programmed in 4 bits register SIM_CDR.

CDR[3:0]	**0000**	**0001 to 1111**
Clock division factor	No clock	CDR[3:0]

Figure 26. USIM Clock Generation



Speed Enhancement

The baud rate can be programmed in the 7-bit register BDR. The etu is one bit rate clock cycle.

1 bit	6 bits
BDR[6]	BDR[5:0]

The baud rate = f/(div1 x div2) where f is the SIM clock frequency.

div1 is coded on BDR[6].

BDR[6]	**0**	**1**
div1	31	32

div2 is coded on BDR[5:0].

BDR[5:0]	**0**	**1 - 63**
div2	64	BDR[5:0]

Before changing the baud rate division factor, the values supported by the SIM card have to be checked by doing a PPS operation as defined in ISO 7816-3 section 7.

Extra Guardtime

An extra guardtime can be programmed when sending characters to the card. The 8-bit register SIM_TTGR (see “Transmitter Time Guard Register” on page 41) allows an extra time guard from 0 to 255 ETU.

Transmission Protocol

The SIM interface handles all specific requirements defined in ISO7816 T = 0 and T = 1 protocol types. It has also some specific features such as maximum character repetition.

Two 16-byte FIFOs are provided in order to free CPU resources, one for reception and one for transmission. Two 4-bit pointers in the Buffer Status Register (SIM_BSR) indicate how many characters are present in the FIFOs, RXPTR for receiver FIFO, TXPTR for transmitter FIFO.

Reception

The receiver can be reset by using the RSTRX command in SIM_CR. This empties the Rx FIFO and the receiver is waiting for a new valid character.

When a complete character is received, it is transferred to the receiver FIFO and the RXRDY status bit in SIM_CSR is set. If the FIFO is full, the RXFULL status bit in SIM_CSR is set and if a new character is received, the last character in the FIFO is overwritten and the OVRE status bit in SIM_CSR is set.

The receiver FIFO is accessible through Receiver Holding Register (SIM_RHR). In the following, an access to SIM_RHR means an access to the receiver FIFO.

- T=0

Upon detection of a start bit, the following data byte is shifted in the Receiver Holding Register (SIM_RHR) when the shift is completed and the parity is checked. If a parity error is detected, the PARE bit is set in SIM_CSR and a low error signal is sent for one Elementary Time Unit (ETU), 10.5 ETUs after the start bit. This error signal is sent from the receiver to the transmitter but can be inhibited by setting the bit IRXNACK in the register SIM_MR.

- T=1

Upon detection of a start bit, the following data byte is shifted in the Receiver Holding Register (SIM_RHR) when the shift is completed and the parity is checked. If a parity error is detected, the PARE bit is set in status register SIM_CSR. In this protocol there is only one stop bit.

- Time-out

This function allows an idle condition on reception to be detected. The maximum delay for which the terminal should wait for a new character to arrive is programmed in SIM_RTOR (Receiver Time-out). When this register is set to 0, no time-out is detected. Otherwise, the receiver waits for a first character and then initializes a counter, which is decremented at each bit period and reloaded at each byte reception. When the counter reaches 0, the TIMEOUT bit in SIM_MSR is set. The user can restart the wait for a first character with the STTO (Start Time-out) bit in SIM_CR.

Transmission

The transmitter can be reset by using the RSTTX command in SIM_CR. This will empty the Tx FIFO and the transmitter will be inactive until a new character has to be sent.

The transmitter FIFO is accessible through the Transmit Holding Register (SIM_THR).

When a character is written to SIM_THR (Transmit Holding), it is transferred to the Shift Register as soon as it is empty.

Whenever the FIFO is not full, the TXRDY status bit in SIM_CSR is set. If the Transmit Shift Register and the transmitter FIFO are both empty, the TXEMPTY bit in SR is set.

If the FIFO is full and a new character is written to SIM_THR, the last character in the FIFO will be overwritten.

In protocol T=0, if the SIM card sends back a Non-Acknowledgment signal, the status bit TXNACK in register SIM_CSR is set. It can be reset by using the RSTTXNACK command in SIM_CR.

- Time-guard

The time-guard function allows the transmitter to insert an idle state on the IO line between two characters. The duration of the idle state is programmed in SIM_TTGR (Transmitter Time-guard). When this register is set to zero, no time-guard is generated. Otherwise, the transmitter holds a high level on SIM_IO after each transmitted byte for the number of bit periods programmed in SIM_TTGR.

Timings

- T = 0

The minimum interval between two consecutive characters is at least 12 ETUs.

If two consecutive characters are sent in opposite directions, the minimum interval of time should be 16 ETUs. This is automatically managed by the hardware.

WWT (Work waiting time) overflow can be managed by the 16-bit time-out counter. If 65536 cycles are not enough, the timer can be rearmed by using the RETTO command in register in SIM_CR.

- T = 1

The minimum interval between the leading edge of the start bits of two consecutive characters is at least 11 etus.

The Block Guard Time (22 etus) is automatically managed by hardware.

CWT (Character waiting time) and BWT (Block waiting time) can be managed by the time-out counter as for WWT in protocol T=0.

Character Repetition for T = 0

Protocol T = 0 allows character repetition.

- Reception

When IRXNACK is set and a parity error is detected, an error signal is not sent. The received byte is available in the SIM_RHR register and the RXRDY bit is set.

If IRXNACK = 0, the number of character repetitions depends on Disable Successive Non-Acknowledgment (DSRXNACK) bit and MAX_ITERATION bits, both in SIM_MR.

MAX_ITERATION is a 3-bit field configurable with a value between 0 and 7. This implies that a character can be repeated up to eight times.

If DSRXNACK = 0, an error signal is sent on the I/O line as soon as a parity error occurs in the received character.

If DSRXNACK = 1, successive parity errors are counted up to the value specified in the MAX_ITERATION field. These parity errors generate a error signal on the SIM_IO line. As soon as this value is reached, no additional error signal is sent on the I/O line. The flag ITERATION is asserted.

To reset the ITERATION (SIM_MSR) flag, the RSIT bit must be set in the Control Register (SIM_CR).

- Transmission

A character repetition can be executed if the MAX_ITERATION field in SIM_MR is different from 0.

If MAX_ITERATION = 0, no repetition is done.

If MAX_ITERATION is different from zero and no parity error has been detected, no repetition is done.

If MAX_ITERATION is different from zero and a parity error has been detected, the transmitter re-sends the corrupted value. If a parity error is still detected, the corrupted value is sent as many times as the value loaded in the MAX_ITERATION field.

If the number of repetitions of the corrupted value reaches the value loaded in the MAX_ITERATION field, the ITERATION (SIM_MSR) flag is set. The transmitter is disabled until the ITERATION flag is reset.

If at some stage during the repetition sequence, no error parity is detected, repetition is stopped.

To reset the ITERATION (SIM_MSR) flag, the RSIT command can be used, but in that case the transfer will continue if the FIFO is not empty and not all characters would have been correctly sent. That's why it is recommended to reset the transmitter with the RSTTX command in the Control Register (SIM_CR).

Error Counter

If errors occurred during a transfer, it is possible to obtain the total number of errors by reading the register in SIM_NER. This is a read-only register reset by a read action. Up to 255 errors can be recorded.

Interrupts

All interrupts can be masked in registers SIM_IMR1 and SIM_IMR2

RXRDY

A character has been received.

An interrupt occurs when status bit RXRDY in SIM_CSR is set.

Reset of status bit causes reset of interrupt.

RXFULL The receiver FIFO is full.
An interrupt occurs when status bit RXFULL in SIM_CSR is set.
Reset of status bit causes reset of interrupt.

OVRE The last character in the receiver FIFO has been overwritten.
An interrupt occurs when status bit OVRE in SIM_CSR is set.
Reset of status bit causes reset of interrupt.

PARE A parity error occurred.
An interrupt occurs when status bit PARE in SIM_CSR is set.
Reset of status bit causes reset of interrupt.

TXRDY The transmitter FIFO has one byte space left.
An interrupt occurs when status bit TXRDY in SIM_CSR is set.
Reset of status bit causes reset of interrupt.

TXEMPTY All characters have been transmitted.
An interrupt occurs when status bit TXEMPTY in SIM_CSR is set.
Reset of status bit causes reset of interrupt.

TXNACK An error bit has been received.
An interrupt occurs when status bit TXNACK in SIM_CSR is set.
Reset of status bit causes reset of interrupt.

TIMEOUT The timer has expired.
An interrupt occurs when status bit TIMEOUT in SIM_MSR is set.
Reset of status bit causes reset of interrupt.

ITERATION The maximum iteration number has been reached.
An interrupt occurs when status bit ITERATION in SIM_MSR is set.
Reset of status bit causes reset of interrupt.

PRES The SIM card has been removed or inserted.
An interrupt occurs when status bit PRES in SIM_MSR is changing.
RSTPRES command in register SIM_CR causes reset of interrupt.

RXHALF The receiver FIFO is half full.
An interrupt occurs when receiver FIFO pointer RXPTR goes from 7 to 8.
Reading SIM_BSR causes reset of interrupt.

TXHALF The transmitter FIFO is half full.
An interrupt occurs when transmitter FIFO pointer TXPTR goes from 9 to 8.
Reading SIM_BSR causes reset of interrupt.

Charger Control

The AT73C203 is able to control the charging of two lithium ion batteries from either a PSU or USB supply.

Charging can occur in two different modes as follows:

- Stand-alone mode. The AT73C203 preconditions the battery independently of the application processor (the application processor is not powered up).
- Controlled mode. The application processor controls the charging phases via registers accessed via the SPI.

Figure 27. Charger Control Schematic

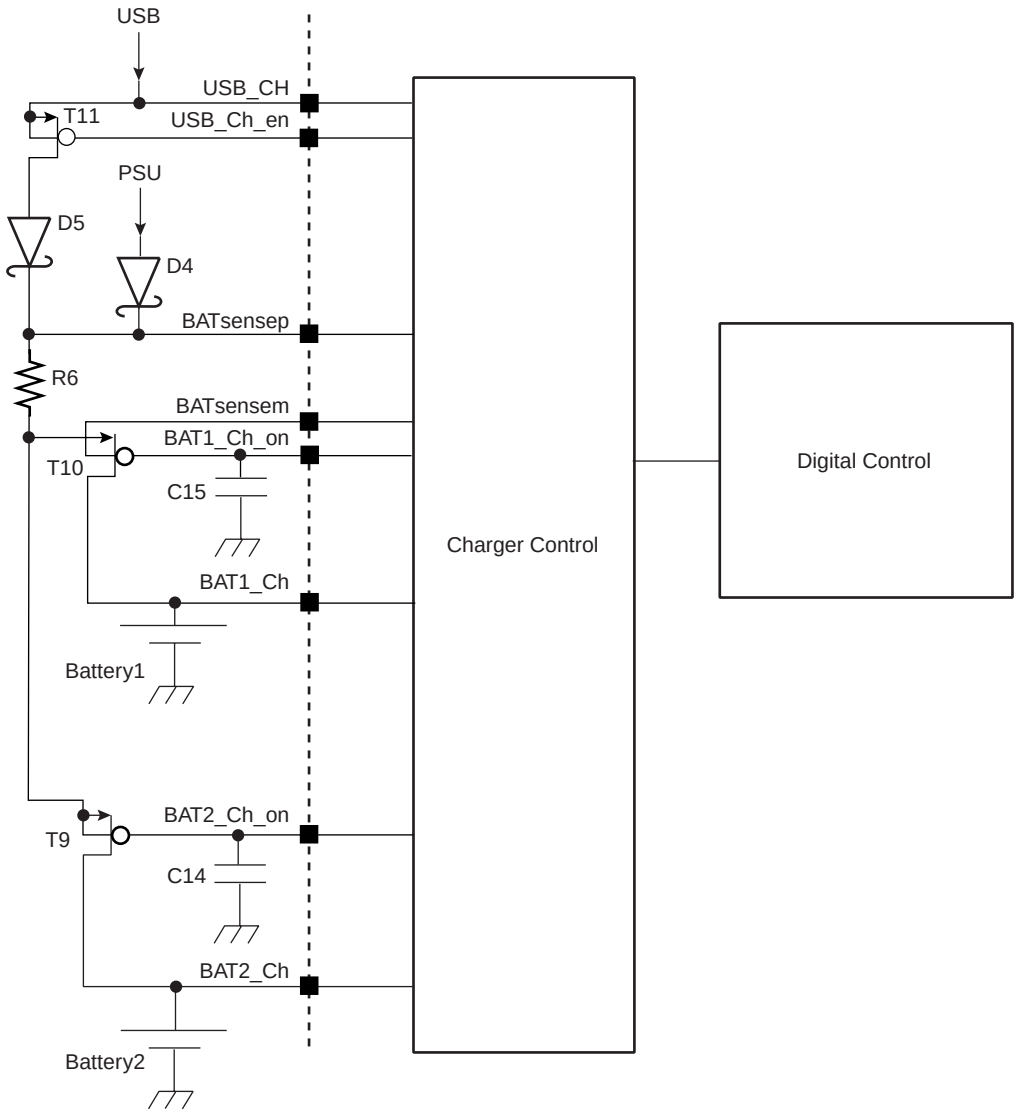


Table 29. Charger Components

Schematic Reference	Reference
BAT1	Li-ion battery 4.2V-3.0V. Permanently connected to module
BAT2	Li-ion battery 4.2V-3.0V. Optional battery
C14, C15	10 nFX56 ± 10% ceramic capacitor
D4, D5	MBRA120LT3 (ON Semiconductor)
R6	200 mΩ +/- 2% 50 mW
T7	Si8401DL
T11	Si1405DL

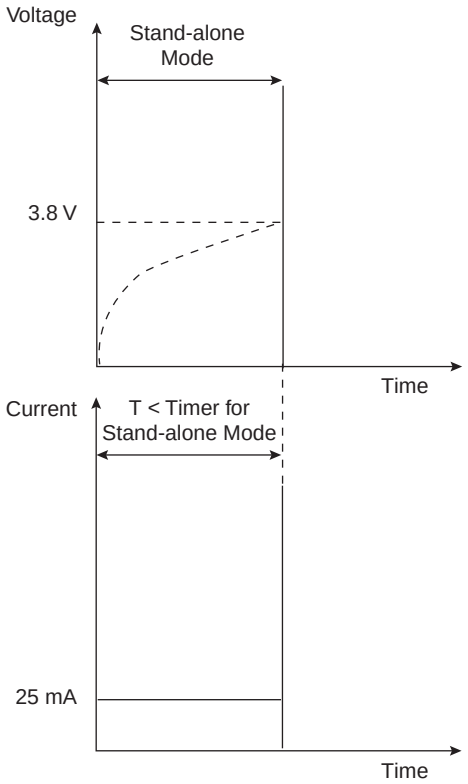
Charge Principles

Stand-alone Mode

The stand-alone mode occurs only when the USB is plugged in and there is no battery 2 (or it is flat) and battery 1 is flat and the PSU unplugged (see “State Machine Description” on page 15 and Figure 30 on page 101). The AT73C203 can then choose to precharge battery 1 if the temperature range is within limits. The stand-alone mode is terminated if the charge timer expires or if the voltage of battery 1 goes above 3.8V.

The digital core (via the USB_SCR register) can put the AT73C203 into a mode in which the digital core is off and battery 1 is charged (25 mA) through the USB up to 4.1V.

Figure 28. Stand-alone Mode

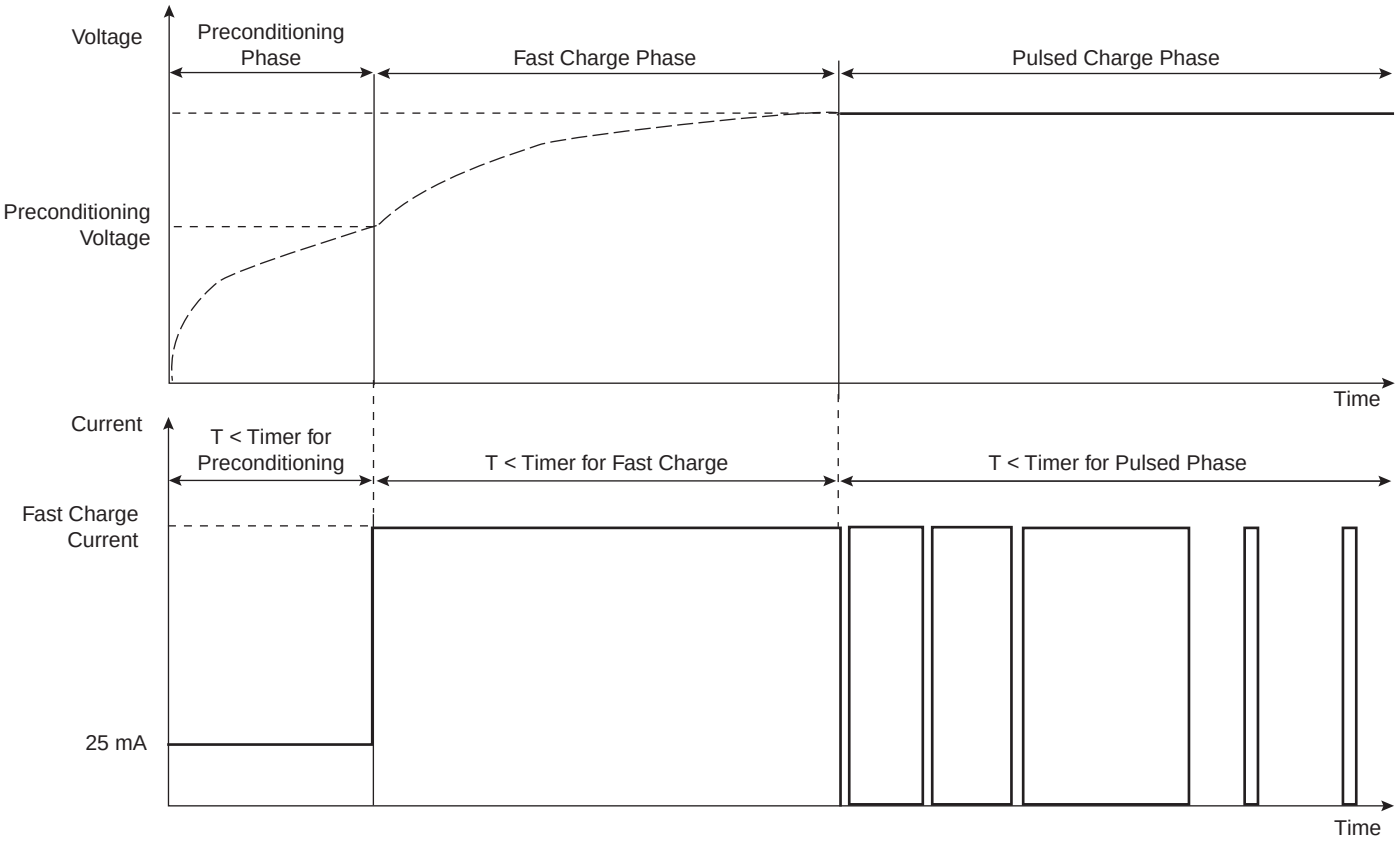


Controlled Mode

After the digital reset phase, the application processor can launch a charge phase. By default the charge phase is stopped when the application processor wakes up.

The charge control includes three charging phases (preconditioning, fast charge and pulsed charge) during which the application processor must check via the monitoring function that the operating temperature is within allowable limits for battery charging.

Figure 29. Controlled Mode



Preconditioning Phase

Battery 1 and Battery 2 can be preconditioned to a predetermined voltage from either the PSU or USB source. Precondition current is set to 25 mA.

To enable the precondition phase, the application processor must use the charger control register.

To program the preconditioning voltage threshold, the application processor must use an interrupt, which can be programmed for battery 1 and battery 2 with the over limit registers included in the monitoring function.

A safety timer (CHA_STR_CR) can be launched during this phase. If the safety timer expires, an interrupt is launched and the pre-conditioning phase is automatically stopped. If the pre-conditioning voltage threshold has been reached, the application processor should put the charger into the fast charge phase.

Fast Charge Phase

To enable the fast charge phase, the application processor must use the charger control register. The battery is charged at a constant current that can be adjusted (CHA_CURR in the CHA_MR in register). Note that battery 1 and battery 2 can not be in the fast charge phase at the same time.

The fast charge is automatically stopped when the battery voltage reaches the regulation voltage. The regulation voltage can be trimmed. By default, the voltage is 4.2V. When this voltage is reached an interrupt is sent to warn the microprocessor.

A safety timer (CHA_STR_CR) can be launched during this phase.

Pulsed Charge Phase

To enable the pulsed charge phase, the application processor must use the charger control register. Note that battery 1 and battery 2 can not be in pulsed charge phase at the same time.

The charger control uses a hysteretic algorithm with minimum on-times and minimum off-times of the external PMOS. These minimum on-times and off-times can be programmed via registers CHA_TMINON and CHA_TMINOFF.

The battery voltage is sampled every 0.3 millisecond (typical). If the battery voltage is less than the battery regulation voltage, the external PMOS FET either turns on or, if already on, remains on. If the battery voltage is greater than, or equal to, the regulation voltage threshold, the FET either turns off or, if already off, remains off until the next sample.

At the beginning of the pulsed charge phase, the current stays on for many consecutive cycles between single off periods. As the battery continues to charge, the percentage of time spent in the “current-on” mode decreases. At the end of the pulsed phase, the current stays off for many cycles between single “on” pulses.

This phase is automatically stopped when the duty ratio of “on” cycles to “off” cycles falls below a threshold which must be programmed trough register CHA_TR. Additionally, an interrupt is sent to warn the microprocessor.

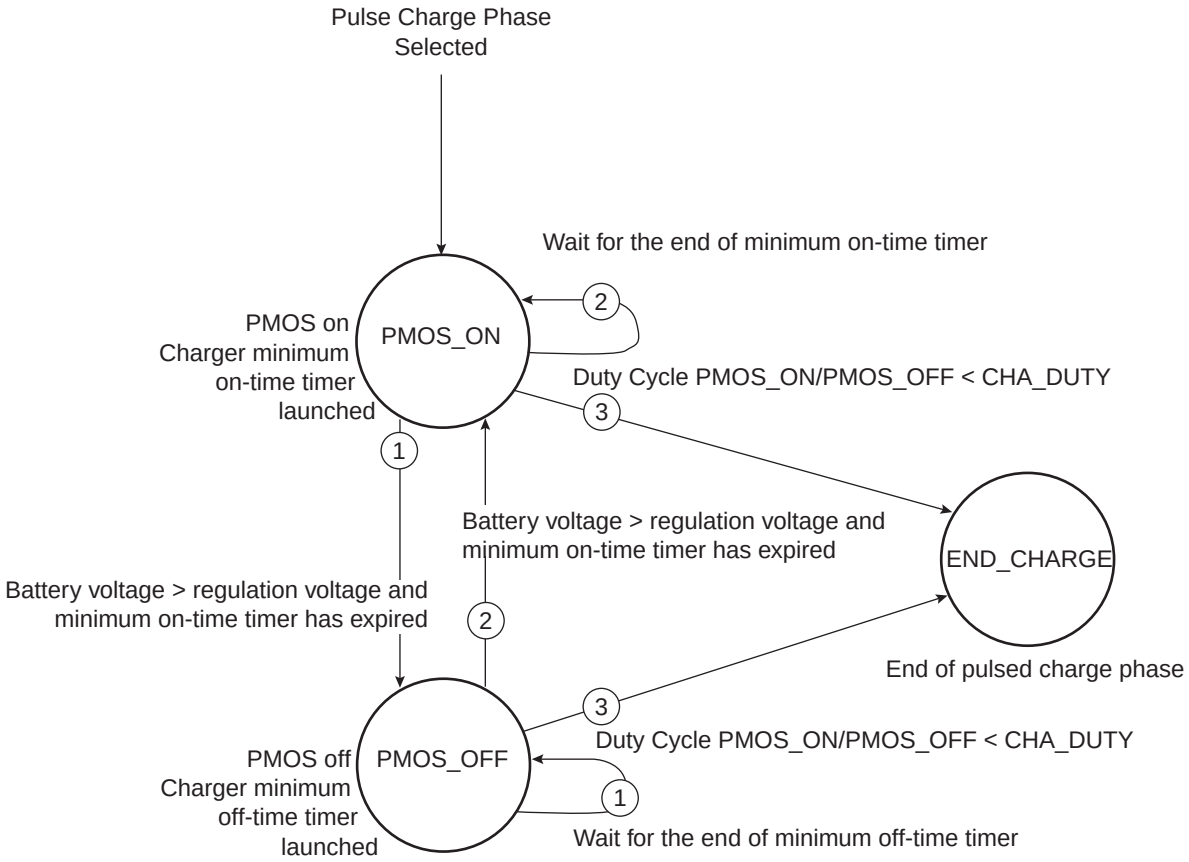
For safety, a timer (CHA_STR_CR) can be launched during this phase.

If this timer expires, an interrupt is launched and the pulsed charge phase is automatically stopped.

The “Start-up State Machine Pulsed Charge Phase” shown in Figure 30 on page 101 presents a summary of the pulsed charge phase. Refer also to the “State Machine Description” on page 15 for more information on the pulsed charge phase.

The parameters (CHA_TMINON, CHA_TMINOFF and CHA_TR) can be trimmed in order to be adapted to the battery. To properly choose the parameters, a test must been done with the real battery. At the end of top-off mode, it is preferable to use a small current (100 mA). A good default value seems to be 200 ms for CHA_TMINON and CHA_TMINOFF and a duty cycle threshold of 1/64.

Figure 30. Start-up State Machine Pulsed Charge Phase



Watchdog

For safety, during any phase of the controlled mode a watchdog is launched automatically. The application processor must rearm the watchdog via the charger control register, CHA_CR, at least every 13 s. If during 13 s (typical time), the watchdog has not been rearmed, the charge is stopped.

Charger Control Electrical Specifications

Table 30. Charger Control Electrical Specifications

Symbol	Parameter	Condition	Min	Typ	Max	Units
PSU	Charger Voltage		4.90	5.0	5.10	V
USB	USB Voltage		4.62	5.0	5.25	V
$I_{PRECOND}$	Preconditioning Current	USB or PSU		25		mA
I_{CH}	Charge Current	CHA_CURR = 11		500		mA
		CHA_CURR = 10		300		mA
		CHA_CURR = 01		200		mA
		CHA_CURR = 00		100		mA
V_{REGTH}	Regulation Voltage Threshold	CHA_VOLT_TRIM =000		4.20		V
		CHA_VOLT_TRIM =001		4.170		V
		CHA_VOLT_TRIM = 010		4.130		V
		CHA_VOLT_TRIM = 011		4.10		V
		CHA_VOLT_TRIM = 100		4.23		V
		CHA_VOLT_TRIM = 101		4.26		V
		CHA_VOLT_TRIM = 110		4.30		V
		CHA_VOLT_TRIM = 111		4.07		V
Hystbat1	Input hysteresis			2		mV
	Timer for stand alone mode			1		h
	Threshold voltage for stand alone mode			3.8		V
$t_{ACCURACY}$	Timing accuracy			±25		%
I_{CC}	Current consumption			1		mA

Power Dissipation

The internal power dissipation depends on the operating mode of the chip; thus, worst case mode is considered.

Table 31 gives power dissipation values (estimated).

Table 31. Power Dissipation (Estimated)

Block Name	Power Dissipation (Estimated) in mW
Power switch	50
Digital rails (DC/DC converters)	50
Charger	300
SIM regulator	120
Monitoring function	10
Core block + digital	20
TOTAL	550

Quiescent Current

The AT73C203 has two modes: off and active mode.

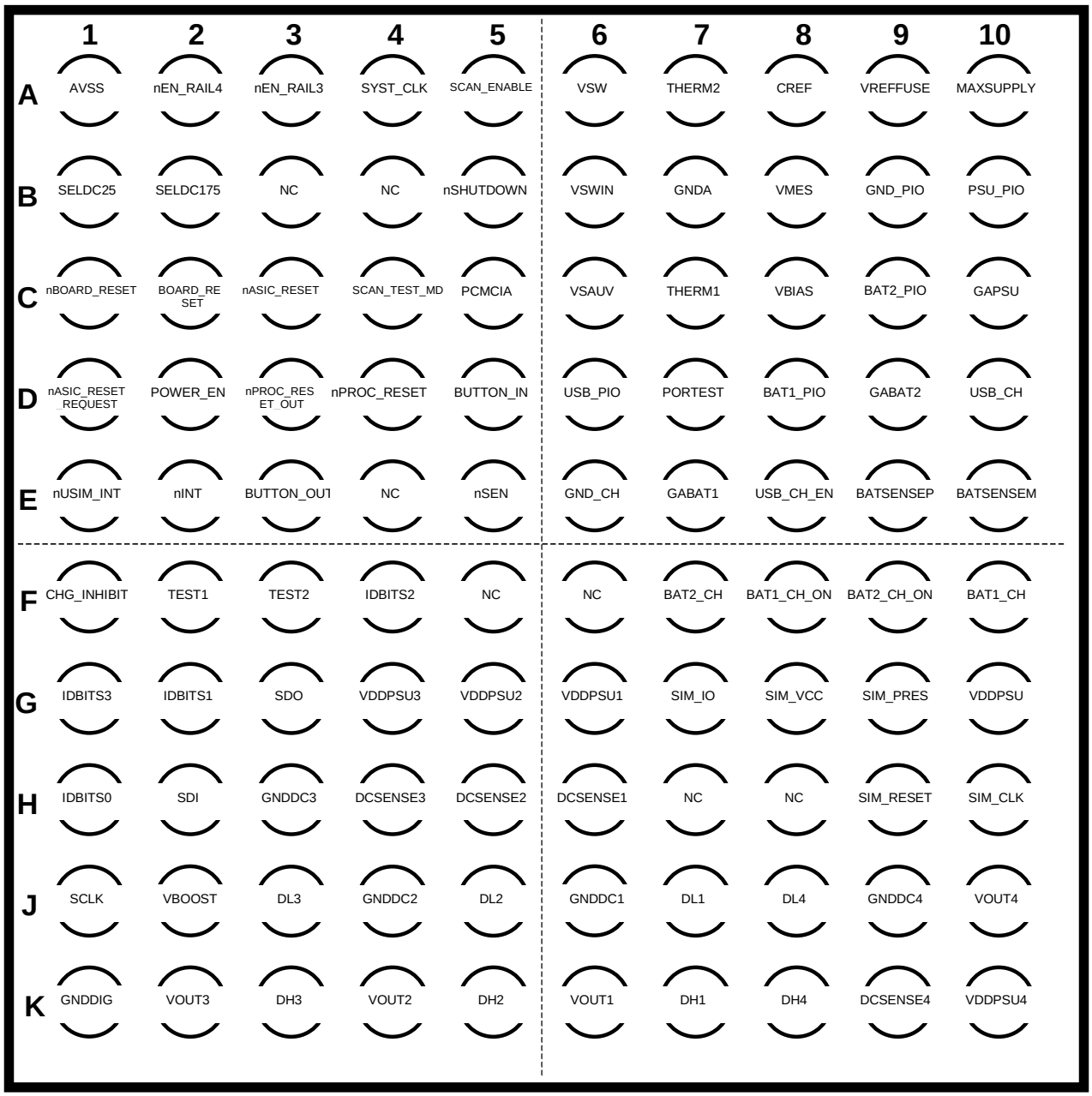
In off mode, the target is to achieve an off time of three months with a 600 mA fully-charged battery.

If the self discharge of the battery (maximum 50 µA) is taken into consideration, the maximum current of the AT73C203 in this mode must be below 220 µA.

Typical measure on Rev C: 70 µA.

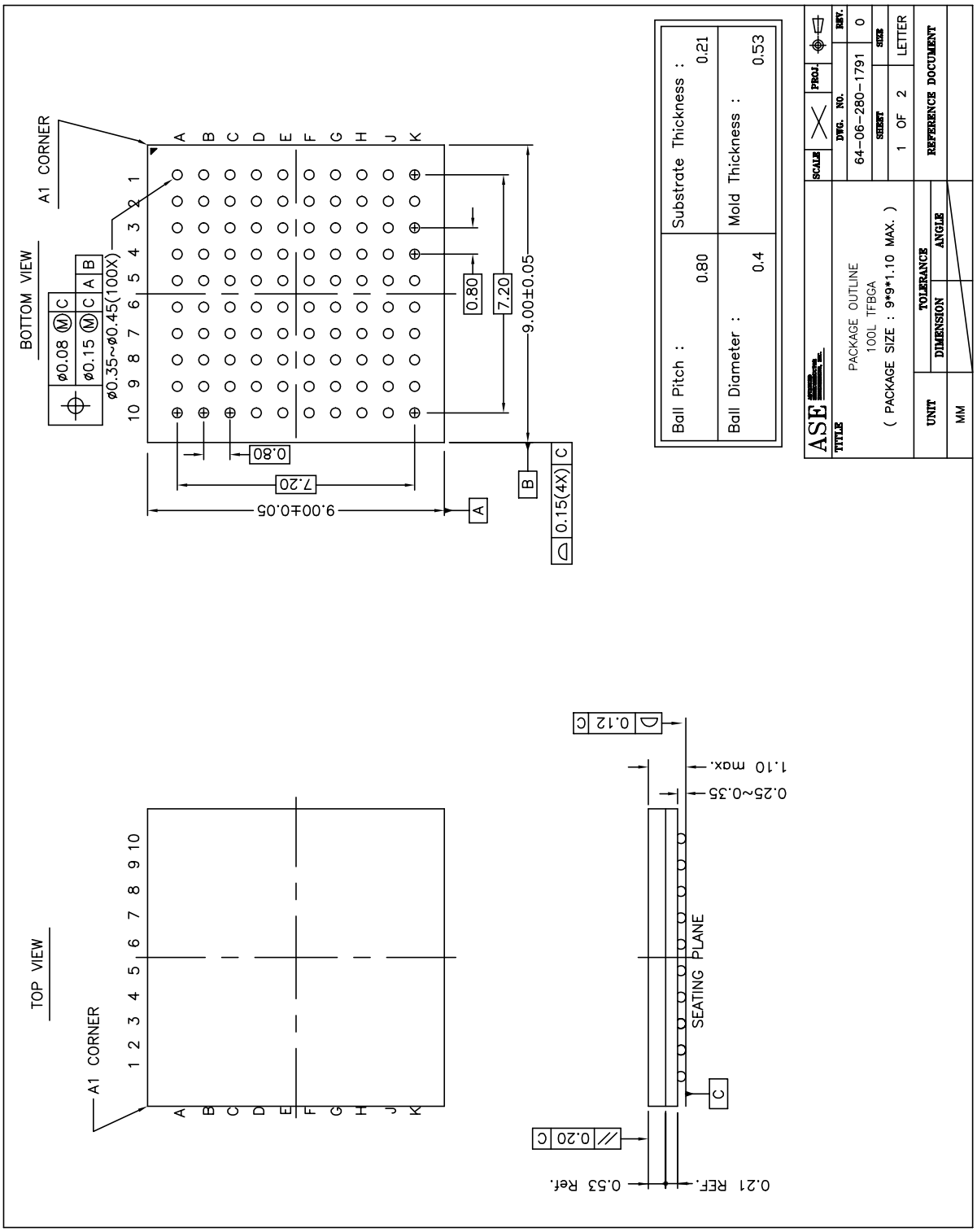
Package Outline (Top View)

Figure 31. 10 x 10 balls, 0.8mm Pitch BGA Package on 9 x 9mm Body Size for AT73C203



Package Specification

Figure 32. AT73C203 Package Specification



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