PJDLLLC05

Low Capacitance TVS Diode Array

This diode array is configured to protect up to two high speed data transmission lines, used in Low Voltage Differential Signal(LVDS) ports.Acting as a line terminator, minimizes overshoot and undershoot conditions due to bus impedance, as well as protect against over-voltage events as electrostatic discharges. The line-line concept minimizes the problems to customers to re-route PCB lines, simplifying the design.

FEATURES

- Maximum Capacitance of 1.2pF at 0Vdc 1MHz Line-to-Ground
- Maximum Leakage Current of 1.0uA @ V_{RWM}
- Industry Standard SMT Package SOT-563
- IEC61000-4-2 Full Compliance; 15kV air,8kV Contact
- 100% Tin Matte finish(LEAD-FREE PRODUCT)
- Lead free in comply with EU RoHS 2002/95/EC directives.
- Green molding compound as per IEC61249 Std. . (Halogen Free)

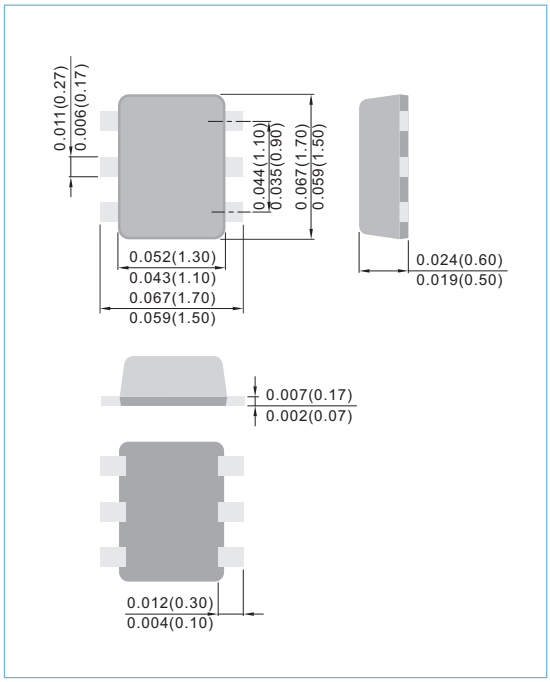
MECHANICAL DATA

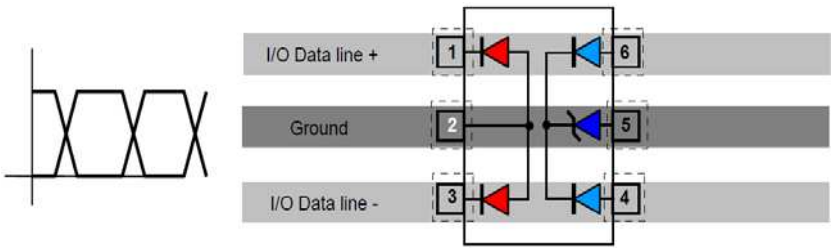
- Case: SOT-563, Plastic
- Terminals:Solder plated,solderable per MIL-STD-750,Method2026
- Appox Weight : 0.0026 grams, 0.00009 ounces

APPLICATIONS

- USB 2.0 and Firewire Port Protection
- HDMI Version 1.3
- DVI
- Marking:05

SOT-563 Unit : inch(mm)





Line-line concept ease the PCB design, directly placing the device over the data lines, opening only the contact points.

VREF is fixed by the operating voltage, referenced to the ground.

Note: pins 1and 6 (Line1), pins 3 and 4 (Line2) and pins 2 and 5 (Gnd) must be connected extemally, as the drawing attached below.

MAXIMUM RATINGS (T_J=25°C unless otherwise noted)

RATING	SYMBOL	VALUE	UNITS
Peak Pulse Power (8/20μs Waveform)	P_{PP}	75	W
Peak Pulse Current (8/20μs Waveform)	I_{PP}	5	A
Operating Temperature Range	T_J	-55 to 125	°C
Storage Temperature Range	T_{STG}	-55 to 150	°C
Soldering Temperature, t max=10s	T_L	260	°C

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ELECTRICAL CHARACTERISTICS (T_J=25°C unless otherwise noted)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Reverse Stand-Off Voltage	V_{RWM}	-	-	-	5	V
Reverse Breakdown Voltage	V_{BR}	I_{BR}=1mA	6.2	-	-	V
Reverse Leakage Current	I_R	V_R=5V	-	-	1.0	µA
Clamping Voltage (8/20µs)	V_C	I_{PP}=1A	-	-	10	V
Clamping Voltage (8/20µs)	V_C	I_{PP}=2A	-	-	12	V
Clamping Voltage (8/20µs)	V_C	I_{PP}=5A	-	-	15	V
Off State Junction Capacitance	C_J	0 Vdc Bias f=1MHz Between I/O pins and pin GND	-	-	1.2	pF
		0 Vdc Bias f=1MHz Between I/O pins	-	-	0.6	pF

ELECTRICAL CHARACTERISTIC CURVES

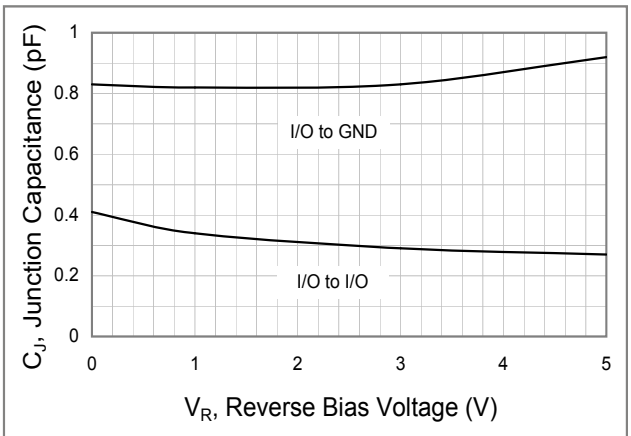

Fig.1 Typical Junction Capacitance

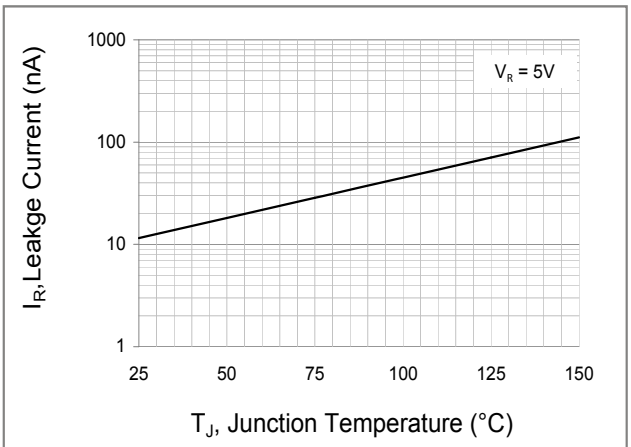

Fig.2 Typical Reverse Characteristics

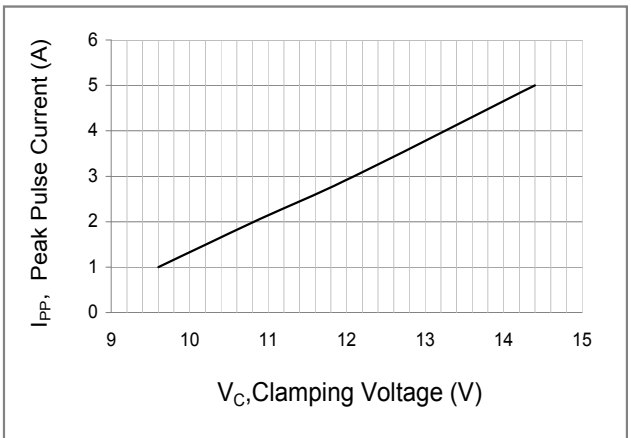

Fig.3 Typical Peak Clamping Voltage (8/20µs)

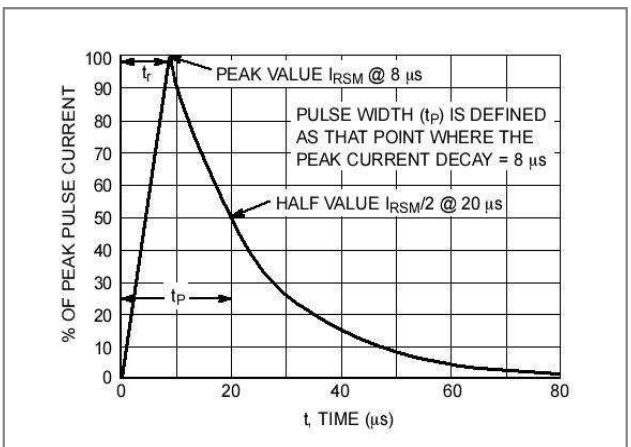

Fig.4 8/20µs Peak Pulse Current Waveform

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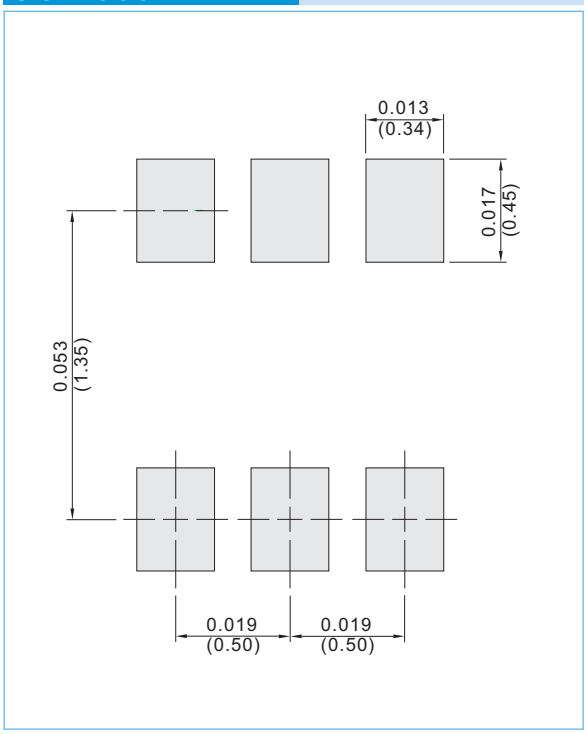
MOUNTING PAD LAYOUT

SOT-563 Unit : inch(mm)



ORDER INFORMATION

- Packing information

  T/R - 4K per 7" plastic Reel

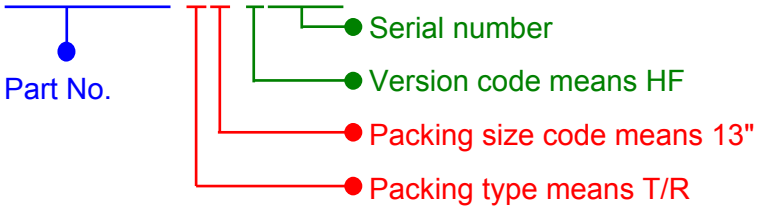
  T/R - 10K per 13" plastic Reel

LEGAL STATEMENT

PJDLLLC05

For example :

RB500V-40_R2_00001



Part No_packing code_Version

PJDLLLC05_R1_00001
PJDLLLC05_R1_10001
PJDLLLC05_R2_00001
PJDLLLC05_R2_10001

Packing Code XX				Version Code XXXXX		
Packing type	1st Code	Packing size code	2nd Code	HF or RoHS	1st Code	2nd~5th Code
T/B	A	N/A	0	HF	0	serial number
T/R	R	7"	1	RoHS	1	serial number
B/P	B	13"	2			
T/P	T	26mm	X			
TRR	S	52mm	Y			
TRL	L	PBCU	U			
FORMING	F	PBCD	D			