MKW22D512V

Package Information
Plastic Package 8x8 56-pin LGA
Case 2234-01

MKW22D512V

Also covers MKW21D512V and MKW21D256V

Ordering Information

Device	Program flash	System RAM	Package
MKW22D512V (USB)	512 K	64 K	8x8 56-pin LGA
MKW21D512V	512 K	64 K	8x8 56-pin LGA
MKW21D256V	256 K	32 K	8x8 56-pin LGA

1 Introduction

The MKW22D512 device consists of two separate ICs: a 2.4 GHz transceiver and a microcontroller. The MCU is done in the 90 nm thin film storage (TFS) process, is built from the Kinetis platform and is part of the Kinetis portfolio. The transceiver is built using a 180 nm process.

The primary target for the MKW22D512V portfolio is to meet the higher performance requirements of ZigBee Pro and ZigBee IP based applications, especially Smart Energy and Commercial Building Automation. This product is a cost-effective solution that matches or exceeds competitive solutions.

The following content describes the MKW22D512V.

The MKW22D512V portfolio consist of a system on chip for the IEEE® 802.15.4 standard that incorporates a complete, low power, 2.4 GHz 802.15.4 compliant radio frequency transceiver and a Kinetis family low power, mixed-signal ARM® eCortex™- M4 MCU, with a functional set of MCU peripherals integrated into a single package.

1.1 Ordering information

Table 1. Orderable parts details

Device	Program flash	System RAM
MKW22D512V (USB)	512 K	64 K
MKW21D512V	512 K	64 K
MKW21D256V	256 K	32 K

2 Features

This section provides a simplified block diagram and highlights MKW22D512V features.

2.1 Block diagram

Figure 1 shows a simplified block diagram of the MKW22D512V, which is an IEEE®802.15.4 standard compatible transceiver.

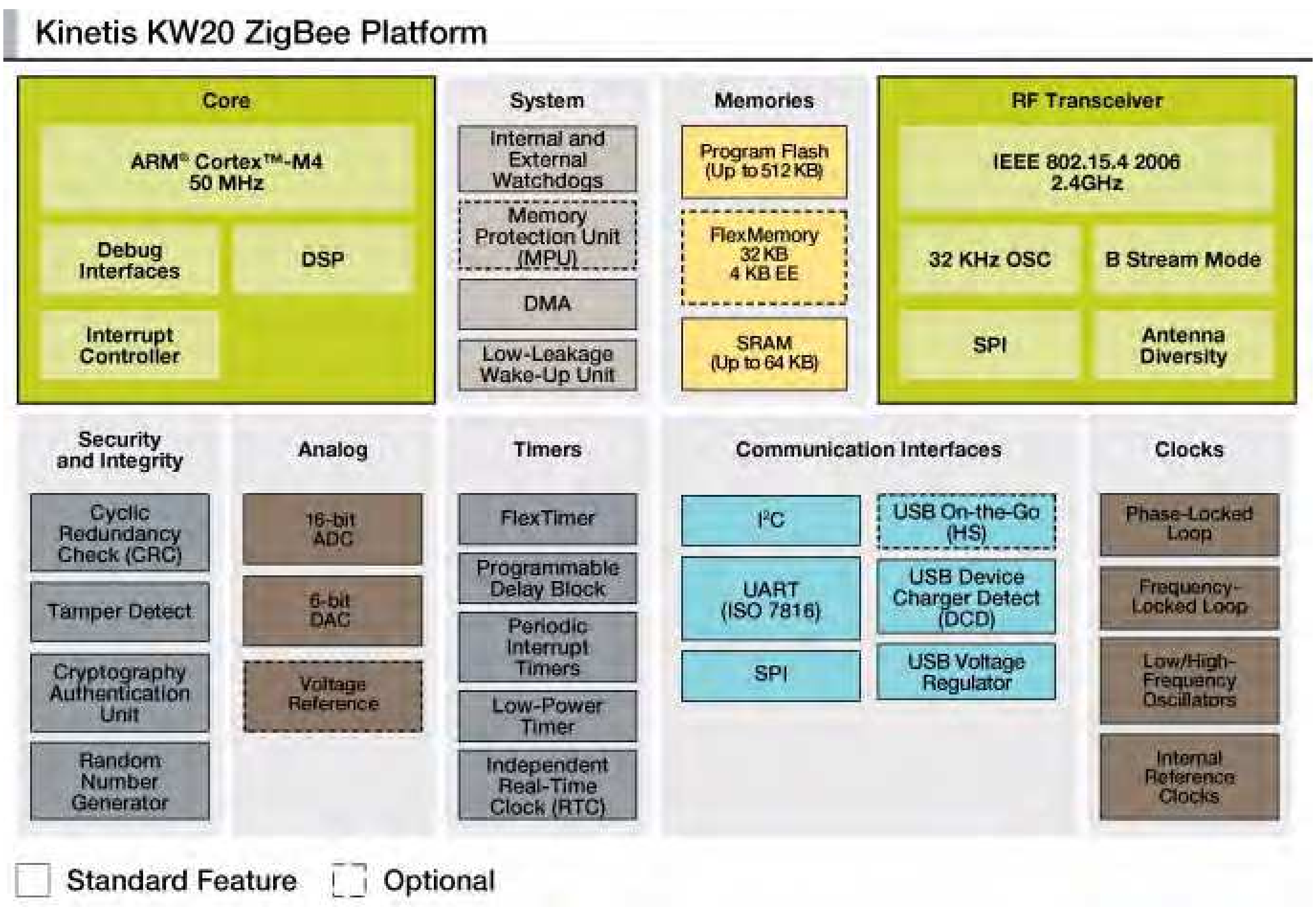


Figure 1. MKW22D512V simplified block diagram

2.2 Radio features

- 2.4 GHz frequency band of operation
- 250 kbps data rate with O-QPSK modulation in 5.0 MHz channels with direct sequence spread-spectrum (DSSS) encode and decode
- Operates on one of 16 selectable channels per IEEE 802.15.4 specification
- Programmable output power
- Supports 2.36 to 2.4 GHz Medical Band (MBAN) frequencies with same modulation as IEEE 802.15.4
- Small RF footprint
  - Differential input/output port used with external balun
  - Integrated transmit/receive switch
  - Supports single ended and diversity antenna options
  - Low external component count
  - Supports external PA and LNA
- Hardware acceleration for IEEE® 802.15.4 2006 packet processing
  - Random number generator
  - Support for dual PAN mode
- 32 MHz crystal reference oscillator with on board trim capability to supplement external load capacitors
- Programmable frequency clock output (CLK_OUT)
- Bit stream mode (BSM) to monitor packet data with synchronization clock
- Advanced Security Module with support for AES encryption
- GPIO for Antenna Diversity control
- Clocks
  - 32 MHz crystal oscillator
  - Internal 1 kHz low power oscillator
  - DC to 32 MHz external square wave input clock

2.3 Microcontroller features

In addition all MKW22D512V devices contain the below microcontroller features:

- Core:
  - ARM Cortex-M4 Core delivering 1.25 DMIPS/MHz with DSP instructions (floating-point unit available on certain Kinetis families)
  - 16-channel DMA for peripheral and memory servicing with minimal CPU intervention
- Reliability, Safety and Security:
  - Hardware cyclic redundancy check engine for validating memory contents/communication data and increased system reliability
  - Independent-clocked COP for protection against code runaway in fail-safe applications

- External watchdog monitor
- Analog tamper detects (voltage, temperature, and clock)
- External tamper detect
- 256-bit secure storage (asynchronously erased on tamper detect)

- Ultra-low power:
  - 10 low power operating modes for optimizing peripheral activity and wake-up times for extended battery life.
  - Low–leakage wake-up unit, low power timer, and low power RTC for additional low power flexibility
  - Industry-leading fast wake-up times
- Memory:
  - FlexMemory with up to 512 KB FlexNVM and up to 4 KB FlexRAM. FlexNVM can be partitioned to support additional program flash memory (ex. bootloader), data flash (ex. storage for large tables), or EEPROM backup. FlexRAM supports
  - EEPROM byte-write/byte-erase operations and dictates the maximum EEPROM size.
  - EEPROM endurance capable of exceeding 10 million cycles
  - EEPROM erase/write times an order of magnitude faster than traditional EEPROM
- Connectivity and Communications:
  - UART, I2C and DSPI
- Mixed-signal analog:
  - Fast, high precision 16-bit ADC. Powerful signal conditioning, conversion and analysis capability with reduced system cost
- Timing and Control:
  - Powerful FlexTimers which support general purpose, PWM, and motor control functions
  - Programmable Interrupt Timer for RTOS task scheduler time base or trigger source for ADC conversion and programmable delay block
- System:
  - Wide operating voltage range from 1.8 V to 3.6 V with flash programmable down to 1.8 V with fully functional flash and analog peripherals
  - Ambient operating temperature ranges from –40°C to 105°C

MKW22D512V devices are supported by a market-leading enablement bundle from Freescale and numerous ARM 3rd party ecosystem partners.

Common features among the MKW22D512V family:

- Operating characteristics
  - Voltage range 1.8 V – 3.6 V
  - Flash memory programming down to 1.8 V
  - Temperature range (TA) –40 to 105°C
  - Flexible modes of operation

- Core features
  - Next generation 32-bit ARM Cortex-M4 core
  - Supports DSP instructions
  - Nested vectored interrupt controller (NVIC)
  - Asynchronous wake-up interrupt controller (AWIC)
  - Debug and trace capability
    - 2-pin serial wire debug (SWD)
    - IEEE 1149.1 Joint Test Action Group (JTAG)
    - IEEE 1149.7 compact JTAG (cJTAG)
    - Trace port interface unit (TPIU)
    - Flash patch and breakpoint (FPB)
    - Data watchpoint and trace (DWT)
    - Instrumentation trace macrocell (ITM)
    - Enhanced Trace Macrocell (ETM)
- System and power management
  - Software and hardware watchdog with external monitor pin
  - DMA controller with 16 channels
  - Low-leakage wake-up unit (LLWU)
  - Power management controller with 10 different power modes
  - Non-maskable interrupt (NMI)
  - 128-bit unique identification (ID) number per chip
- Clocks
  - Multi-purpose clock generator
    - PLL and FLL operation
    - Internal reference clocks (32 kHz or 2 MHz)
  - Three separate crystal oscillators
    - 3 MHz to 32 MHz crystal oscillator for MCU
    - 32 kHz to 40 kHz crystal oscillator for MCU or RTC
    - 32 MHz crystal oscillator for Radio
  - Internal 1 kHz low power oscillator
  - DC to 50 MHz external square wave input clock
- Memories and Memory Interfaces
  - FlexMemory consisting of FlexNVM (non-volatile flash memory that can execute program code, store data, or backup EEPROM data) or FlexRAM (RAM memory that can be used as traditional RAM or as high-endurance EEPROM storage, and also accelerates flash programming)
  - Flash security and protection features
  - Serial flash programming interface (EzPort)

- Security and integrity
    - Cyclic redundancy check (CRC)
    - Tamper detect
    - Hardware encryption
    - AES128 Hardware encryption
- Analog
    - 16-bit SAR ADC
    - High-speed Analog comparator (CMP) with 6-bit DAC
- Timers
    - Up to 12 channels; 7 channels support external connections; 5 channels are internal only
    - Carrier modulator timer (CMT)
    - Programmable delay block (PDB)
    - 1x4ch programmable interrupt timer (PIT)
    - Low-power timer (LPT)
- Communications
    - SPI
    - I2C with SMBUS support
    - UART (w/ ISO7816, IrDA and hardware flow control)
- Human-machine interface
    - GPIO with pin interrupt support, DMA request capability, digital glitch filter, and other pin control options

3 Transceiver description

3.1 Key specifications

MKW22D512V meets or exceeds all IEEE 802.15.4 performance specifications applicable to 2.4 GHz ISM and MBAN (Medical Band Area Network) bands. Key specifications for MKW22D512V are:

- ISM band:
    - RF operating frequency: 2405 MHz to 2480 MHz (center frequency range)
    - ISM Channel numbering: Fc = 2405 + 5 (k – 11) in MHz, k = 11, 12, …, 26.
- MBAN band:
    - RF operating frequency: 2360 MHz to 2400 MHz (center frequency range)
    - MBANS channel page 9 is (2360 MHz–2390 MHz band)
    - Fc = 2363.0 + 1.0 * k in MHz for k = 0......26
    - MBANS channel page 10 is (2390 MHz–2400 MHz band)
    - Fc = 2390.0 + 1.0 * k in MHz for k = 0......8
- IEEE 802.15.4 Standard 2.4 GHz modulation scheme
    - Chip rate: 2000 kbps

- Data rate: 250 kbps
- Symbol rate: 62.5 kbps
- Modulation: OQPSK

- Receiver sensitivity: –102 dBm, typical(@1% PER for 20 byte payload packet)
- Differential bidirectional RFinput/output port with integrated transmit/receive switch
- Programmable output power from –30 dBm to +10 dBm.

3.2 RF interface and usage

The MKW22D512V RF output ports are bidirectional (diplexed between receive/transmit modes) and differential enabling interfaces with numerous off-chip devices such as a balun. When using a balun, this device provides an interface to directly connect between a single-ended antenna with MKW22D512V RF ports. In addition, MKW22D512V provides four output driver ports that can have both drive strength and slew rate configured to control external peripheral devices. These signals designated ANT_A, ANT_B, RX_SWITCH, and TX_SWITCH when enabled are switched via an internal hardware state machine. These ports provide control features for peripheral devices such as:

- Antenna diversity modules
- External PAs
- External LNAs
- T/R switched

3.2.1 Clock output feature

The CLK_OUT digital output can be enabled to drive the system clock to the MCU. This provides a highly accurate clock source based on the transceiver reference oscillator. The clock is programmable over a wide range of frequencies divided down from the reference 32 MHz (see Table 3).The CLK_OUT pin will be enabled upon POR. The frequency CLK_OUT will be determined by the state of the GPIO5/BOPT pin. If this pin is low upon POR, then the frequency will be 4 MHz (32 MHz/8). If this pin is high upon POR (upon POR GPIO5 has a pullup resistor) then the frequency will be 32.78689 kHz (32 MHz/976).

3.3 Transceiver functions

3.3.1 Receive path

The receive path has the functionality to operate in run state or operate in a low power run state (LPRS) that can be considered as a partial power down mode. The radio receiver path is based upon a near zero IF (NZIF) architecture incorporating front end amplification, one(1) mixed signal down conversion to IF that is programmably filtered, demodulated and digitally processed. The RF front end (FE) input port is differential that shares the same off chip matching network with the transmit path.

3.3.2 Transmit path

MKW22D512V transmits OQPSK modulation having power and channel selection adjustment per user application. After the channel of operation is determined, coarse and fine tuning is executed within the Frac-N PLL to engage signal lock. After signal lock is established, the modulated buffered signal is then routed to a multi-stage amplifier for transmission. The differential signals at the output of the PA (RFOUTP, RFOUTN) are converted as single ended (SE) signals with off chip components as required.

3.3.3 Clear channel assessment (CCA), energy detection (ED), and link quality indicator (LQI)

MKW22D512V supports three clear channel assessment (CCA) modes of operation to include energy detection (ED) and link quality indicator (LQI). Functionality for each of these modes is provided in the sections that follow.

3.3.3.1 CCA mode 1

CCA mode 1 has two functions:

- To estimate the energy in the received baseband signal. This energy is estimated based on receiver signal strength indicator (RSSI).
- To determine whether the energy is greater than a threshold.

The estimate of the energy can also be used as the Link Quality metric. In CCA Mode 1, MKW22D512V warms up from Idle to Receive mode where RSSI (Receiver Signal Strength Indicator) averaging takes place right after 170μs of receiver warm-up.

3.3.3.2 CCA mode 2

CCA mode 2 detects whether there is any 802.15.4 signal transmitting at the frequency band that an 802.15.4 transmitter intends to transmit. From the definition of CCA mode 2 in the 802.15.4 standard, the requirement is to detect an 802.15.4 complied signal. Whether the detected energy is strong or not is not important for CCA mode 2.

3.3.3.3 CCA mode 3

CCA mode 3 as defined by 802.15.4 standard is implemented using a logical combination of CCA mode 1 and CCA mode 2. Specifically, CCA mode 3 operates in one of two operating modes:

- CCA mode 3 is asserted if both CCA mode 1 and CCA mode 2 are asserted.
- CCA mode 3 is asserted if either CCA mode 1 or CCA mode 2 is asserted.

This mode setting is available through a programmable register.

3.3.3.4 Energy detection (ED)

Energy detection (ED) is based on receiver signal strength indicator (RSSI) and correlator output for the 802.15.4 standard. energy detect (ED) is an average value of signal strength. The magnitude from this measurement is calculated from the digital RSSI value that is averaged over an 128 μs duration.

3.3.3.5 Link quality indicator (LQI)

Link quality indicator (LQI), is based on receiver signal strength indicator (RSSI) or correlator output for the 802.15.4 standard. In this mode, RSSI measurement is done during normal packet reception. LQI computations for MKW22D512V are based on either digital RSSI or correlator peak values. This setting is executed through a register bit where the final LQI value is available 64 μs after preamble is detected. If a continuous update of LQI based on RSSI throughout the packet is desired, it can be read in a separate 8-bit register by enabling continuous update in a register bit.

3.3.4 Packet processor

The MKW22D512V packet processor performs sophisticated hardware filtering of the incoming received packet, to determine whether the packet is both PHY- and MAC-compliant, whether the packet is addressed to this device, and if the device is a PAN coordinator, whether a message is pending for the sending device. The packet processor greatly reduces the packet filtering burden on software, allowing software to tend to higher-layer tasks with a lower latency and smaller software footprint.

3.3.4.1 Features

- Aggressive packet filtering to enable long, uninterrupted MCU sleep periods
- Fully compliant with both 2003 and 2006 versions of the 802.15.4 wireless standard
- Supports all frame types, including reserved types
- Supports all valid 802.15.4 frame lengths
- Enables auto-Tx acknowledge frames (no MCU intervention) by parsing of frame control field and sequence number
- Supports all source and destination address modes, and also PAN ID compression
- Supports broadcast address for PAN ID and short address mode
- Supports “promiscuous” mode, to receive all packets regardless of address- and rules-checking
- Allows frame type-specific filtering (e.g., reject all but beacon frames)
- Supports SLOTTED and non-SLOTTED modes
- Includes special filtering rules for PAN coordinator devices
- Enables minimum-turnaround Tx-acknowledge frames for data-polling requests by automatically determining message-pending status
- Assists MCU in locating pending messages in its indirect queue for data-polling end devices
- Makes available to MCU detailed status of frames that fail address- or rules-checking.
- Supports Dual PAN mode, allowing the device to exist on 2 PAN’s simultaneously
- Supports 2 IEEE addresses for the device

- Supports active promiscuous mode

3.3.5 Packet buffering

The packet buffer is a 128-byte random access memory (RAM) dedicated to the storage of 802.15.4 packet contents for both TX and RX sequences. For TX sequences, software stores the contents of the packet buffer starting with the frame length byte at packet buffer address 0, followed by the packet contents at the subsequent packet buffer addresses. For RX sequences the incoming packet's frame length is stored in a register, external to the packet buffer. Software will read this register to determine the number of bytes of packet buffer to read. This facilitates DMA transfer through the SPI. For receive packets, an LQI byte is stored at the byte immediately following the last byte of the packet (frame length +1). Usage of the packet buffer for RX and TX sequences is on a time-shared basis; receive packet data will overwrite the contents of the packet buffer. Software can inhibit receive-packet overwriting of the packet buffer contents by setting the PB_PROTECT bit. This will block RX packet overwriting, but will not inhibit TX content loading of the packet buffer via the SPI.

3.3.5.1 Features

- 128 byte buffer stores maximum length 802.15.4 packets
- Same buffer serves both TX and RX sequences
- The entire Packet Buffer can be uploaded or downloaded in a single SPI burst.
- Automatic address auto-incrementing for burst accesses
- Single-byte access mode supported.
- Entire packet buffer can be accessed in hibernate mode
- Under-run error interrupt supported

3.4 Dual PAN ID

In the past, radio transceivers designed for 802.15.4 and ZigBee applications allowed a device to associate to one and only one PAN (Personal Area Network) at any given time. MKW22D512V represents a high-performance SoC that includes hardware support for a device to reside in two networks simultaneously. In optional Dual PAN mode, the device alternates between the two (2) PANs under hardware or software control. Hardware support for Dual PAN operation consists of two (2) sets of PAN and IEEE addresses for the device, two (2) different channels (one for each PAN), a programmable timer to automatically switch PANs (including on-the-fly channel changing) without software intervention. There are control bits to configure and enable Dual PAN mode and read only bits to monitor status in Dual PAN mode. A device can be configured to be a PAN coordinator on either network, both networks, or neither.

For the purpose of defining PAN in the content of Dual PAN mode, two (2) sets of network parameters are maintained, PAN0 and PAN1. PAN0 and PAN1 will be used to refer to the two (2) PANs where each parameter set uniquely identifies a PAN for Dual PAN mode. These parameters are described in Table 2.

Table 2. PAN0 and PAN1 descriptions

PAN0	PAN1
Channel0 (PHY_INT0, PHY_FRAC0)	Channel1 (PHY_INT1, PHY_FRAC1)
MacPANID0 (16-bit register)	MacPANID1 (16-bit register)
MacShortAddrs0 (16-bit register)	MacShortAddrs1 (16-bit register)
MacLongAddrs0 (64-bit registers)	MacLongAddrs1 (64-bit registers)
PANCORDNTR0 (1-bit register)	PANCORDNTR1 (1-bit register)

During device initialization if Dual PAN mode is used, software will program both parameter sets to configure the hardware for operation on two (2) networks.

4 System and power management

The MKW22D512V is a low power device that also supports extensive system control and power management modes to maximize battery life and provide system protection.

4.1 Modes of operation

The transceiver modes of operation include:

- Idle mode
- Doze mode
- Low power (LP) / hibernate mode
- Reset / powerdown mode
- Run mode

4.2 Power management

The MKW22D512V power management is controlled through programming the modes of operation. Different modes allow for different levels of power-down and RUN operation. For the receiver, programmable power modes available are:

- Receiver modes of operation:
  - RX preamble search
  - RX Preamble search sniff
  - X FAD Preamble search
  - RX packet decoding
- The RF section of the radio only powered-up asrequired to do a TX, RX, or CCA/ED operation.

5 Radio Peripherals

The MKW22D512V provides a set of I/O pins useful for suppling a system clock to the MCU, controlling external RF modules/circuitry, and GPIO. In addition, there is a special option for streaming the digital packet data for external monitoring (BSM).

5.1 Clock output (CLK_OUT)

MKW22D512V integrates a programmable clock to source numerous frequencies for connection with various MCUs. Package pin 39 can be used to provide this clock source as required allowing the user to make adjustments per their application requirement.

The transceiver CLK_OUT pin is internally connected to the MCU EXTAL pin so that no external connection is needed to drive the MCU clock.

Care must be taken that the clock output signal does not “talk” or interfere with the reference oscillator or the radio. Additional functionality this feature supports is:

- 3 clock domains (XTAL, SCLK, SDM_CK).
- Built in synchronization at all clock domain crossings.
- Aggressive clock gating in the XTAL domain to minimize dynamic current consumption based on the power mode selected.
- XTAL domain can be completely gated off (hibernate mode)
- SPI communication allowed in hibernate
- Single-clock domain in scan mode

Table 3. CLK_OUT table

CLK_OUT_DIV [2:0]	CLK_OUT frequency	Comments
0	32 MHz	
1	16 MHz	
2	8 MHz	
3	4 MHz	DEFAULT if GPIO5/BOPT=0
4	2 MHz	
5	1 MHz	
6	62.5 kHz	
7	32.786 kHz	DEFAULT if GPIO5/BOPT=1

There is an enable and disable bit for CLK_OUT. When disabling, the clock output will optionally continue to run for 128 clock cycles after disablement. There will also be one (1) bit available to adjust the CLK_OUT I/O pad drive strength.

5.2 Bit streaming mode (BSM)

Another peripheral option is bit streaming mode that when activated allows all 802.15.4 packet data, received or transmitted, to be serialized and shifted out to external hardware for further processing. A simple development system can be crafted to consume the BSM outputs and generate packet trace data for all 802.15.4 traffic appearing on a network within the range of the MKW22D512V device allowing for PAN-level monitoring and debugging.

BSM uses a simple synchronous 3-wire interface consisting of BSM_CLK, BSM_DATA, and BSM_FRAME outputs. Packet data is shifted out serially at the 802.15.4 bit rate (250 kHz). Signaling is provided on BSM_FRAME to indicate start-of-packet and end-of-packet and to discriminate between TX and RX packet types. BSM_DATA and BSM_FRAME are synchronous to BSM_CLK. BSM_DATA and BSM_FRAME are shifted out on the falling BSM_CLK and intended to be captured on rising BSM_CLK.

A single shift register control bit activates or deactivates BSM. Aside from controlling this bit, BSM requires no software support while the mode is engaged. BSM outputs are multiplexed with GPIO, so that the pins are available for general-purpose use when BSM is disabled. BSM does not interfere with packet processing or transmit data handling in any way, it is merely a monitoring tool. BSM when engaged will not measurably increase current consumption because the hardware (including the external I/O) operates at the 250 kHz rate.

5.3 General-purpose input output (GPIO)

MKW22D512V embedded transceiver supports up to 8 GPIO pins where all I/O pins will have the same supply voltage, which depending on the battery can vary from 1.8 V up to 3.6 V. Not all 8 are available on the MKW22D512V. When a die pin is configured as a general-purpose output or for peripheral use, there will be specific settings required per use case. Pin configuration will be executed by software to adjust input/output direction and drive strength, capability. When a die pin is configured as a general-purpose input or for peripheral use, software (see Table 4) can enable a pull-up or pull-down device. Immediately after reset, all pins are configured as high-impedance general-purpose inputs with “internal pull-up or pull-down devices enabled”.

Features for these pins include:

- Programmable output drive strength
- Programmable output slew rate
- Hi-Z mode
- Programmable as outputs or inputs (default)
- Pins shared with BSM mode outputs

Table 4. Pin configuration summary

Pin function configuration	Details	Tolerance			Units
		Min.	Typ.	Max.	
I/O buffer full drive mode[1]	Source or sink	—	±10	—	mA
I/O buffer partial drive mode[2]	Source or sink	—	±2	—	mA
I/O buffer high impedance[3]	Off state	—	—	10	nA
No slew, full drive	Rise and fall time[4]	2	4	6	ns
No slew, partial drive	Rise and fall time	2	4	6	ns
Slew, full drive	Rise and fall time	6	12	24	ns
Slew, partial drive	Rise and fall time	6	12	24	ns
Propagation delay[5], no slew	Full drive[6]	—	—	11	ns
Propagation delay, no slew	Partial drive[7]	—	—	11	ns
Propagation delay, slew	Full drive	—	—	50	ns
Propagation delay, slew	Partial drive	—	—	50	ns

1 For this drive condition, the output voltage will not deviate more than 0.5 V from the rail reference VOH or VOL.
2 For this drive condition, the output voltage will not deviate more than 0.5 V from the rail reference VOH or VOL.
3 Leakage current applies for the full range of possible input voltage conditions.
4 Rise and fall time values in reference to 20% and 80%
5 Propagation Delay measured from/to 50% voltage point.
6 Full drive values provided are in reference to a 75 pF load.
7 Partial drive values provided are in reference to a 15 pF load.

5.3.1 Serial peripheral interface (SPI)

MKW22D512V’s SPI interface allows an MCU to communicate with MKW22D512V’s register set and packet buffer. The SPI is a slave-only interface; the MCU must drive R_SSEL_B, R_SCLK and R_MOSI. Write and read access to both direct and indirect registers is supported, and transfer length can be single-byte, or bursts of unlimited length. Write and read access to the Packet buffer can also be single-byte, or a burst mode of unlimited length. The SPI interface is asynchronous to the rest of the IC. No relationship between R_SCLK and MKW22D512V’s internal oscillator is assumed. And no relationship between R_SCLK and the CLK_OUT pin is assumed. All synchronization of the SPI interface to the IC takes place inside the SPI module. SPI synchronization takes place in both directions: SPI-to-IC (register writes), and IC-to-SPI (register reads). The SPI is capable of operation in all power modes, except Reset. Operation in hibernate mode allows most MKW22D512V registers and the complete packet buffer to be accessed in the lowest-power operating state enabling minimal power consumption, especially during the register-initialization phase of the IC. The SPI design features a compact, single-byte control word, reducing SPI access latency to a minimum. Most SPI access types require only a single-byte control word, with the address embedded in the control word. During control word transfer (the first byte of any SPI access), the contents of the IRQSTS1 register (MKW22D512V’s highest-priority status register) are always shifted out, so that the MCU gets access to IRQSTS1, with the minimum possible latency, on every SPI access.

5.3.1.1 Features

- 4-wire industry standard interface, supported by all MCUs
- SPI R_SCLK maximum frequency 16 MHz (for SPI write accesses).
- SPI R_SCLK maximum frequency 9 MHz (for SPI read accesses).
- Write and read access to all Coconino registers (direct and indirect)
- Write and read access to packet buffer
- SPI accesses can be single-byte or burst.
- Automatic address auto-incrementing for burst accesses
- The entire packet buffer can be uploaded or downloaded in a single SPI burst.
- Entire packet buffer, and most registers, can be accessed in hibernate mode
- Built-in synchronization inside the SPI module to/from the rest of the IC.
- R_MISO can be tristated when SPI inactive, enabling multi-slave configurations

5.3.2 Antenna diversity

To improve the reliability of RF connectivity to long range applications, the antenna diversity feature is supported without using the MCU through use of four dedicated control pins (package pins 44, 45, 46, and 47) by direct register antenna selection. The digital regulator supplies bias to analog switches that can be programmed to sink and source current or operate in a high impedance mode.

Fast antenna diversity (FAD) mode supports this radio feature and, when enabled, will allow the choice of selection between two antennas during the preamble phase. By continually monitoring the received signal, the FAD block will select the first antenna on which the received signal has a correlation factor above a predefined progammable threshold. The FAD accomplishes the antenna selection by sequentially switching between the two antennas testing for the presence of a suitably strong signals/symbols where the first antenna to reach this condition is then selected for the reception of the packet.

The first antenna is monitored for a period equal to 1 symbol, t_s = 16 μs, then antenna monitoring is switched to the second antenna, t_a = 8 μs. The period t_a is required to allow for the external module control circuitry to turn on/off to select the antenna. $t_s + t_a$ = 24 μs that will allow enough time to test both antennas within the first 4 preamble symbols, $t_{fad} = 3 \times t_a + 2 \times t_s$ = 56 μs, thus $t_{fad} < 4 \times t_s$ < 64 μs. Operationally, FAD will continue to switch between the two antennas until one is found that has a sufficiently strong detected signal. FAD's operation covers less than four s0 symbols before the antenna that is selected allowing the symbol demodulator to detect at least four s0 symbols before declaring "Preamble Detect".

6 MKW22D512V operating modes

The radio has these 6 operating modes:

- Reset / power down
- Low power (LP) / hibernate
- [illegible]

(low power with reference oscillator active)

- Idle
- Receive
- Transmit

Table 5 lists and describes these modes.

Table 5. Radio mode definitions and transition times

Mode	Definition	Current consumption[1]	Transition time to or from idle
Reset / powerdown	All IC functions off, leakage only. $\overline{RST}$ asserted.	< 30 nA	TBD
Low power / hibernate	Crystal reference oscillator off. (SPI is functional.)	< 1 µA	TBD
Doze	Crystal reference oscillator on but CLK_OUT output available only if selected.	600 µA (no clockout)	TBD
Idle	Crystal reference oscillator on with CLK_OUT output available.	700 µA (no clockout)	TBD
Receive	Crystal reference oscillator on. Receiver on.	15 mA [2]	TBD
Transmit	Crystal reference oscillator on. Transmitter on.	15 mA [3]	TBD

[1] Conditions: VBAT and VBAT_2 = 2.7 V, nominal process @ 25°C

[2] Signal sensitivity = –102 dBm

[3] RF output = 0 dBm

The MCU has these radio modes:

Table 6. MCU power modes

Chip mode	Description	Core mode	Normal recovery method
Normal run	Allows maximum performance of chip. Default mode out of reset; on-chip voltage regulator is on.	Run	-

Table continues on the next page...

Chip mode	Description	Core mode	Normal recovery method
Normal Wait - via WFI	Allows peripherals to function while the core is in sleep mode, reducing power. NVIC remains sensitive to interrupts; peripherals continue to be clocked.	Sleep	Interrupt
Normal Stop - via WFI	Places chip in static state. Lowest power mode that retains all registers while maintaining LVD protection. NVIC is disabled; AWIC is used to wake up from interrupt; peripheral clocks are stopped.	Sleep Deep	Interrupt
VLPR (Very Low Power Run)	On-chip voltage regulator is in a low power mode that supplies only enough power to run the chip at a reduced frequency. Reduced frequency Flash access mode (1 MHz); LVD off; internal oscillator provides a low power 4 MHz source for the core, the bus and the peripheral clocks.	Run	Interrupt
VLPW (Very Low Power Wait) -via WFI	Same as VLPR but with the core in sleep mode to further reduce power; NVIC remains sensitive to interrupts (FCLK = ON). On-chip voltage regulator is in a low power mode that supplies only enough power to run the chip at a reduced frequency.	Sleep	Interrupt
VLPS (Very Low Power Stop)-via WFI	Places chip in static state with LVD operation off. Lowest power mode with ADC and pin interrupts functional. Peripheral clocks are stopped, but LPTimer, RTC, CMP, DAC can be used. NVIC is disabled (FCLK = OFF); AWIC is used to wake up from interrupt. On-chip voltage regulator is in a low power mode that supplies only enough power to run the chip at a reduced frequency. All SRAM is operating (content retained and I/O states held).	Sleep Deep	Interrupt
LLS (Low Leakage Stop)	State retention power mode. Most peripherals are in state retention mode (with clocks stopped), but LLWU, LPTimer, RTC, CMP, DAC can be used. NVIC is disabled; LLWU is used to wake up. **NOTE:** The LLWU interrupt must not be masked by the interrupt controller to avoid a scenario where the system does not fully exit stop mode on an LLS recovery. All SRAM is operating (content retained and I/O states held).	Sleep Deep	Wakeup Interrupt[1]
VLLS3 (Very Low Leakage Stop3)	Most peripherals are disabled (with clocks stopped), but LLWU, LPTimer, RTC, CMP, DAC can be used. NVIC is disabled; LLWU is used to wake up. SRAM_U and SRAM_L remain powered on (content retained and I/O states held).	Sleep Deep	Wakeup Reset[2]
VLLS2 (Very Low Leakage Stop2)	Most peripherals are disabled (with clocks stopped), but LLWU, LPTimer, RTC, CMP, DAC can be used. NVIC is disabled; LLWU is used to wake up. SRAM_L is powered off. A portion of SRAM_U remains powered on (content retained and I/O states held).	Sleep Deep	Wakeup Reset[2]
VLLS1 (Very Low Leakage Stop1)	Most peripherals are disabled (with clocks stopped), but LLWU, LPTimer, RTC, CMP, DAC can be used. NVIC is disabled; LLWU is used to wake up. All of SRAM_U and SRAM_L are powered off. The 32-byte system register file and the 32-byte VBAT register file remain powered for customer-critical data.	Sleep Deep	Wakeup Reset[2]

Table continues on the next page...

Chip mode	Description	Core mode	Normal recovery method
VLLS0 (Very Low Leakage Stop 0)	Most peripherals are disabled (with clocks stopped), but LLWU and RTC can be used. NVIC is disabled; LLWU is used to wake up. All of SRAM_U and SRAM_L are powered off. The 32-byte system register file and the 32-byte VBAT register file remain powered for customer-critical data. The POR detect circuit can be optionally powered off.	Sleep Deep	Wakeup Reset[2]
BAT (backup battery only)	The chip is powered down except for the VBAT supply. The RTC and the 32-byte VBAT register file for customer-critical data remain powered.	Off	Power-up Sequence

1. Resumes normal run mode operation by executing the LLWU interrupt service routine.
2. Follows the reset flow with the LLWU interrupt flag set for the NVIC.

Table 7. Power Modes

MCU Mode	Radio Mode	MCU typical current consumption	Radio typical current consumption
Stop	Idle	320 µA	700 µA, typ. (no CLOCKOUT)
Stop	Doze	320 µA	600 µA, typ. (no CLOCKOUT)
VLLS1	Low power / Hibernate	0.6 µA	<1 µA[1]
VLLS0	Reset / Powerdown	<250 nA	<30 nA
Run[2]	Transmit	12 mA	15 mA
Run[3]	Receive	12 mA	15 mA

1 Value does not include SPI activity.
2 32 MHz operation
3 32 MHz operation

Table 7 describes alignment of radio and MCU power modes versus current consumption for typical conditions: VBAT / VDD = + 2.7V @ T=25°C

7 MKW22D512V electrical characteristics

7.1 Recommended operating conditions

Table 8. Recommended operating conditions

Characteristic	Symbol	Min	Typ	Max	Unit
Power Supply Voltage (V_{BATT} = VDD_{INT})	V_{BATT}, VDD_{INT}	1.8	2.7	3.6	Vdc
Input Frequency	fin	2.360	—	2.480	GHz
Ambient Temperature Range	TA	–40	25	105	°C
Logic Input Voltage Low	VIL	0	—	30% VDDINT	V
Logic Input Voltage High	VIH	70% VDDINT	—	VDDINT	V
SPI Clock Rate	f_{SPI}	—	—	16.0	MHz
RF Input Power	Pmax	—	—	10	dBm
Crystal Reference Oscillator Frequency (±40 ppm over operating conditions to meet the 802.15.4 Standard.)	fref	32 MHz only			

7.2 Thermal handling ratings

Symbol	Description	Min.	Max.	Unit	Nots
T_{STG}	Storage temperature	–55	150	°C	1
T_{SDR}	Solder temperature, lead-free	—	260	°C	2

1 Determined according to JEDEC Standard JESD22-A103, *High Temperature Storage Life*.

2 Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices.*

7.3 Moisture handling ratings

Symbol	Description	Min.	Max.	Unit	Nots
MSL	Moisture sensitivitiy level	—	3	—	1

1 Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic* Solid *State Surface Mount Devices.*

7.4 ESD handling ratings

Symbol	Description	Min.	Max.	Unit	Nots
V_{HBM}	Electrostatic discharge voltage, human body model	–2000	2000	V	1
V_{CDM}	Electrostatic discharge voltage, charged-device model	–500	500	V	2
I_{LAT}	Latch-up current at ambient temperature of 105°C	–100	100	mA	

1 Determined according to JEDEC Standard JESD22-A103, *High Temperature Storage Life*.

2 Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices.*

7.5 Voltage and current ratings

Symbol	Description	Min.	Max.	Unit
V_{DD}	Digital supply voltage	–0.3	3.8	V
I_{DD}	Digital supply current	—	155	mA
V_{DIO}	Digital input voltage (except $\overline{RESET}$, EXTAL, and XTAL)	–0.3		V
V_{AIO}	Analog[1], $\overline{RESET}$, EXTAL, and XTAL input voltage	–0.3	V_{DD} + 0.3	V
I_D	Maximum current single pin limit (applies to all port pins)	–25	25	mA
V_{DDA}	Analog supply voltage	V_{DD} – 0.3	V_{DD} + 0.3	V
V_{USB_DP}	USB_DP input voltage	–0.3	3.63	V
V_{USB_DM}	USB_DM input voltage	–0.3	3.63	V
VREGIN	USB regulator input	–0.3	6	V
V_{BAT}	RTC battery supply voltage	–0.3	3.8	V

1 Analog pins are defined as pins that do not have an associated general purpose I/O port function.

7.5.1 EMC radiated emissions operating behaviors

Symbol	Description	Frequency band (MHz)	Typ.	Unit	Notes
V_{RE1}	Radiated emissions voltage, band 1	0.15–50	TBD	dBμV	1 , 2
V_{RE2}	Radiated emissions voltage, band 2	50–150	TBD	dBμV	
V_{RE3}	Radiated emissions voltage, band 3	150–500	TBD	dBμV	
V_{RE4}	Radiated emissions voltage, band 4	500–1000	TBD	dBμV	
V_{RE_IEC}	IEC level	0.15–1000	TBD	—	2, 3

1. Determined according to IEC Standard 61967-1, *Integrated Circuits - Measurement of Electromagnetic Emissions, 150 kHz to 1 GHz Part 1: General Conditions and Definitions* and IEC Standard 61967-2, *Integrated Circuits - Measurement of Electromagnetic Emissions, 150 kHz to 1 GHz Part 2: Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method*. Measurements were made while the microcontroller was running basic application code. The reported emission level is the value of the maximum measured emission, rounded up to the next whole number, from among the measured orientations in each frequency range.
2. V_{DD} = 3.3 V, T_A = 25 °C, f_{OSC} = 12 MHz (crystal), f_{SYS} = 48 MHz, f_{BUS} = 48MHz
3. Specified according to Annex D of IEC Standard 61967-2, *Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method*

7.5.2 Designing with radiated emissions in mind

To find application notes that provide guidance on designing your system to minimize interference from radiated emissions:

1. Go to http://www.freescale.com.
2. Perform a keyword search for "EMC design."

7.5.3 Capacitance attributes

Symbol	Description	Min.	Max.	Unit
C_{IN_A}	Input capacitance: analog pins	—	7	pF
C_{IN_D}	Input capacitance: digital pins	—	7	pF

8 MCU Electrical characteristics

8.1 Maximum ratings

Table 9. Maximum ratings

Requirement	Description	Symbol	Rating level	Unit
Power Supply Voltage		VBAT, VBAT2	–0.3 to 3.6	Vdc
Digital Input Voltage		Vin	–0.3 to (VDDINT + 0.3)	Vdc
RF Input Power		Pmax	+10	dBm
ESD[1]	Human Body Model	HBM	±2000	Vdc
	Machine Model	MM	±200	Vdc
	Charged Device Model	CDM	±750	Vdc
EMC[2]	Power Electro-Static Discharge / Direct Contact	PESD	No damage / latch up to ±4000	Vdc
			No soft failure / reset to ±1000	
	Power Electro-Static Discharge / Indirect Contact		No damage / latch up to ±6000	Vdc
			No soft failure / reset to ±1000	
	Langer IC / EFT / P201	EFT (Electro Magnetic Fast Transient)	No damage / latch up to ±5	Vdc
			No soft failure / reset to ±5	
	Langer IC / EFT / P201		No damage / latch up to ±300	Vdc
			No soft failure / reset to ±150	
Junction Temperature		T_J	+150	°C
Storage Temperature Range		T_{stg}	–65 to +165	°C

NOTE

Maximum ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the electrical characteristics or recommended operating conditions tables.

[1] Electrostatic discharge on all device pads meet this requirement
[2] Electromagnetic compatibility for this product is low stress rating level

8.2 General

8.2.1 AC electrical characteristics

Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured at the 20% and 80% points, as shown in the following figure.

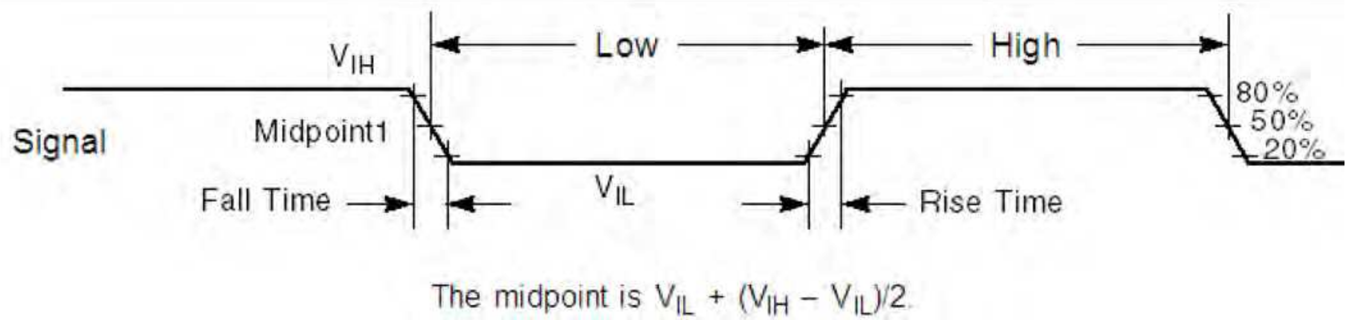


Figure 2. Input signal measurement reference

All digital I/O switching characteristics assume:

- output pins
  - — have C_L=30pF loads,
  - — are configured for fast slew rate (PORTx_PCRn[SRE]=0), and
  - — are configured for high drive strength (PORTx_PCRn[DSE]=1)
- input pins
  - — have their passive filter disabled (PORTx_PCRn[PFE]=0)

8.2.2 Nonswitching electrical specifications

8.2.2.1 Voltage and current operating requirements

1

Symbol	Description	Min.	Max.	Unit	Notes
V_{DD}	Supply voltage	1.71	3.6	V	
V_{DDA}	Analog supply voltage	1.71	3.6	V	
$V_{DD} - V_{DDA}$	V_{DD}-to-V_{DDA} differential voltage	–0.1	0.1	V	
$V_{SS} - V_{SSA}$	V_{SS}-to-V_{SSA} differential voltage	–0.1	0.1	V	
V_{BAT}	RTC battery supply voltage	1.71	3.6	V	
V_{IH}	Input high voltage • $2.7 V \leq V_{DD} \leq 3.6 V$ • $1.7 V \leq V_{DD} \leq 2.7 V$	 $0.7 \times V_{DD}$ $0.75 \times V_{DD}$	 — —	 V V	
V_{IL}	Input low voltage • $2.7 V \leq V_{DD} \leq 3.6 V$ • $1.7 V \leq V_{DD} \leq 2.7 V$	 — —	 $0.35 \times V_{DD}$ $0.3 \times V_{DD}$	 V V	
V_{HYS}	Input hysteresis	$0.06 \times V_{DD}$	—	V	
I_{ICIO}	I/O pin DC injection current — single pin • $V_{IN} < V_{SS}$-0.3V (Negative current injection) • $V_{IN} > V_{DD}$+0.3V (Positive current injection)	 -3 —	 — +3	mA	1
I_{ICcont}	Contiguous pin DC injection current —regional limit, includes sum of negative injection currents or sum of positive injection currents of 16 contiguous pins • Negative current injection • Positive current injection	 -25 —	 — +25	mA	
V_{RAM}	V_{DD} voltage required to retain RAM	1.2	—	V	
V_{RFVBAT}	V_{BAT} voltage required to retain the VBAT register file	V_{POR_VBAT}	—	V	

1. All analog pins are internally clamped to V_{SS} and V_{DD} through ESD protection diodes. If V_{IN} is greater than V_{AIO_MIN} (=V_{SS}-0.3V) and V_{IN} is less than V_{AIO_MAX}(=V_{DD}+0.3V) is observed, then there is no need to provide current limiting resistors at the pads. If these limits cannot be observed then a current limiting resistor is required. The negative DC injection current limiting resistor is calculated as $R=(V_{AIO\_MIN}-V_{IN})/|I_{IC}|$. The positive injection current limiting resistor is calcualted as $R=(V_{IN}-V_{AIO\_MAX})/|I_{IC}|$. Select the larger of these two calculated resistances.

8.3 LVD and POR operating requirements

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{POR}	Falling VDD POR detect voltage	0.8	1.1	1.5	V	
V_{LVDH}	Falling low-voltage detect threshold — high range (LVDV=01)	2.48	2.56	2.64	V	
	Low-voltage warning thresholds — high range					1
V_{LVW1H}	• Level 1 falling (LVWV=00)	2.62	2.70	2.78	V	
V_{LVW2H}	• Level 2 falling (LVWV=01)	2.72	2.80	2.88	V	
V_{LVW3H}	• Level 3 falling (LVWV=10)	2.82	2.90	2.98	V	
V_{LVW4H}	• Level 4 falling (LVWV=11)	2.92	3.00	3.08	V	
V_{HYSH}	Low-voltage inhibit reset/recover hysteresis — high range	—	±80	—	mV	
V_{LVDL}	Falling low-voltage detect threshold — low range (LVDV=00)	1.54	1.60	1.66	V	
	Low-voltage warning thresholds — low range					1
V_{LVW1L}	• Level 1 falling (LVWV=00)	1.74	1.80	1.86	V	
V_{LVW2L}	• Level 2 falling (LVWV=01)	1.84	1.90	1.96	V	
V_{LVW3L}	• Level 3 falling (LVWV=10)	1.94	2.00	2.06	V	
V_{LVW4L}	• Level 4 falling (LVWV=11)	2.04	2.10	2.16	V	
V_{HYSL}	Low-voltage inhibit reset/recover hysteresis — low range	—	±60	—	mV	
V_{BG}	Bandgap voltage reference	0.97	1.00	1.03	V	
t_{LPO}	Internal low power oscillator period — factory trimmed	900	1000	1100	μs	

1. Rising thresholds are falling threshold + hysteresis voltage.

VBAT power operating requirements

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{POR_VBAT}	Falling VBAT supply POR detect voltage	0.8	1.1	1.5	V	

8.3.1V

Symbol	Description	Min.	Max.	Unit	Notes
V_{OH}	Output high voltage — high drive strength				
	• 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OH} = - 9 mA	V_{DD} – 0.5	—	V	
	• 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OH} = -3 mA	V_{DD} – 0.5	—	V	
	Output high voltage — low drive strength				
	• 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OH} = -2 mA	V_{DD} – 0.5	—	V	
	• 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OH} = -0.6 mA	V_{DD} – 0.5	—	V	
I_{OHT}	Output high current total for all ports	—	100	mA	
V_{OL}	Output low voltage — high drive strength				
	• 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OL} = 9 mA	—	0.5	V	
	• 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OL} = 3 mA	—	0.5	V	
	Output low voltage — low drive strength				
	• 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OL} = 2 mA	—	0.5	V	
	• 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OL} = 0.6 mA	—	0.5	V	
I_{OLT}	Output low current total for all ports	—	100	mA	
I_{IN}	Input leakage current (per pin)				1
	• @ full temperature range	—	1.0	μA	
	• @ 25 °C	—	0.1	μA	
I_{OZ}	Hi-Z (off-state) leakage current (per pin)	—	1	μA	
I_{OZ}	Total Hi-Z (off-state) leakage current (all input pins)	—	4	μA	
R_{PU}	Internal pullup resistors	22	50	kΩ	2
R_{PD}	Internal pulldown resistors	22	50	kΩ	3

1. Tested by ganged leakage method
2. Measured at Vinput = V_{SS}
3. Measured at Vinput = V_{DD}

8.3.2 Power mode transition operating behaviors

All specifications except t_{POR}, and VLLSx to RUN recovery times in the following table assume this clock configuration:

- CPU and system clocks = 50 MHz
- Bus clock = 50 MHz
- Flash clock = 25 MHz

Symbol	Description	Min.	Max.	Unit	Notes
t_{POR}	After a POR event, amount of time from the point V_{DD} reaches 1.71 V to execution of the first instruction across the operating temperature range of the chip.	—	300	μs	
	• VLLS0 → RUN	—	130	μs	
	• VLLS1 → RUN	—	130	μs	
	• VLLS2 → RUN	—	70	μs	
	• VLLS3 → RUN	—	70	μs	
	• LLS → RUN	—	6	μs	
	• VLPS → RUN	—	5.2	μs	
	• STOP → RUN	—	5.2	μs	

8.3.3 PPower consumption operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{DDA}	Analog supply current	—	—	See note	mA	1
I_{DD_RUN}	Run mode current — all peripheral clocks disabled, code executing from flash					2
	• @ 1.8V	—	TBD	TBD	mA	
	• @ 3.0V	—	17	TBD	mA	
I_{DD_RUN}	Run mode current — all peripheral clocks enabled, code executing from flash					3, 4
	• @ 1.8V	—	TBD	TBD	mA	
	• @ 3.0V					
	• @ 25°C	—	24	TBD	mA	
	• @ 125°C	—	TBD	TBD	mA	
I_{DD_WAIT}	Wait mode high frequency current at 3.0 V — all peripheral clocks disabled	—	12.3	TBD	mA	2
I_{DD_WAIT}	Wait mode reduced frequency current at 3.0 V — all peripheral clocks disabled	—	TBD	TBD	mA	5
I_{DD_STOP}	Stop mode current at 3.0 V	—	200	TBD	µA	
I_{DD_VLPR}	Very-low-power run mode current at 3.0 V — all peripheral clocks disabled	—	1	TBD	mA	6

Table continues on the next page...

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{DD_VLPR}	Very-low-power run mode current at 3.0 V — all peripheral clocks enabled	—	TBD	TBD	mA	7
I_{DD_VLPW}	Very-low-power wait mode current at 3.0 V	—	700	TBD	µA	8
I_{DD_VLPS}	Very-low-power stop mode current at 3.0 V	—	6.3	TBD	µA	
I_{DD_LLS}	Low leakage stop mode current at 3.0 V • @ –40 to 25°C • @ 50°C • @ 70°C • @ 105°C	—	3.2	TBD	µA	
I_{DD_VLLS3}	Very low-leakage stop mode 3 current at 3.0 V • @ –40 to 25°C • @ 50°C • @ 70°C • @ 105°C	—	2.6	TBD	µA	
I_{DD_VLLS2}	Very low-leakage stop mode 2 current at 3.0 V • @ –40 to 25°C • @ 50°C • @ 70°C • @ 105°C	—	0.8	TBD	nA	
I_{DD_VLLS1}	Very low-leakage stop mode 1 current at 3.0 V • @ –40 to 25°C • @ 50°C • @ 70°C • @ 105°C	—	0.6	TBD	nA	
I_{DD_VLLS0}	Very low-leakage stop mode 0 current at 3.0 V with POR detect circuit enabled • @ –40 to 25°C • @ 50°C • @ 70°C • @ 105°C	—	0.4	TBD	nA	
I_{DD_VLLS0}	Very low-leakage stop mode 0 current at 3.0 V with POR detect circuit disabled • @ –40 to 25°C • @ 50°C • @ 70°C • @ 105°C	—	0.2	TBD	nA	
I_{DD_VBAT}	Average current when CPU is not accessing RTC registers at 3.0 V • @ –40 to 25°C • @ 50°C • @ 70°C • @ 105°C	—	0.8	TBD	nA	9

1. The analog supply current is the sum of the active or disabled current for each of the analog modules on the device. See each module's specification for its supply current.
2. 50MHz core and system clock, 25MHz bus clock, and 25MHz flash clock . MCG configured for FEI mode. All peripheral clocks disabled.
3. 50MHz core and system clock, 25MHz bus clock, and 25MHz flash clock. MCG configured for FEI mode. All peripheral clocks enabled, and peripherals are in active operation.
4. Max values are measured with CPU executing DSP instructions
5. 25MHz core and system clock, 25MHz bus clock, and 12.5MHz flash clock. MCG configured for FEI mode.

6. 2 MHz core, system, and bus clock and 1MHz flash clock. MCG configured for BLPE mode. All peripheral clocks disabled. Code executing from flash.
7. 2 MHz core, system, and bus clock and 1MHz flash clock. MCG configured for BLPE mode. All peripheral clocks enabled but peripherals are not in active operation. Code executing from flash.
8. 2 MHz core, system, and bus clock and 1MHz flash clock. MCG configured for BLPE mode. All peripheral clocks disabled.
9. Includes 32kHz oscillator current and RTC operation.

8.4 Switching specification

8.4.1 Device clock specifications

Symbol	Description	Min.	Max.	Unit	Notes
Normal run mode					
f_{SYS}	System and core clock	—	50	MHz	
	System and core clock when Full Speed USB in operation	20	—	MHz	
f_{BUS}	Bus clock	—	50	MHz	
f_{FLASH}	Flash clock	—	25	MHz	
f_{LPTMR}	LPTMR clock	—	25	MHz	
VLPR mode[1]					
f_{SYS}	System and core clock	—	4	MHz	
f_{BUS}	Bus clock	—	4	MHz	
f_{FLASH}	Flash clock	—	1	MHz	
f_{ERCLK}	External reference clock	—	16	MHz	
f_{LPTMR_pin}	LPTMR clock	—	25	MHz	
f_{LPTMR_ERCLK}	LPTMR external reference clock	—	16	MHz	
f_{I2S_MCLK}	I2S master clock	—	12.5	MHz	
f_{I2S_BCLK}	I2S bit clock	—	4	MHz	

1. The frequency limitations in VLPR mode here override any frequency specification listed in the timing specification for any other module.

8.4.2 General switching specifications

These general purpose specifications apply to all signals configured for GPIO, UART, CMT, and I^2C signals.

Symbol	Description	Min.	Max.	Unit	Notes
	GPIO pin interrupt pulse width (digital glitch filter disabled) — Synchronous path	1.5	—	Bus clock cycles	1, 2
	GPIO pin interrupt pulse width (digital glitch filter disabled, analog filter enabled) — Asynchronous path	100	—	ns	3
	GPIO pin interrupt pulse width (digital glitch filter disabled, analog filter disabled) — Asynchronous path	50	—	ns	3
	External reset pulse width (digital glitch filter disabled)	100	—	ns	3
	Mode select (EZP_CS) hold time after reset deassertion	2	—	Bus clock cycles	
	Port rise and fall time (high drive strength)				4
	• Slew disabled				
	• $1.71 \leq V_{DD} \leq 2.7V$	—	13	ns	
	• $2.7 \leq V_{DD} \leq 3.6V$	—		ns	
	• Slew enabled		7		
	• $1.71 \leq V_{DD} \leq 2.7V$	—		ns	
	• $2.7 \leq V_{DD} \leq 3.6V$	—	36	ns	
			24		
	Port rise and fall time (low drive strength)				5
	• Slew disabled				
	• $1.71 \leq V_{DD} \leq 2.7V$	—	12	ns	
	• $2.7 \leq V_{DD} \leq 3.6V$	—	6	ns	
	• Slew enabled				
	• $1.71 \leq V_{DD} \leq 2.7V$	—	36	ns	
	• $2.7 \leq V_{DD} \leq 3.6V$	—	24	ns	

1. This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In Stop, VLPS, LLS, and VLLSx modes, the synchronizer is bypassed so shorter pulses can be recognized in that case.
2. The greater synchronous and asynchronous timing must be met.
3. This is the minimum pulse width that is guaranteed to be recognized as a pin interrupt request in Stop, VLPS, LLS, and VLLSx modes.
4. 75pF load
5. 15pF load

8.5 Core modules

8.5.1 JTAG electricals

Symbol	Description	Min.	Max.	Unit
	Operating voltage	2.7	5.5	V
J1	TCLK frequency of operation • JTAG • CJTAG	 — —	 10 5	MHz
J2	TCLK cycle period	1/J1	—	ns
J3	TCLK clock pulse width • JTAG • CJTAG	 100 200	 — —	 ns ns ns
J4	TCLK rise and fall times	—	1	ns
J5	TMS input data setup time to TCLK rise • JTAG • CJTAG	53 112	— —	ns
J6	TDI input data setup time to TCLK rise	8	—	ns
J7	TMS input data hold time after TCLK rise • JTAG • CJTAG	3.4 3.4	— —	ns
J8	TDI input data hold time after TCLK rise	3.4	—	ns
J9	TCLK low to TMS data valid • JTAG • CJTAG	— —	48 85	ns
J10	TCLK low to TDO data valid	—	48	ns
J11	Output data hold/invalid time after clock edge[1]	—	3	ns

1. They are common for JTAG and CJTAG. Input transition = 1 ns and Output load = 50pf

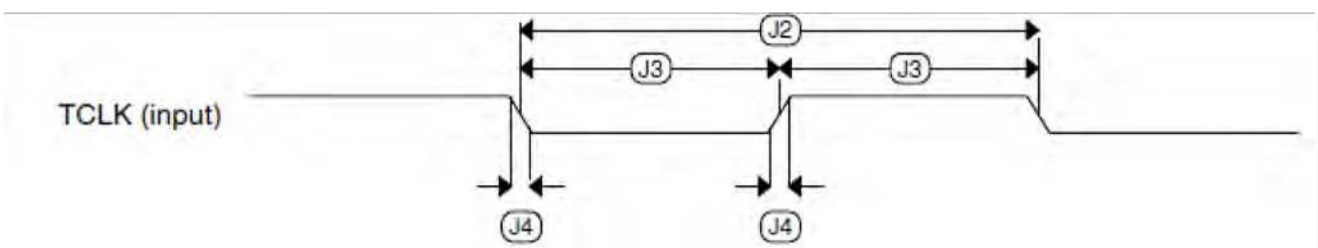


Figure 3. Test clock input timing

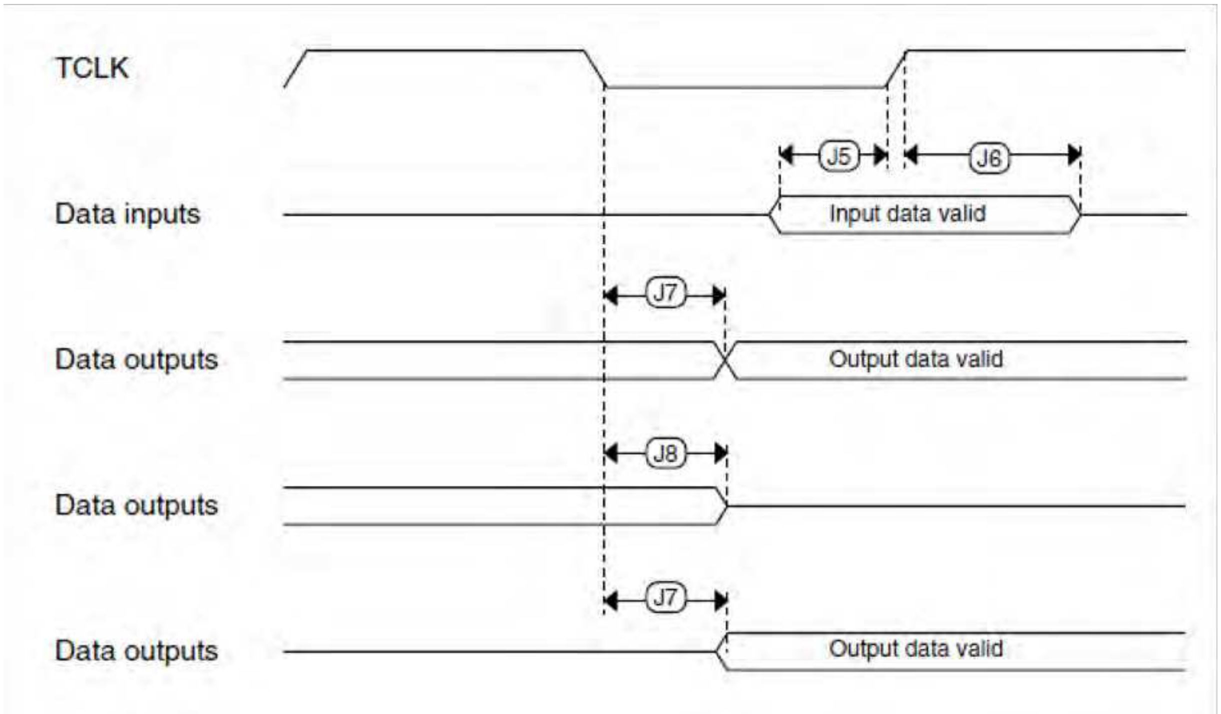


Figure 4. Boundary scan (JTAG) timing

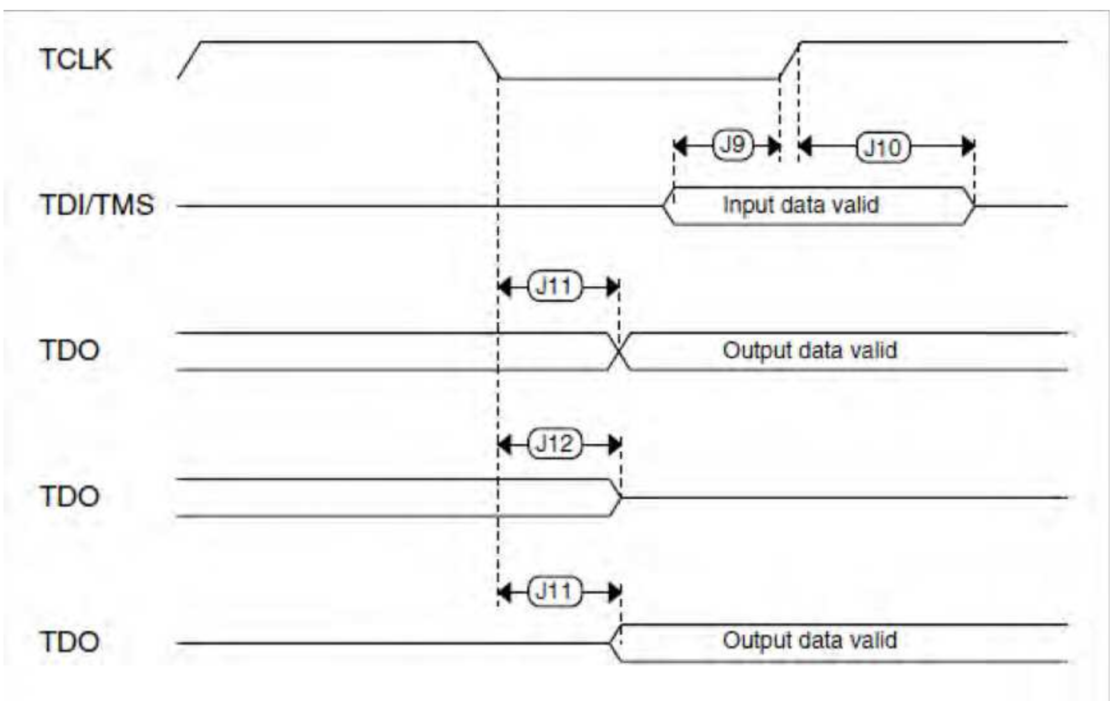


Figure 5. Test access port timing

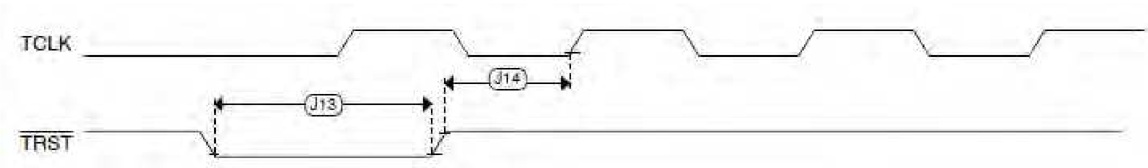


Figure 6. TRST timing

8.6 Clock modules

Symbol	Description		Min.	Typ.	Max.	Unit	Notes
f_{ints_ft}	Internal reference frequency (slow clock) — factory trimmed at nominal VDD and 25 °C		—	32.768	—	kHz	
f_{ints_t}	Internal reference frequency (slow clock) — user trimmed		31.25	—	39.0625	kHz	
$\Delta_{fdco\_res\_t}$	Resolution of trimmed average DCO output frequency at fixed voltage and temperature — using SCTRIM and SCFTRIM		—	± 0.3	± 0.6	$\%f_{dco}$	1
$\Delta f_{dco\_res\_t}$	Resolution of trimmed average DCO output frequency at fixed voltage and temperature — using SCTRIM only		—	± 0.2	± 0.5	$\%f_{dco}$	1
Δf_{dco_t}	Total deviation of trimmed average DCO output frequency over voltage and temperature		—	+0.5/-0.7	± 3	$\%f_{dco}$	1
Δf_{dco_t}	Total deviation of trimmed average DCO output frequency over fixed voltage and temperature range of 0–70°C		—	± 0.3	TBD	$\%f_{dco}$	1
f_{intf_ft}	Internal reference frequency (fast clock) — factory trimmed at nominal VDD and 25°C		—	4	—	MHz	
f_{intf_t}	Internal reference frequency (fast clock) — user trimmed at nominal VDD and 25 °C		3	—	5	MHz	
f_{loc_low}	Loss of external clock minimum frequency — RANGE = 00		(3/5) x f_{ints_t}	—	—	kHz	
f_{loc_high}	Loss of external clock minimum frequency — RANGE = 01, 10, or 11		(16/5) x f_{ints_t}	—	—	kHz	
		FLL					
f_{fll_ref}	FLL reference frequency range		31.25	—	39.0625	kHz	
f_{dco}	DCO output frequency range	Low range (DRS=00) $640 \times f_{fll\_ref}$	20	20.97	25	MHz	2, 3
		Mid range (DRS=01) $1280 \times f_{fll\_ref}$	40	41.94	50	MHz	
		Mid-high range (DRS=10) $1920 \times f_{fll\_ref}$	60	62.91	75	MHz	
		High range (DRS=11) $2560 \times f_{fll\_ref}$	80	83.89	100	MHz	
$f_{dco\_t\_DMX32}$	DCO output frequency	Low range (DRS=00) $732 \times f_{fll\_ref}$	—	23.99	—	MHz	4, 5
		Mid range (DRS=01) $1464 \times f_{fll\_ref}$	—	47.97	—	MHz	
		Mid-high range (DRS=10) $2197 \times f_{fll\_ref}$	—	71.99	—	MHz	
		High range (DRS=11) $2929 \times f_{fll\_ref}$	—	95.98	—	MHz	

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
J_{cyc_fll}	FLL period jitter • f_{VCO} = 48 MHz • f_{VCO} = 98 MHz	— —	180 150	— —	ps	
$t_{fll\_acquire}$	FLL target frequency acquisition time	—	—	1	ms	6
	PLL					
f_{vco}	VCO operating frequency	48.0	—	100	MHz	
I_{pll}	PLL operating current • PLL @ 96 MHz ($f_{osc\_hi\_1}$ = 8 MHz, f_{pll_ref} = 2 MHz, VDIV multiplier = 48)	—	1060	—	µA	7
I_{pll}	PLL operating current • PLL @ 48 MHz ($f_{osc\_hi\_1}$ = 8 MHz, f_{pll_ref} = 2 MHz, VDIV multiplier = 24)	—	600	—	µA	7
f_{pll_ref}	PLL reference frequency range	2.0	—	4.0	MHz	
J_{cyc_pll}	PLL period jitter (RMS) • f_{vco} = 48 MHz • f_{vco} = 100 MHz	— —	120 50	— —	ps ps	8
J_{acc_pll}	PLL accumulated jitter over 1µs (RMS) • f_{vco} = 48 MHz • f_{vco} = 100 MHz	— —	1350 600	— —	ps ps	8
D_{lock}	Lock entry frequency tolerance	± 1.49	—	± 2.98	%	
D_{unl}	Lock exit frequency tolerance	± 4.47	—	± 5.97	%	
t_{pll_lock}	Lock detector detection time	—	—	$150 \times 10^{-6} + 1075(1/f_{pll\_ref})$	s	9

1. This parameter is measured with the internal reference (slow clock) being used as a reference to the FLL (FEI clock mode).
2. These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32=0.
3. The resulting system clock frequencies should not exceed their maximum specified values. The DCO frequency deviation (Δf_{dco_t}) over voltage and temperature should be considered.
4. These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32=1.
5. The resulting clock frequency must not exceed the maximum specified clock frequency of the device.
6. This specification applies to any time the FLL reference source or reference divider is changed, trim value is changed, DMX32 bit is changed, DRS bits are changed, or changing from FLL disabled (BLPE, BLPI) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.
7. Excludes any oscillator currents that are also consuming power while PLL is in operation.
8. This specification was obtained using a Freescale developed PCB. PLL jitter is dependent on the noise characteristics of each PCB and results will vary.
9. This specification applies to any time the PLL VCO divider or reference divider is changed, or changing from PLL disabled (BLPE, BLPI) to PLL enabled (PBE, PEE). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

8.6.1 Oscillator electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{DD}	Supply voltage	1.71	—	3.6	V	
I_{DDOSC}	Supply current — low-power mode (HGO=0)					1
	• 32 kHz	—	500	—	nA	
	• 4 MHz	—	200	—	μA	
	• 8 MHz (RANGE=01)	—	300	—	μA	
	• 16 MHz	—	950	—	μA	
	• 24 MHz	—	1.2	—	mA	
	• 32 MHz	—	1.5	—	mA	
I_{DDOSC}	Supply current — high gain mode (HGO=1)					1
	• 32 kHz	—	25	—	μA	
	• 4 MHz	—	400	—	μA	
	• 8 MHz (RANGE=01)	—	500	—	μA	
	• 16 MHz	—	2.5	—	mA	
	• 24 MHz	—	3	—	mA	
	• 32 MHz	—	4	—	mA	
C_x	EXTAL load capacitance	—	—	—		2, 3
C_y	XTAL load capacitance	—	—	—		2, 3
R_F	Feedback resistor — low-frequency, low-power mode (HGO=0)	—	—	—	MΩ	2, 4
	Feedback resistor — low-frequency, high-gain mode (HGO=1)	—	10	—	MΩ	
	Feedback resistor — high-frequency, low-power mode (HGO=0)	—	—	—	MΩ	
	Feedback resistor — high-frequency, high-gain mode (HGO=1)	—	1	—	MΩ	
R_S	Series resistor — low-frequency, low-power mode (HGO=0)	—	—	—	kΩ	
	Series resistor — low-frequency, high-gain mode (HGO=1)	—	200	—	kΩ	
	Series resistor — high-frequency, low-power mode (HGO=0)	—	—	—	kΩ	
	Series resistor — high-frequency, high-gain mode (HGO=1)	—	0	—	kΩ	

Table continues on the next page...

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{pp}[5]	Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, low-power mode (HGO=0)	—	0.6	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, high-gain mode (HGO=1)	—	V_{DD}	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, low-power mode (HGO=0)	—	0.6	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, high-gain mode (HGO=1)	—	V_{DD}	—	V	

1. V_{DD}=3.3 V, Temperature =25 °C
2. See crystal or resonator manufacturer's recommendation
3. C_x,C_y can be provided by using either the integrated capacitors or by using external components.
4. When low power mode is selected, R_F is integrated and must not be attached externally.
5. The EXTAL and XTAL pins should only be connected to required oscillator components and must not be connected to any other devices.

8.6.1.1 Oscillator frequency specification

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
f_{osc_lo}	Oscillator crystal or resonator frequency — low frequency mode (MCG_C2[RANGE]=00)	32	—	40	kHz	
$f_{osc\_hi\_1}$	Oscillator crystal or resonator frequency — high frequency mode (low range) (MCG_C2[RANGE]=01)	3	—	8	MHz	
$f_{osc\_hi\_2}$	Oscillator crystal or resonator frequency — high frequency mode (high range) (MCG_C2[RANGE]=1x)	8	—	32	MHz	
f_{ec_extal}	Input clock frequency (external clock mode)	—	—	50	MHz	1, 2
t_{dc_extal}	Input clock duty cycle (external clock mode)	40	50	60	%	
t_{cst}	Crystal startup time — 32 kHz low-frequency, low-power mode (HGO=0)	—	750	—	ms	3, 4
	Crystal startup time — 32 kHz low-frequency, high-gain mode (HGO=1)	—	250	—	ms	
	Crystal startup time — 8 MHz high-frequency (MCG_C2[RANGE]=01), low-power mode (HGO=0)	—	0.6	—	ms	
	Crystal startup time — 8 MHz high-frequency (MCG_C2[RANGE]=01), high-gain mode (HGO=1)	—	1	—	ms	

1. Other frequency limits may apply when external clock is being used as a reference for the FLL or PLL.
2. When transitioning from FBE to FEI mode, restrict the frequency of the input clock so that, when it is divided by FRDIV, it remains within the limits of the DCO input clock frequency.

3. Proper PC board layout procedures must be followed to achieve specifications.
4. Crystal startup time is defined as the time between the oscillator being enabled and the OSCINIT bit in the MCG_S register being set.

8.6.2 32 kHz oscillator electrical characteristics

8.6.2.1 32 kHz oscillator DC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit
V_{BAT}	Supply voltage	1.71	—	3.6	V
R_F	Internal feedback resistor	—	100	—	MΩ
C_{para}	Parasitical capacitance of EXTAL32 and XTAL32	—	5	7	pF
V_{pp}[1]	Peak-to-peak amplitude of oscillation	—	0.6	—	V

1. When a crystal is being used with the 32 kHz oscillator, the EXTAL32 and XTAL32 pins should only be connected to required oscillator components and must not be connected to any other devices.

8.6.2.2 32 kHz oscillator frequency specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
f_{osc_lo}	Oscillator crystal	—	32.768	—	kHz	
t_{start}	Crystal start-up time	—	1000	—	ms	1
$f_{ec\_extal32}$	Externally provided input clock frequency	—	32.768	—	kHz	2
$v_{ec\_extal32}$	Externally provided input clock amplitude	700	—	V_{BAT}	mV	2, 3

1. Proper PC board layout procedures must be followed to achieve specifications.
2. This specification is for an externally supplied clock driven to EXTAL32 and does not apply to any other clock input. The oscillator remains enabled and XTAL32 must be left unconnected.
3. The parameter specified is a peak-to-peak value and V_{IH} and V_{IL} specifications do not apply. The voltage of the applied clock must be within the range of V_{SS} to V_{BAT}.

8.7 Memories and memory interfaces

8.7.1 Flash electrical specifications

8.7.1.1 Flash timing specifications — program and erase

The following specifications represent the amount of time the internal charge pumps are active and do not include command overhead.

NVM program/erase timing specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
t_{hvpgm4}	Longword Program high-voltage time	—	7.5	18	μs	
$t_{hversscr}$	Sector Erase high-voltage time	—	13	113	ms	1

1. Maximum time based on expectations at cycling end-of-life.

8.7.1.2 Flash timing specifications — commands

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	Read 1s Block execution time					
$t_{rd1blk256k}$	• 256 KB program/data flash	—	—	1.7	ms	
$t_{rd1sec2k}$	Read 1s Section execution time (flash sector)	—	—	60	μs	1
t_{pgmchk}	Program Check execution time	—	—	45	μs	1
t_{rdrsrc}	Read Resource execution time	—	—	30	μs	1
t_{pgm4}	Program Longword execution time	—	65	145	μs	
	Erase Flash Block execution time					2
$t_{ersblk256k}$	• 256 KB program/data flash	—	122	985	ms	
t_{ersscr}	Erase Flash Sector execution time	—	14	114	ms	2
	Program Section execution time					
$t_{pgmsec512}$	• 512 B flash	—	2.4	—	ms	
$t_{pgmsec1k}$	• 1 KB flash	—	4.7	—	ms	
$t_{pgmsec2k}$	• 2 KB flash	—	9.3	—	ms	
t_{rd1all}	Read 1s All Blocks execution time	—	—	1.8	ms	
t_{rdonce}	Read Once execution time	—	—	25	μs	1
$t_{pgmonce}$	Program Once execution time	—	65	—	μs	
t_{ersall}	Erase All Blocks execution time	—	250	2000	ms	2
t_{vfykey}	Verify Backdoor Access Key execution time	—	—	30	μs	1
	Swap Control execution time					
$t_{swapx01}$	• control code 0x01	—	200	—	μs	
$t_{swapx02}$	• control code 0x02	—	70	150	μs	
$t_{swapx04}$	• control code 0x04	—	70	150	μs	
$t_{swapx08}$	• control code 0x08	—	—	30	μs	

Table continues on the next page...

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	Program Partition for EEPROM execution time					
$t_{pgmpart64k}$	• 256 KB FlexNVM	—	145	—	ms	
$t_{pgmpart256k}$						
	Set FlexRAM Function execution time:					
$t_{setramff}$	• Control Code 0xFF	—	70	—	μs	
$t_{setram32k}$	• 32 KB EEPROM backup	—	0.8	1.2	ms	
$t_{setram64k}$	• 64 KB EEPROM backup	—	1.3	1.9	ms	
$t_{setram256k}$	• 256 KB EEPROM backup	—	4.5	5.5	ms	
Byte-write to FlexRAM for EEPROM operation						
$t_{eewr8bers}$	Byte-write to erased FlexRAM location execution time	—	175	260	μs	3
	Byte-write to FlexRAM execution time:					
$t_{eewr8b32k}$	• 32 KB EEPROM backup	—	385	1800	μs	
$t_{eewr8b64k}$	• 64 KB EEPROM backup	—	475	2000	μs	
$t_{eewr8b128k}$	• 128 KB EEPROM backup	—	650	2400	μs	
$t_{eewr8b256k}$	• 256 KB EEPROM backup	—	1000	3200	μs	
Word-write to FlexRAM for EEPROM operation						
$t_{eewr16bers}$	Word-write to erased FlexRAM location execution time	—	175	260	μs	
	Word-write to FlexRAM execution time:					
$t_{eewr16b32k}$	• 32 KB EEPROM backup	—	385	1800	μs	
$t_{eewr16b64k}$	• 64 KB EEPROM backup	—	475	2000	μs	
$t_{eewr16b128k}$	• 128 KB EEPROM backup	—	650	2400	μs	
$t_{eewr16b256k}$	• 256 KB EEPROM backup	—	1000	3200	μs	
Longword-write to FlexRAM for EEPROM operation						
$t_{eewr32bers}$	Longword-write to erased FlexRAM location execution time	—	360	540	μs	
	Longword-write to FlexRAM execution time:					
$t_{eewr32b32k}$	• 32 KB EEPROM backup	—	630	2050	μs	
$t_{eewr32b64k}$	• 64 KB EEPROM backup	—	810	2250	μs	
$t_{eewr32b128k}$	• 128 KB EEPROM backup	—	1200	2675	μs	
$t_{eewr32b256k}$	• 256 KB EEPROM backup	—	1900	3500	μs	

1. Assumes 25MHz flash clock frequency.
2. Maximum times for erase parameters based on expectations at cycling end-of-life.
3. For byte-writes to an erased FlexRAM location, the aligned word containing the byte must be erased.

Flash high voltage current behaviors

Symbol	Description	Min.	Typ.	Max.	Unit
I_{DD_PGM}	Average current adder during high voltage flash programming operation	—	2.5	6.0	mA
I_{DD_ERS}	Average current adder during high voltage flash erase operation	—	1.5	4.0	mA

8.7.1.4 NVM reliability specifications

Symbol	Description	Min.	Typ.[1]	Max.	Unit	Notes
	Program Flash					
$t_{nvmretp10k}$	Data retention after up to 10 K cycles	5	50	—	years	
$t_{nvmretp1k}$	Data retention after up to 1 K cycles	20	100	—	years	
$n_{nvmcycp}$	Cycling endurance	10 K	50 K	—	cycles	2
	Data Flash					
$t_{nvmretd10k}$	Data retention after up to 10 K cycles	5	50	—	years	
$t_{nvmretd1k}$	Data retention after up to 1 K cycles	20	100	—	years	
$n_{nvmcycd}$	Cycling endurance	10 K	50 K	—	cycles	2
	FlexRAM as EEPROM					
$t_{nvmretee100}$	Data retention up to 100% of write endurance	5	50	—	years	
$t_{nvmretee10}$	Data retention up to 10% of write endurance	20	100	—	years	
	Write endurance					3
$n_{nvmwree16}$	• EEPROM backup to FlexRAM ratio = 16	35 K	175 K	—	writes	
$n_{nvmwree128}$	• EEPROM backup to FlexRAM ratio = 128	315 K	1.6 M	—	writes	
$n_{nvmwree512}$	• EEPROM backup to FlexRAM ratio = 512	1.27 M	6.4 M	—	writes	
$n_{nvmwree4k}$	• EEPROM backup to FlexRAM ratio = 4096	10 M	50 M	—	writes	
$n_{nvmwree32k}$	• EEPROM backup to FlexRAM ratio = 32,768	80 M	400 M	—	writes	

1. Typical data retention values are based on measured response accelerated at high temperature and derated to a constant 25°C use profile. Engineering Bulletin EB618 does not apply to this technology. Typical endurance defined in Engineering Bulletin EB619.
2. Cycling endurance represents number of program/erase cycles at -40°C ≤ T_j ≤ 125°C.
3. Write endurance represents the number of writes to each FlexRAM location at -40°C ≤Tj ≤ 125°C influenced by the cycling endurance of the FlexNVM (same value as data flash) and the allocated EEPROM backup per subsystem. Minimum and typical values assume all byte-writes to FlexRAM.

8.7.1.5 Write endurance to FlexRAM for EEPROM

When the FlexNVM partition code is not set to full data flash, the EEPROM data set size can be set to any of several non-zero values.

The bytes not assigned to data flash via the FlexNVM partition code are used by the flash memory module to obtain an effective endurance increase for the EEPROM data. The built-in EEPROM record management system raises the number of program/erase cycles that can be attained prior to device wear-out by cycling the EEPROM data through a larger EEPROM NVM storage space.

While different partitions of the FlexNVM are available, the intention is that a single choice for the FlexNVM partition code and EEPROM data set size is used throughout the entire lifetime of a given application. The EEPROM endurance equation and graph shown below assume that only one configuration is ever used.

$$\text{Writes\_subsystem} = \frac{\text{EEPROM . 2 Å\~{} EEESPLIT Å\~{} EEESIZE}}{\text{EEESPLIT Å\~{} EEESIZE}} \times \text{Write\_efficiency} \times n_{nvmcycd}$$

where

- Writes_subsystem — minimum number of writes to each FlexRAM location for subsystem (each subsystem can have different endurance)
- EEPROM — allocated FlexNVM for each EEPROM subsystem based on DEPART; entered with the Program Partition command
- EEESPLIT — FlexRAM split factor for subsystem; entered with the Program Partition command
- EEESIZE — allocated FlexRAM based on DEPART; entered with the Program Partition command
- Write_efficiency
  - — 0.25 for 8-bit writes to FlexRAM
  - — 0.50 for 16-bit or 32-bit writes to FlexRAM
- $n_{nvmcycd}$ — data flash cycling endurance (the following graph assumes 10,000 cycles)

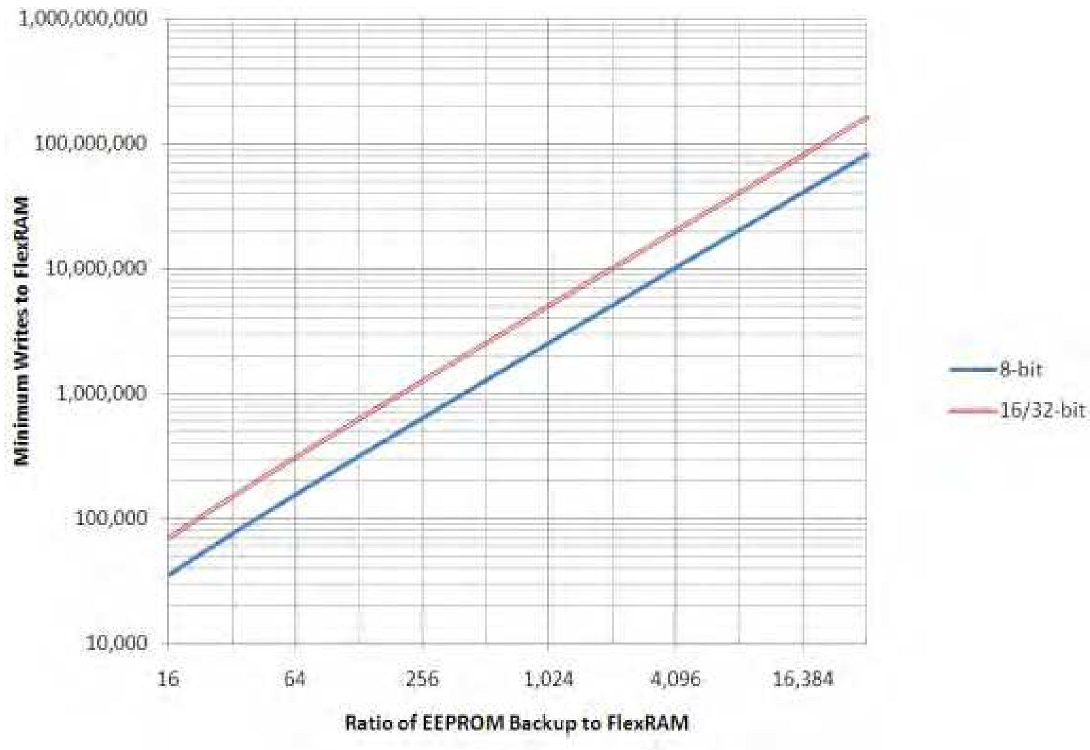


Figure 7. EEPROM backup writes to FlexRAM

8.7.2 EzPort switching specifications

Num	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
EP1	EZP_CK frequency of operation (all commands except READ)	—	$f_{SYS}/2$	MHz
EP1a	EZP_CK frequency of operation (READ command)	—	$f_{SYS}/8$	MHz
EP2	$\overline{EZP\_CS}$ negation to next $\overline{EZP\_CS}$ assertion	2 x t_{EZP_CK}	—	ns
EP3	$\overline{EZP\_CS}$ input valid to EZP_CK high (setup)	5	—	ns
EP4	EZP_CK high to $\overline{EZP\_CS}$ input invalid (hold)	5	—	ns
EP5	EZP_D input valid to EZP_CK high (setup)	2	—	ns
EP6	EZP_CK high to EZP_D input invalid (hold)	5	—	ns
EP7	EZP_CK low to EZP_Q output valid	—		ns
EP8	EZP_CK low to EZP_Q output invalid (hold)	0	—	ns
EP9	$\overline{EZP\_CS}$ negation to EZP_Q tri-state	—	12	ns

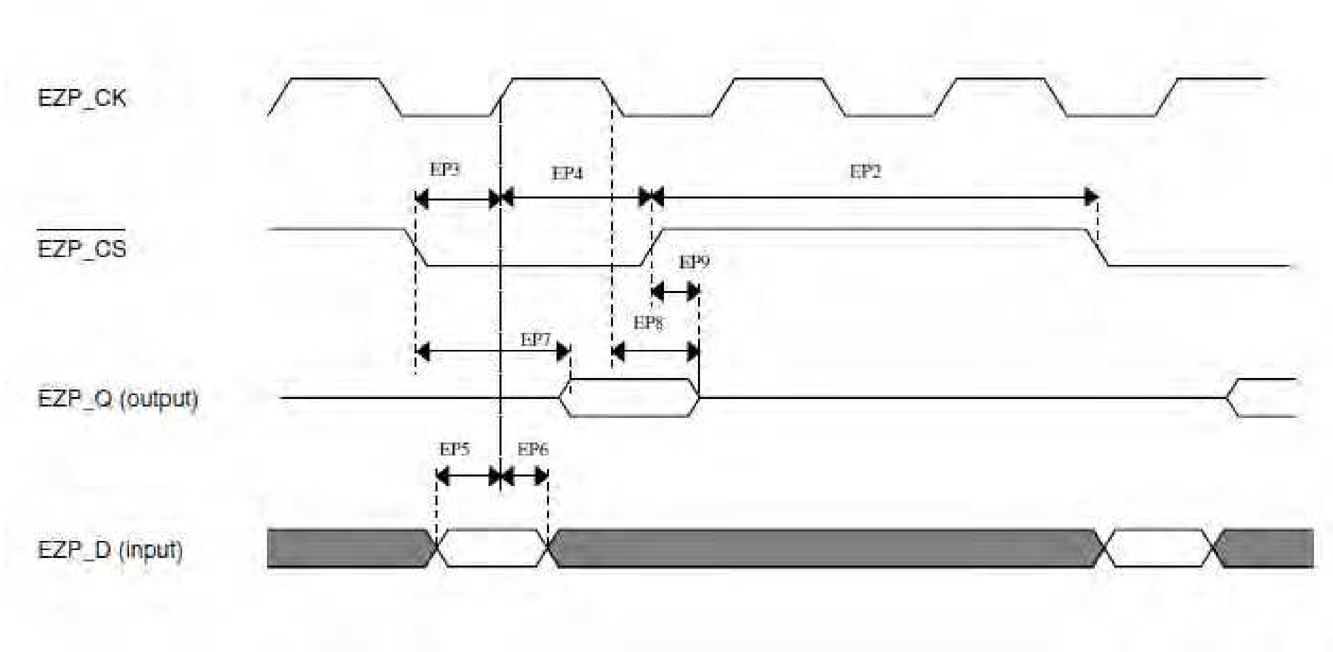


Figure 8. ExPort timing diagram

8.8 Analog

8.8.1 ADC electrical specifications

The 16-bit accuracy specifications are achievable on the differential pins ADCx_DP0, ADCx_DM0.

All other ADC channels meet the 13-bit differential/12-bit single-ended accuracy specifications.

Symbol	Description	Conditions	Min.	Typ.[1]	Max.	Unit	Notes
V_{DDA}	Supply voltage	Absolute	1.71	—	3.6	V	
ΔV_{DDA}	Supply voltage	Delta to V_{DD} (V_{DD}-V_{DDA})	-100	0	+100	mV	2
ΔV_{SSA}	Ground voltage	Delta to V_{SS} (V_{SS}-V_{SSA})	-100	0	+100	mV	2

Symbol	Description	Conditions	Min.	Typ.[1]	Max.	Unit	Notes
V_{REFH}	ADC reference voltage high		1.13	V_{DDA}	V_{DDA}	V	
V_{REFL}	Reference voltage low		V_{SSA}	V_{SSA}	V_{SSA}	V	
V_{ADIN}	Input voltage		V_{REFL}	—	V_{REFH}	V	
C_{ADIN}	Input capacitance	• 16 bit modes • 8/10/12 bit modes	— —	8 4	10 5	pF	
R_{ADIN}	Input resistance		—	2	5	kΩ	
R_{AS}	Analog source resistance	13/12 bit modes f_{ADCK} < 4MHz	—	—	5	kΩ	3
f_{ADCK}	ADC conversion clock frequency	≤ 13 bit modes	1.0	—	18.0	MHz	4
f_{ADCK}	ADC conversion clock frequency	16 bit modes	2.0	—	12.0	MHz	4
C_{rate}	ADC conversion rate	≤ 13 bit modes No ADC hardware averaging Continuous conversions enabled, subsequent conversion time	20.000	—	818.330	Ksps	5
C_{rate}	ADC conversion rate	16 bit modes No ADC hardware averaging Continuous conversions enabled, subsequent conversion time	37.037	—	461.467	Ksps	5

1. Typical values assume V_{DDA} = 3.0 V, Temp = 25°C, f_{ADCK} = 1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
2. DC potential difference.
3. This resistance is external to MCU. The analog source resistance should be kept as low as possible in order to achieve the best results. The results in this datasheet were derived from a system which has <8 Ω analog source resistance. The R_{AS}/C_{AS} time constant should be kept to <1ns.
4. To use the maximum ADC conversion clock frequency, the ADHSC bit should be set and the ADLPC bit should be clear.
5. For guidelines and examples of conversion rate calculation, download the ADC calculator tool: http://cache.freescale.com/files/soft_dev_tools/software/app_software/converters/ADC_CALCULATOR_CNV.zip?fpsp=1

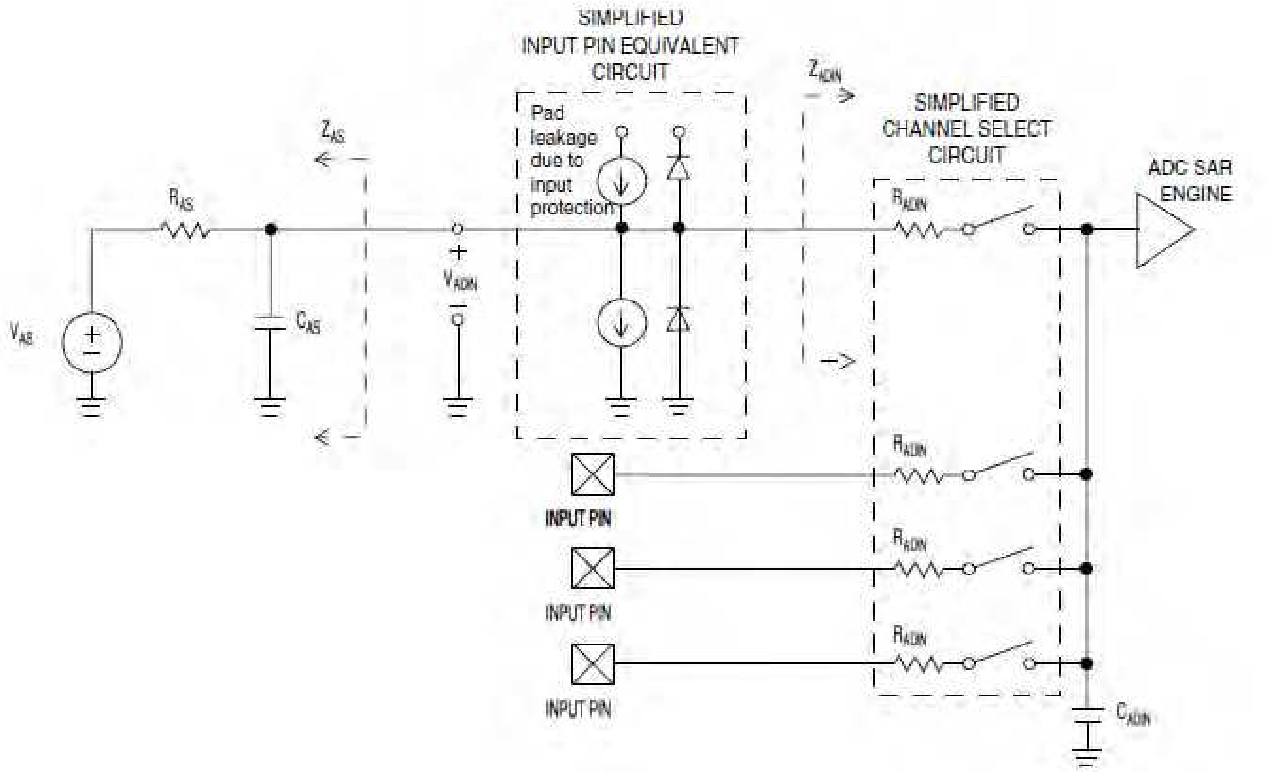


Figure 9. ADC input impedance equivalency diagram

8.8.1.1 16-bit ADC electrical characteristics

Symbol	Description	Conditions[1]	Min.	Typ.[2]	Max.	Unit	Notes
I_{DDA_ADC}	Supply current		0.215	—	1.7	mA	3
f_{ADACK}	ADC asynchronous clock source	• ADLPC=1, ADHSC=0 • ADLPC=1, ADHSC=1 • ADLPC=0, ADHSC=0 • ADLPC=0, ADHSC=1	1.2 3.0 2.4 4.4	2.4 4.0 5.2 6.2	3.9 7.3 6.1 9.5	MHz MHz MHz MHz	t_{ADACK} = 1/ f_{ADACK}
	Sample Time	See Reference Manual chapter for sample times					
TUE	Total unadjusted error	• 12 bit modes • <12 bit modes	— —	±4 ±1.4	±6.8 ±2.1	LSB[4]	5
DNL	Differential non-linearity	• 12 bit modes • <12 bit modes	— —	±0.7 ±0.2	-1.1 to +1.9 -0.3 to 0.5	LSB[4]	5
INL	Integral non-linearity	• 12 bit modes • <12 bit modes	— —	±1.0 ±0.5	-2.7 to +1.9 -0.7 to +0.5	LSB[4]	5
E_{FS}	Full-scale error	• 12 bit modes • <12 bit modes	— —	-4 -1.4	-5.4 -1.8	LSB[4]	V_{ADIN} = V_{DDA} 5

Table continues on the next page...

Symbol	Description	Conditions[1]	Min.	Typ.[2]	Max.	Unit	Notes

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{DDA_DACLP}	Supply current — low-power mode	—	—	150	μA	
I_{DDA_DACHP}	Supply current — high-speed mode	—	—	700	μA	
t_{DACLP}	Full-scale settling time (0x080 to 0xF7F) — low-power mode	—	100	200	μs	1
t_{DACHP}	Full-scale settling time (0x080 to 0xF7F) — high-power mode	—	15	30	μs	1
$t_{CCDACLP}$	Code-to-code settling time (0xBF8 to 0xC08) — low-power mode and high-speed mode	—	0.7	1	μs	1
$V_{dacoutl}$	DAC output voltage range low — high-speed mode, no load, DAC set to 0x000	—	—	100	mV	
$V_{dacouth}$	DAC output voltage range high — high-speed mode, no load, DAC set to 0xFFF	V_{DACR} −100	—	V_{DACR}	mV	
INL	Integral non-linearity error — high speed mode	—	—	±8	LSB	2
DNL	Differential non-linearity error — V_{DACR} > 2 V	—	—	±1	LSB	3
DNL	Differential non-linearity error — V_{DACR} = VREF_OUT	—	—	±1	LSB	4
V_{OFFSET}	Offset error	—	±0.4	±0.8	%FSR	5
E_G	Gain error	—	±0.1	±0.6	%FSR	5
PSRR	Power supply rejection ratio, V_{DDA} > = 2.4 V	60	—	90	dB	
T_{CO}	Temperature coefficient offset voltage	—	3.7	—	μV/C	6
T_{GE}	Temperature coefficient gain error	—	0.000421	—	%FSR/C	
Rop	Output resistance load = 3 kΩ	—	—	250	Ω	
SR	Slew rate -80h→ F7Fh→ 80h • High power (SP_{HP}) • Low power (SP_{LP})	 1.2 0.05	 1.7 0.12	 — —	V/μs	
CT	Channel to channel cross talk	—	—	-80	dB	
BW	3dB bandwidth • High power (SP_{HP}) • Low power (SP_{LP})	 550 40	 — —	 — —	kHz	

1. Settling within ±1 LSB
2. The INL is measured for 0+100mV to V_{DACR}−100 mV
3. The DNL is measured for 0+100 mV to V_{DACR}−100 mV
4. The DNL is measured for 0+100mV to V_{DACR}−100 mV with V_{DDA} > 2.4V
5. Calculated by a best fit curve from V_{SS}+100 mV to V_{DACR}−100 mV
6. VDDA = 3.0V, reference select set for VDDA (DACx_CO:DACRFS = 1), high power mode(DACx_C0:LPEN = 0), DAC set to 0x800, Temp range from -40C to 105C

7. Input data is 1 kHz sine wave. ADC conversion clock <12MHz.

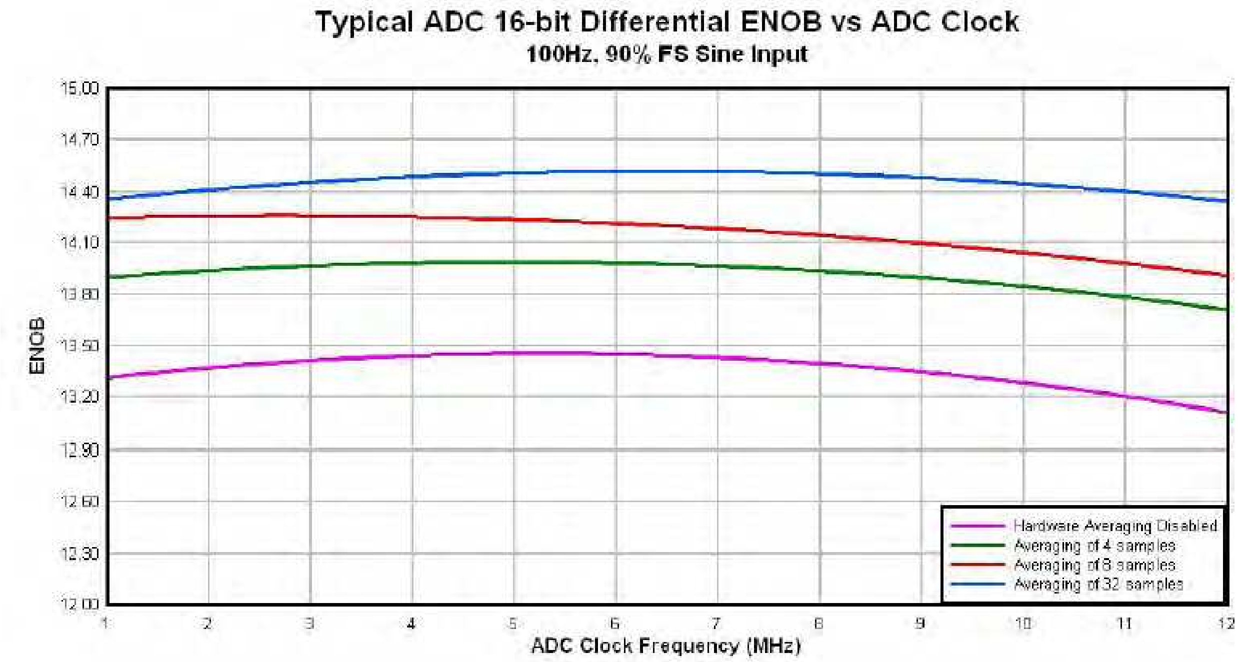


Figure 10. Typical ENOB vs. ADC_CLK for 16-bit differential mode

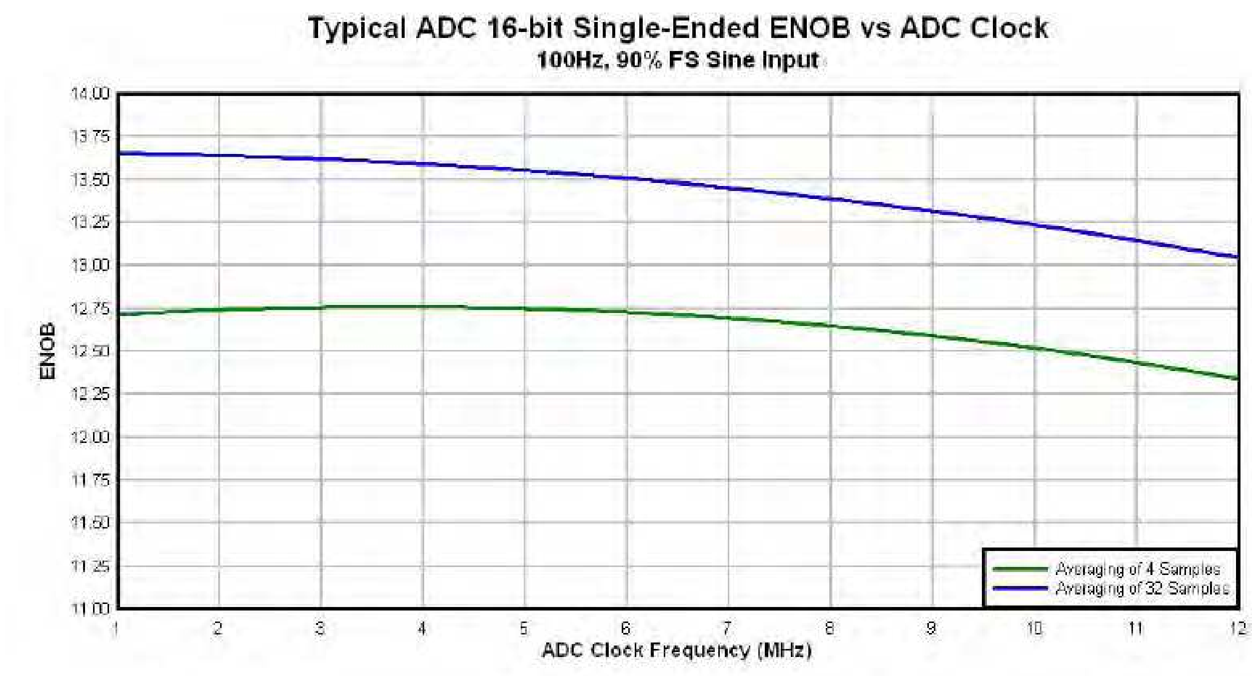


Figure 11. Typical ENOB vs. ADC_CLK for 16-bit single-ended mode

8.8.2 CMP and 6-bit DAC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit
V_{DD}	Supply voltage	1.71	—	3.6	V
I_{DDHS}	Supply current, High-speed mode (EN=1, PMODE=1)	—	—	200	μA
I_{DDLS}	Supply current, low-speed mode (EN=1, PMODE=0)	—	—	20	μA
V_{AIN}	Analog input voltage	$V_{SS} - 0.3$	—	V_{DD}	V
V_{AIO}	Analog input offset voltage	—	—	20	mV
V_H	Analog comparator hysteresis[1]				
	• CR0[HYSTCTR] = 00	—	5	—	mV
	• CR0[HYSTCTR] = 01	—	10	—	mV
	• CR0[HYSTCTR] = 10	—	20	—	mV
	• CR0[HYSTCTR] = 11	—	30	—	mV
V_{CMPOh}	Output high	$V_{DD} - 0.5$	—	—	V
V_{CMPOl}	Output low	—	—	0.5	V
t_{DHS}	Propagation delay, high-speed mode (EN=1, PMODE=1)	20	50	200	ns
t_{DLS}	Propagation delay, low-speed mode (EN=1, PMODE=0)	80	250	600	ns
	Analog comparator initialization delay[2]	—	—	40	μs
I_{DAC6b}	6-bit DAC current adder (enabled)	—	7	—	μA
INL	6-bit DAC integral non-linearity	–0.5	—	0.5	LSB[3]
DNL	6-bit DAC differential non-linearity	–0.3	—	0.3	LSB

1. Typical hysteresis is measured with input voltage range limited to 0.6 to V_{DD}-0.6V.
2. Comparator initialization delay is defined as the time between software writes to change control inputs (Writes to DACEN, VRSEL, PSEL, MSEL, VOSEL) and the comparator output settling to a stable level.
3. 1 LSB = $V_{reference}/64$

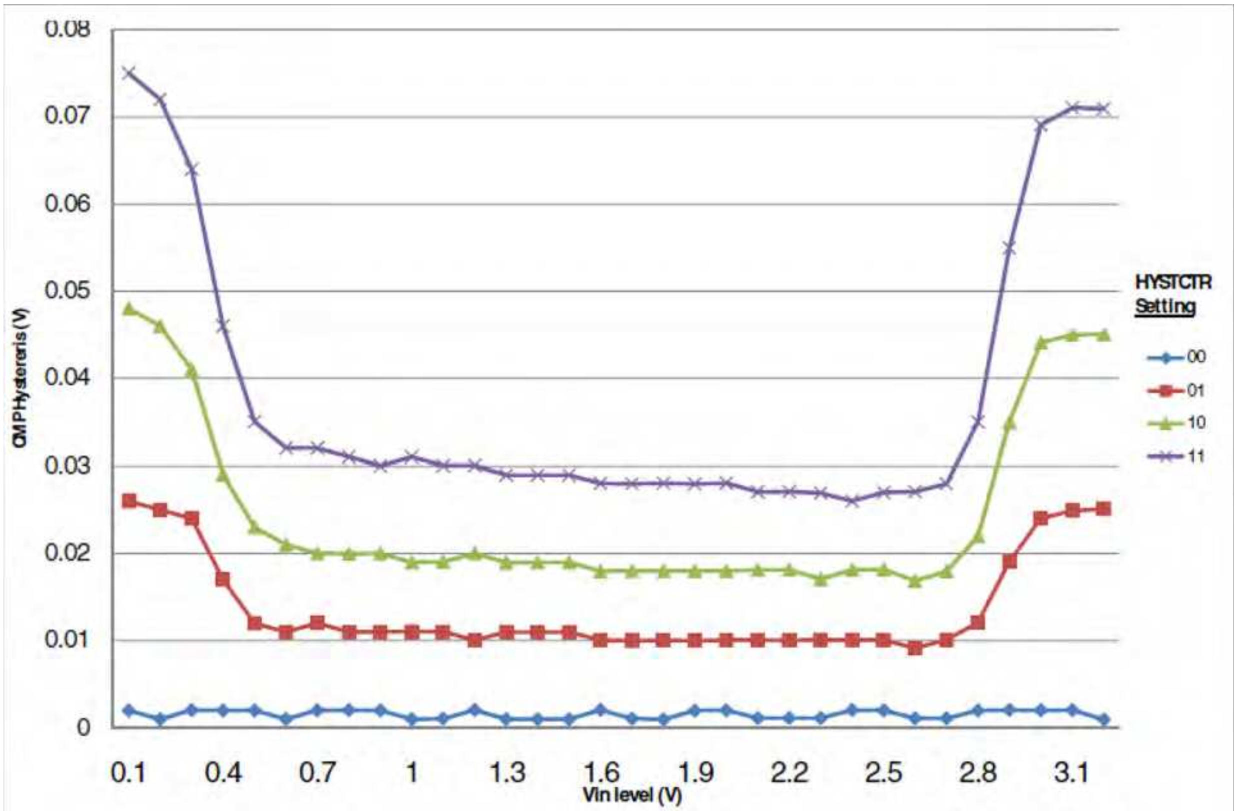


Figure 12. Typical hysteresis vs. Vin level (VDD=3.3 V, PMODE=0)

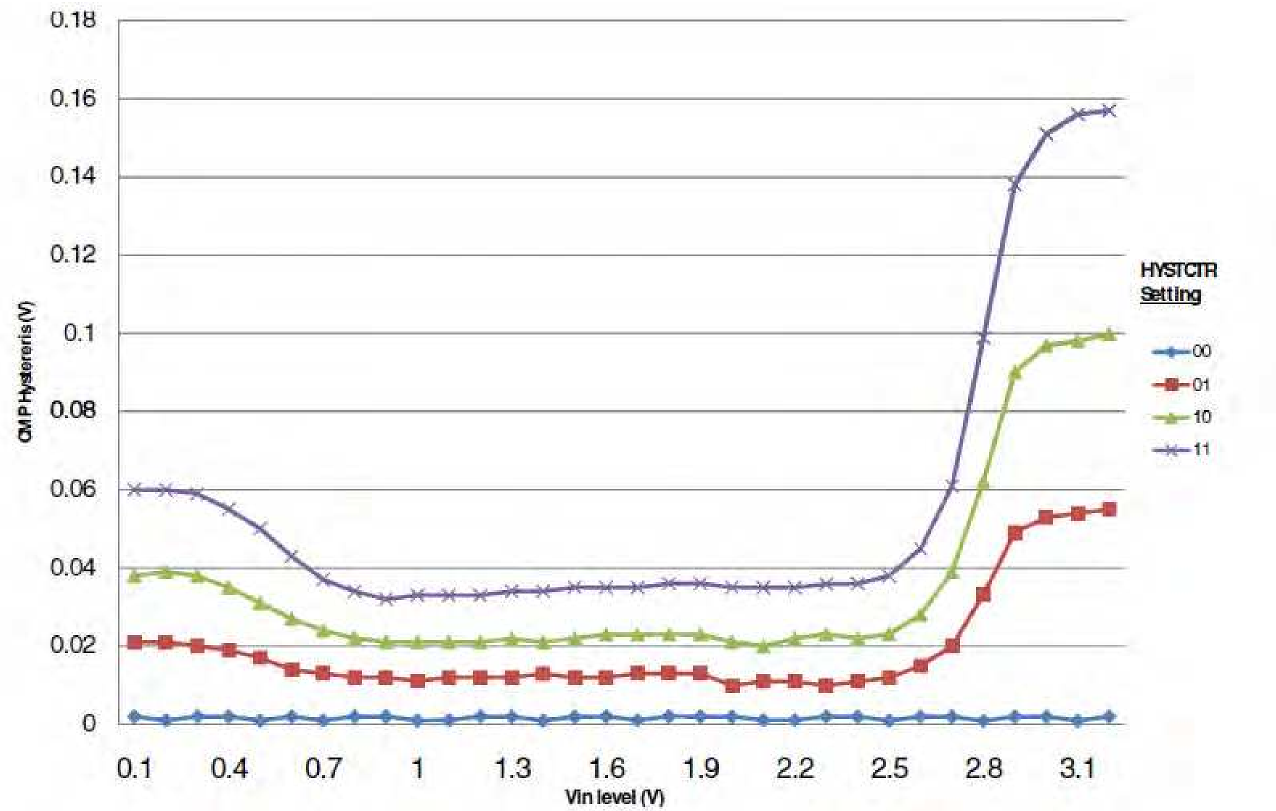


Figure 13. Typical hysteresis vs. Vin level (VDD=3.3 V, PMODE=1)

8.8.3 12-bit DAC electrical characteristics

8.8.3.1 12-bit DAC operating requirements

Symbol	Desciption	Min.	Max.	Unit	Notes
V_{DDA}	Supply voltage	1.71	3.6	V	
V_{DACR}	Reference voltage	1.13	3.6	V	1
T_A	Temperature	−40	105	°C	
C_L	Output load capacitance	—	100	pF	2
I_L	Output load current	—	1	mA	

1. The DAC reference can be selected to be VDDA or the voltage output of the VREF module (VREF_OUT)
2. A small load capacitance (47 pF) can improve the bandwidth performance of the DAC

8.8.3.2 12-bit DAC operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{DDA_DACLP}	Supply current — low-power mode	—	—	150	μA	
I_{DDA_DACHP}	Supply current — high-speed mode	—	—	700	μA	
t_{DACLP}	Full-scale settling time (0x080 to 0xF7F) — low-power mode	—	100	200	μs	1
t_{DACHP}	Full-scale settling time (0x080 to 0xF7F) — high-power mode	—	15	30	μs	1
$t_{CCDACLP}$	Code-to-code settling time (0xBF8 to 0xC08) — low-power mode and high-speed mode	—	0.7	1	μs	1
$V_{dacoutl}$	DAC output voltage range low — high-speed mode, no load, DAC set to 0x000	—	—	100	mV	
$V_{dacouth}$	DAC output voltage range high — high-speed mode, no load, DAC set to 0xFFF	V_{DACR} −100	—	V_{DACR}	mV	
INL	Integral non-linearity error — high speed mode	—	—	±8	LSB	2
DNL	Differential non-linearity error — V_{DACR} > 2 V	—	—	±1	LSB	3
DNL	Differential non-linearity error — V_{DACR} = VREF_OUT	—	—	±1	LSB	4
V_{OFFSET}	Offset error	—	±0.4	±0.8	%FSR	5
E_G	Gain error	—	±0.1	±0.6	%FSR	5
PSRR	Power supply rejection ratio, V_{DDA} > = 2.4 V	60	—	90	dB	
T_{CO}	Temperature coefficient offset voltage	—	3.7	—	μV/C	6
T_{GE}	Temperature coefficient gain error	—	0.000421	—	%FSR/C	
Rop	Output resistance load = 3 kΩ	—	—	250	Ω	
SR	Slew rate -80h→ F7Fh→ 80h • High power (SP_{HP}) • Low power (SP_{LP})	 1.2 0.05	 1.7 0.12	 — —	V/μs	
CT	Channel to channel cross talk	—	—	-80	dB	
BW	3dB bandwidth • High power (SP_{HP}) • Low power (SP_{LP})	 550 40	 — —	 — —	kHz	

1. Settling within ±1 LSB
2. The INL is measured for 0+100mV to V_{DACR}−100 mV
3. The DNL is measured for 0+100 mV to V_{DACR}−100 mV
4. The DNL is measured for 0+100mV to V_{DACR}−100 mV with V_{DDA} > 2.4V
5. Calculated by a best fit curve from V_{SS}+100 mV to V_{DACR}−100 mV
6. VDDA = 3.0V, reference select set for VDDA (DACx_CO:DACRFS = 1), high power mode(DACx_C0:LPEN = 0), DAC set to 0x800, Temp range from -40C to 105C

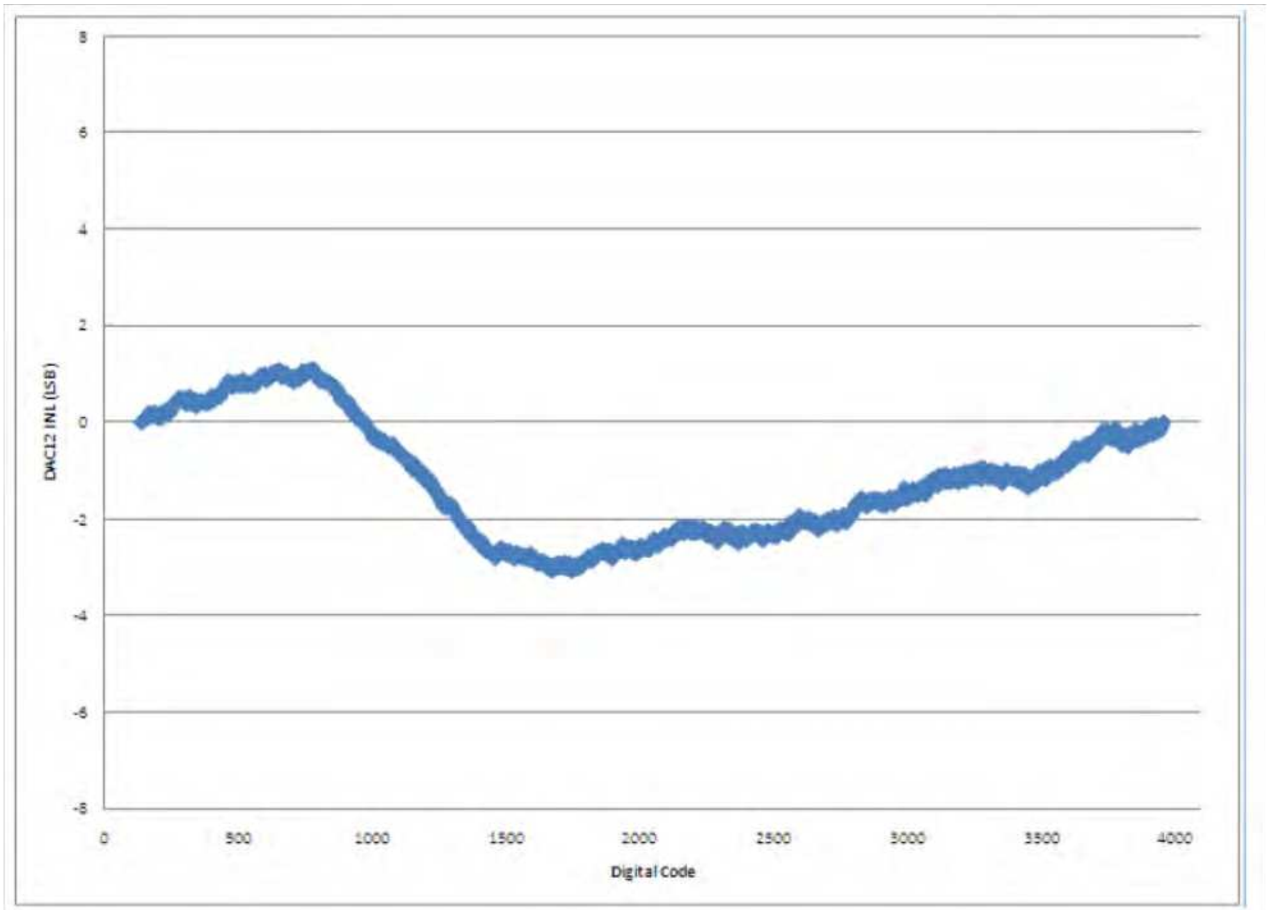


Figure 14. Typical INL error vs. digital code

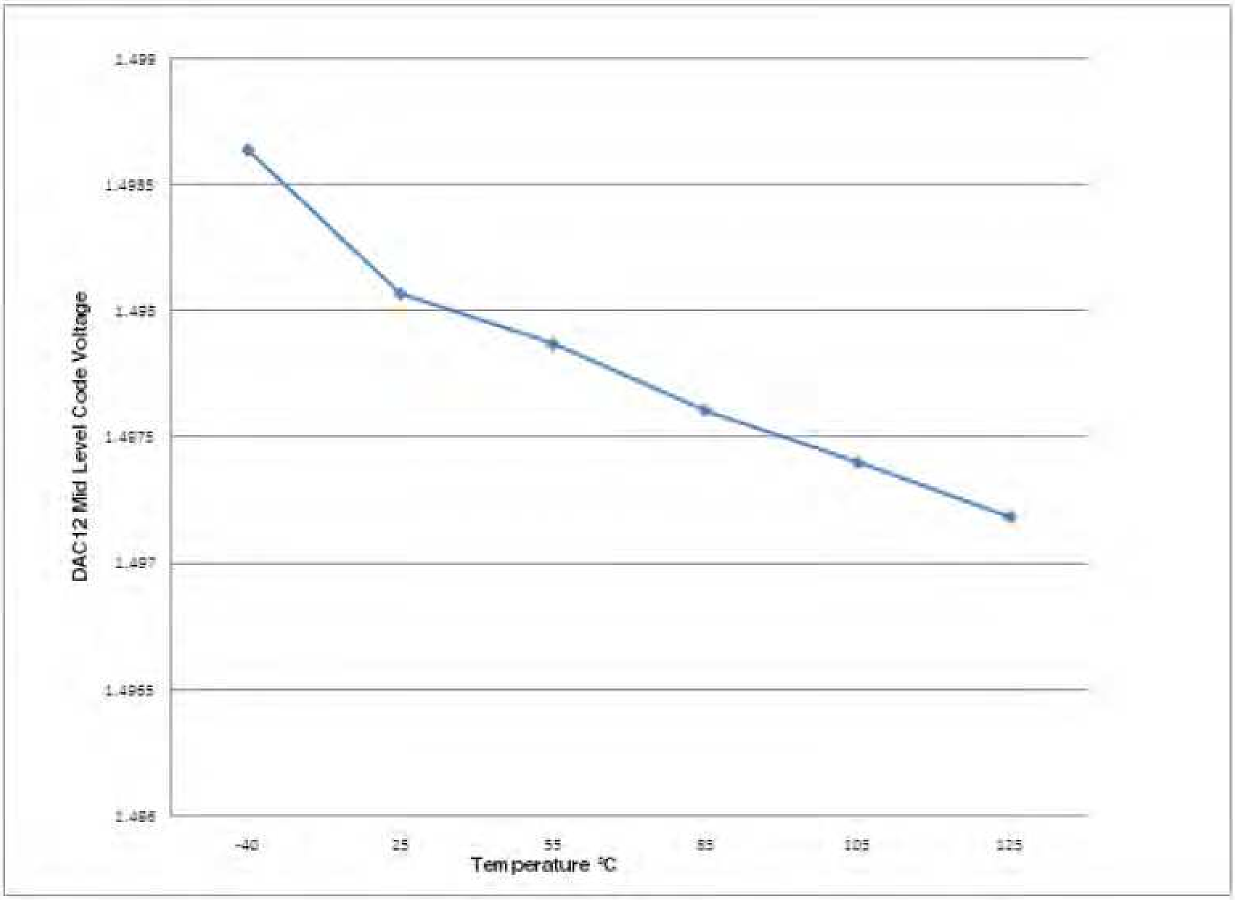


Figure 15. Offset at half scale vs. temperature

8.8.4 Voltage reference electrical specifications

8.8.4.1 VREF full-range operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
V_{DDA}	Supply voltage	1.71	3.6	V	
T_A	Temperature	–40	105	°C	
C_L	Output load capacitance	100		nF	1, 2

1. C_L must be connected to VREF_OUT if the VREF_OUT functionality is being used for either an internal or external reference.
2. The load capacitance should not exceed +/-25% of the nominal specified C_L value over the operating temperature range of the device.

8.8.4.2 VREF full-range operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{out}	Voltage reference output with factory trim at nominal V_{DDA} and temperature=25C	1.1915	1.195	1.1977	V	
V_{out}	Voltage reference output — factory trim	1.1584	—	1.2376	V	
V_{out}	Voltage reference output — user trim	1.193	—	1.197	V	
V_{step}	Voltage reference trim step	—	0.5	—	mV	
V_{tdrift}	Temperature drift (Vmax -Vmin across the full temperature range)	—	—	80	mV	
I_{bg}	Bandgap only current	—	—	80	µA	1
ΔV_{LOAD}	Load regulation • current = ± 1.0 mA	—	200	—	µV	1, 2
T_{stup}	Buffer startup time	—	—	100	µs	
V_{vdrift}	Voltage drift (Vmax -Vmin across the full voltage range)	—	2	—	mV	1

1. See the chip's Reference Manual for the appropriate settings of the VREF Status and Control register.
2. Load regulation voltage is the difference between the VREF_OUT voltage with no load vs. voltage with defined load

8.8.4.3 VREF limited-range operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
T_A	Temperature	0	50	°C	

8.8.4.4 VREF limited-range operating behaviors

Symbol	Description	Min.	Max.	Unit	Notes
V_{out}	Voltage reference output with factory trim	1.173	1.225	V	

8.9 Communication interfaces

8.9.1 USB electrical specifications

The USB electricals for the USB On-the-Go module conform to the standards documented by the Universal Serial Bus Implementers Forum. For the most up-to-date standards, visit http://www.usb.org.

8.9.2 USB DCD electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit
V_{DP_SRC}	USB_DP source voltage (up to 250 µA)	0.5	—	0.7	V
V_{LGC}	Threshold voltage for logic high	0.8	—	2.0	V
I_{DP_SRC}	USB_DP source current	7	10	13	µA
I_{DM_SINK}	USB_DM sink current	50	100	150	µA
R_{DM_DWN}	D- pulldown resistance for data pin contact detect	14.25	—	24.8	kΩ
V_{DAT_REF}	Data detect voltage	0.25	0.33	0.4	V

8.9.3 VREG electrical specifications

Symbol	Description	Min.	Typ.[1]	Max.	Unit	Notes
VREGIN	Input supply voltage	2.7	—	5.5	V	
I_{DDon}	Quiescent current — Run mode, load current equal zero, input supply (VREGIN) > 3.6 V	—	120	186	µA	
I_{DDstby}	Quiescent current — Standby mode, load current equal zero	—	1.1	1.54	µA	
I_{DDoff}	Quiescent current — Shutdown mode • VREGIN = 5.0 V and temperature=25C • Across operating voltage and temperature	 — —	 650 —	 — 4	 nA µA	
$I_{LOADrun}$	Maximum load current — Run mode	—	—	120	mA	
$I_{LOADstby}$	Maximum load current — Standby mode	—	—	1	mA	
$V_{Reg33out}$	Regulator output voltage — Input supply (VREGIN) > 3.6 V • Run mode • Standby mode	 3 2.1	 3.3 2.8	 3.6 3.6	 V V	
$V_{Reg33out}$	Regulator output voltage — Input supply (VREGIN) < 3.6 V, pass-through mode	2.1	—	3.6	V	2
C_{OUT}	External output capacitor	1.76	2.2	8.16	µF	
ESR	External output capacitor equivalent series resistance	1	—	100	mΩ	
I_{LIM}	Short circuit current	—	290	—	mA	

1. Typical values assume VREGIN = 5.0 V, Temp = 25 °C unless otherwise stated.
2. Operating in pass-through mode: regulator output voltage equal to the input voltage minus a drop proportional to I_{Load}.

8.9.4 DSPI switching specifications (limited voltate range)

The DMA Serial Peripheral Interface (DSPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The tables below provide DSPI timing characteristics for classic SPI timing modes. Refer to the DSPI chapter of the Reference Manual for information on the modified transfer formats used for communicating with slower peripheral devices.

Master mode

Num	Description	Min.	Max.	Unit	Notes
	Operating voltage	2.7	3.6	V	
	Frequency of operation	—	25	MHz	
DS1	DSPI_SCK output cycle time	2 x t_{BUS}	—	ns	
DS2	DSPI_SCK output high/low time	$(t_{SCK}/2) - 2$	$(t_{SCK}/2) + 2$	ns	
DS3	DSPI_PCS*n* valid to DSPI_SCK delay	$(t_{BUS} \times 2) - 2$	—	ns	1
DS4	DSPI_SCK to DSPI_PCS*n* invalid delay	$(t_{BUS} \times 2) - 2$	—	ns	2
DS5	DSPI_SCK to DSPI_SOUT valid	—	8.5	ns	
DS6	DSPI_SCK to DSPI_SOUT invalid	–2	—	ns	
DS7	DSPI_SIN to DSPI_SCK input setup	15	—	ns	
DS8	DSPI_SCK to DSPI_SIN input hold	0	—	ns	

1. The delay is programmable in SPIx_CTARn[PSSCK] and SPIx_CTARn[CSSCK].
2. The delay is programmable in SPIx_CTARn[PASC] and SPIx_CTARn[ASC].

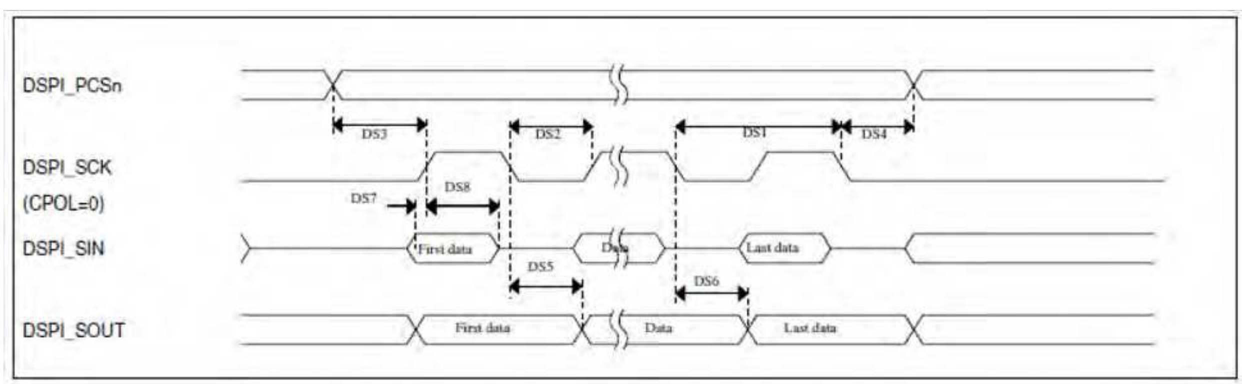


Figure 16. DSPI classic SPI timing — master mode

Slave mode

Num	Description	Min.	Max.	Unit
	Operating voltage	2.7	3.6	V
	Frequency of operation		12.5	MHz
DS9	DSPI_SCK input cycle time	4 x t_{BUS}	—	ns
DS10	DSPI_SCK input high/low time	$(t_{SCK}/2) - 2$	$(t_{SCK}/2) + 2$	ns
DS11	DSPI_SCK to DSPI_SOUT valid	—	10	ns
DS12	DSPI_SCK to DSPI_SOUT invalid	0	—	ns
DS13	DSPI_SIN to DSPI_SCK input setup	2	—	ns
DS14	DSPI_SCK to DSPI_SIN input hold	7	—	ns
DS15	$\overline{DSPI\_SS}$ active to DSPI_SOUT driven	—	14	ns
DS16	$\overline{DSPI\_SS}$ inactive to DSPI_SOUT not driven	—	14	ns

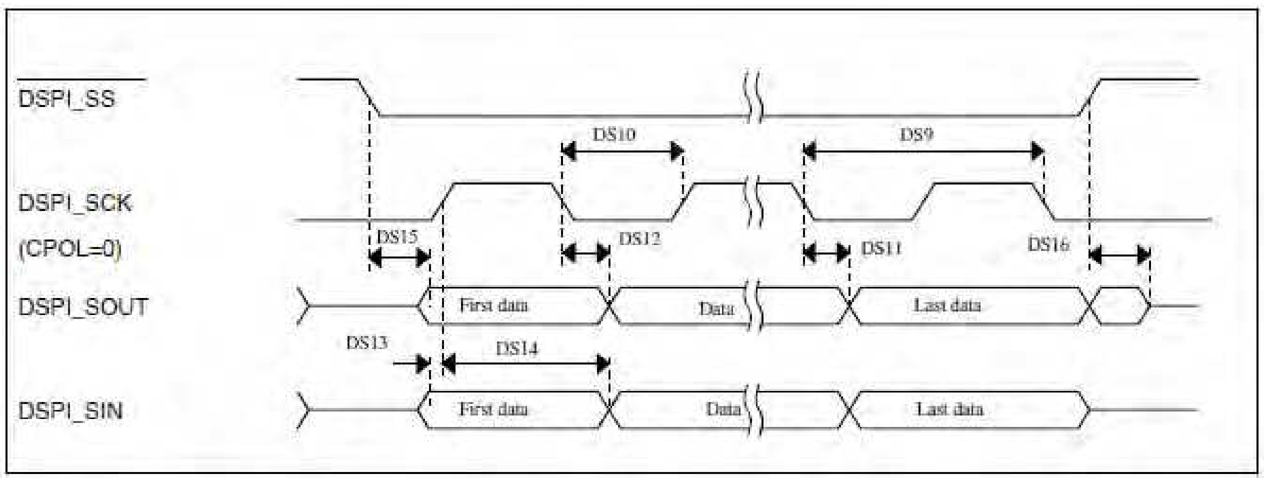


Figure 17. DSPI classic SPI timing — slave mode

8.9.5 DSPI switching specification (full voltage range)

The DMA Serial Peripheral Interface (DSPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The tables below provides DSPI timing characteristics for classic SPI timing modes. Refer to the DSPI chapter of the Reference Manual for information on the modified transfer formats used for communicating with slower peripheral devices.

Master mode DSPI timing (full voltage range)

Num	Description	Min.	Max.	Unit	Notes
	Operating voltage	1.71	3.6	V	1
	Frequency of operation	—	12.5	MHz	
DS1	DSPI_SCK output cycle time	4 x t_{BUS}	—	ns	
DS2	DSPI_SCK output high/low time	(t_{SCK}/2) - 4	($t_{SCK/2)}$ + 4	ns	
DS3	DSPI_PCS*n* valid to DSPI_SCK delay	(t_{BUS} x 2) − 4	—	ns	2
DS4	DSPI_SCK to DSPI_PCS*n* invalid delay	(t_{BUS} x 2) − 4	—	ns	3
DS5	DSPI_SCK to DSPI_SOUT valid	—	10	ns	
DS6	DSPI_SCK to DSPI_SOUT invalid	-4.5	—	ns	
DS7	DSPI_SIN to DSPI_SCK input setup	20.5	—	ns	
DS8	DSPI_SCK to DSPI_SIN input hold	0	—	ns	

1. The DSPI module can operate across the entire operating voltage for the processor, but to run across the full voltage range the maximum frequency of operation is reduced.
2. The delay is programmable in SPIx_CTARn[PSSCK] and SPIx_CTARn[CSSCK].
3. The delay is programmable in SPIx_CTARn[PASC] and SPIx_CTARn[ASC].

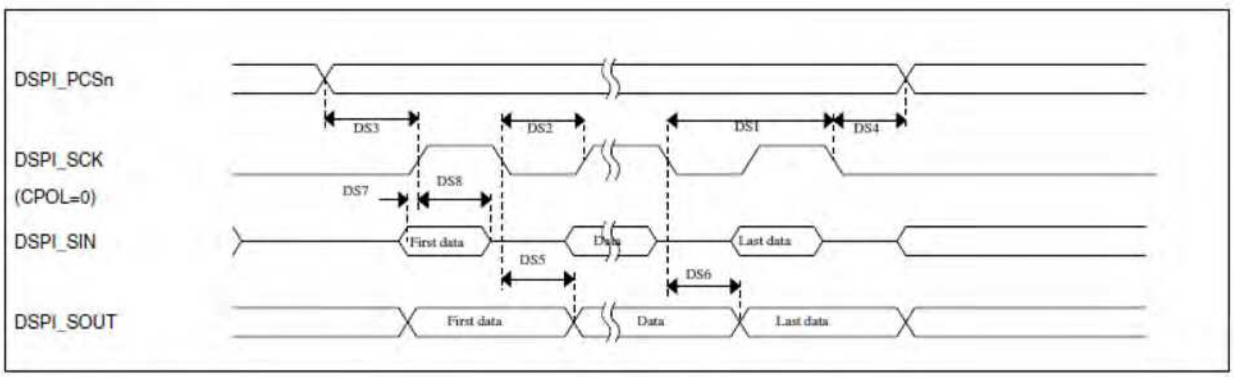


Figure 18. DSPI classic SPI timing — master mode

Slave mode DSPI timing (full voltage range)

Num	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V

Num	Description	Min.	Max.	Unit
	Frequency of operation	—	6.25	MHz
DS9	DSPI_SCK input cycle time	8 x t_{BUS}	—	ns
DS10	DSPI_SCK input high/low time	$(t_{SCK}/2) - 4$	$(t_{SCK/2}) + 4$	ns
DS11	DSPI_SCK to DSPI_SOUT valid	—	20	ns
DS12	DSPI_SCK to DSPI_SOUT invalid	0	—	ns
DS13	DSPI_SIN to DSPI_SCK input setup	2	—	ns
DS14	DSPI_SCK to DSPI_SIN input hold	7	—	ns
DS15	$\overline{\text{DSPI\_SS}}$ active to DSPI_SOUT driven	—	19	ns
DS16	$\overline{\text{DSPI\_SS}}$ inactive to DSPI_SOUT not driven	—	19	ns

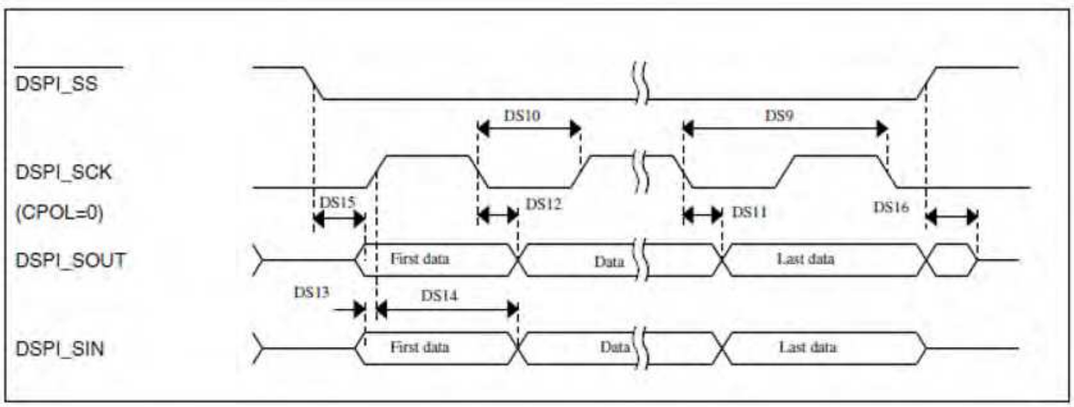


Figure 19. DSPI classic SPI timing — slave mode

8.9.6 Normal Run, Wait and Stop mode performance over the fulloperating voltage range

This section provides the operating performance over the full operating voltage for the device in Normal Run, Wait and Stop modes.

I2S/SAI master mode timing

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S1	I2S_MCLK cycle time	40	—	ns
S2	I2S_MCLK pulse width high/low	45%	55%	MCLK period
S3	I2S_TX_BCLK/I2S_RX_BCLK cycle time (output)	80	—	ns
S4	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low	45%	55%	BCLK period
S5	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output valid	—	15	ns
S6	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output invalid	0	—	ns
S7	I2S_TX_BCLK to I2S_TXD valid	—	15	ns
S8	I2S_TX_BCLK to I2S_TXD invalid	0	—	ns
S9	I2S_RXD/I2S_RX_FS input setup before I2S_RX_BCLK	25	—	ns
S10	I2S_RXD/I2S_RX_FS input hold after I2S_RX_BCLK	0	—	ns

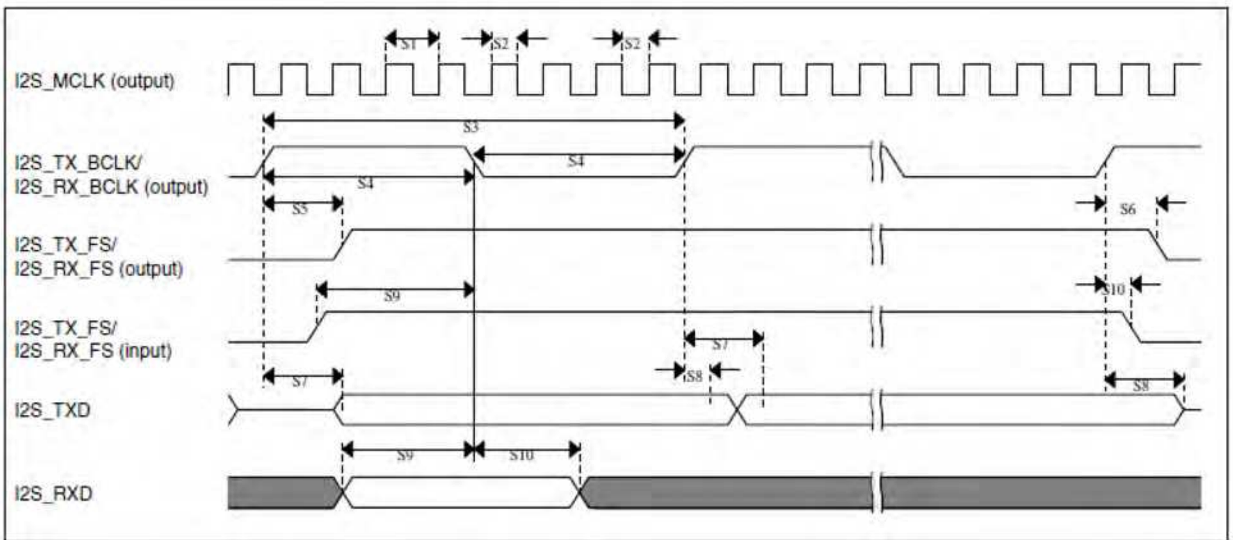


Figure 20. I2S/SAI timing — master modes

I2S/SAI slave mode timing

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S11	I2S_TX_BCLK/I2S_RX_BCLK cycle time (input)	80	—	ns
S12	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low (input)	45%	55%	MCLK period
S13	I2S_TX_FS/I2S_RX_FS input setup before I2S_TX_BCLK/I2S_RX_BCLK	10	—	ns
S14	I2S_TX_FS/I2S_RX_FS input hold after I2S_TX_BCLK/I2S_RX_BCLK	2	—	ns
S15	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output valid	—	29	ns
S16	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output invalid	0	—	ns
S17	I2S_RXD setup before I2S_RX_BCLK	10	—	ns
S18	I2S_RXD hold after I2S_RX_BCLK	2	—	ns
S19	I2S_TX_FS input assertion to I2S_TXD output valid[1]	—	21	ns

1. Applies to first bit in each frame and only if the TCR4[FSE] bit is clear

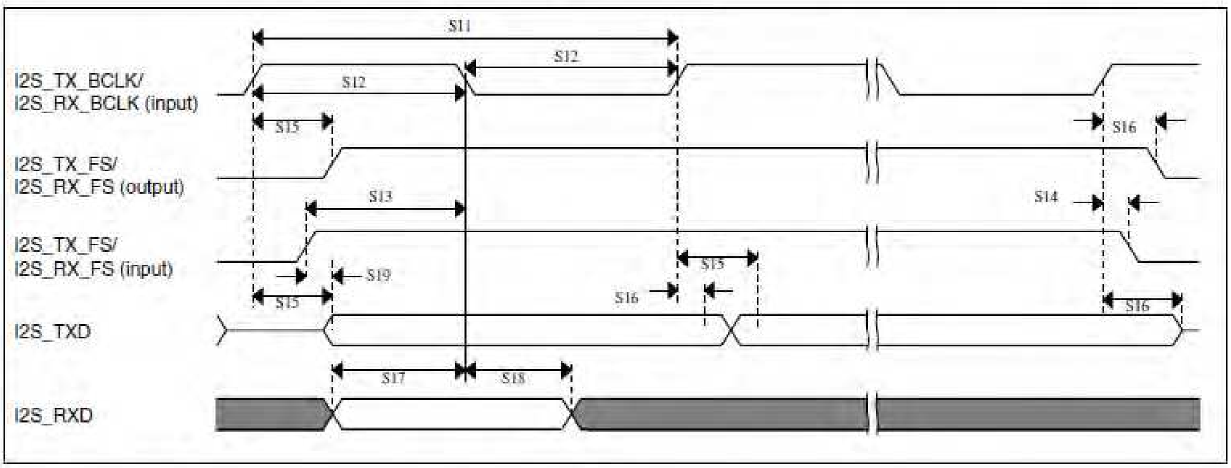


Figure 21. I2S/SAI timing — slave modes

8.9.7 VLPR, VLPW, and VLPS mode performance over the full operating voltage range

This section provides the operating performance over the full operating voltage for the device in VLPR, VLPW, and VLPS modes.

I2S/SAI master mode timing in VLPR, VLPW, and VLPS modes (full voltage range)

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S1	I2S_MCLK cycle time	62.5	—	ns
S2	I2S_MCLK pulse width high/low	45%	55%	MCLK period
S3	I2S_TX_BCLK/I2S_RX_BCLK cycle time (output)	250	—	ns
S4	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low	45%	55%	BCLK period
S5	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output valid	—	45	ns
S6	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output invalid	0	—	ns
S7	I2S_TX_BCLK to I2S_TXD valid	—	45	ns
S8	I2S_TX_BCLK to I2S_TXD invalid	0	—	ns
S9	I2S_RXD/I2S_RX_FS input setup before I2S_RX_BCLK	75	—	ns
S10	I2S_RXD/I2S_RX_FS input hold after I2S_RX_BCLK	0	—	ns

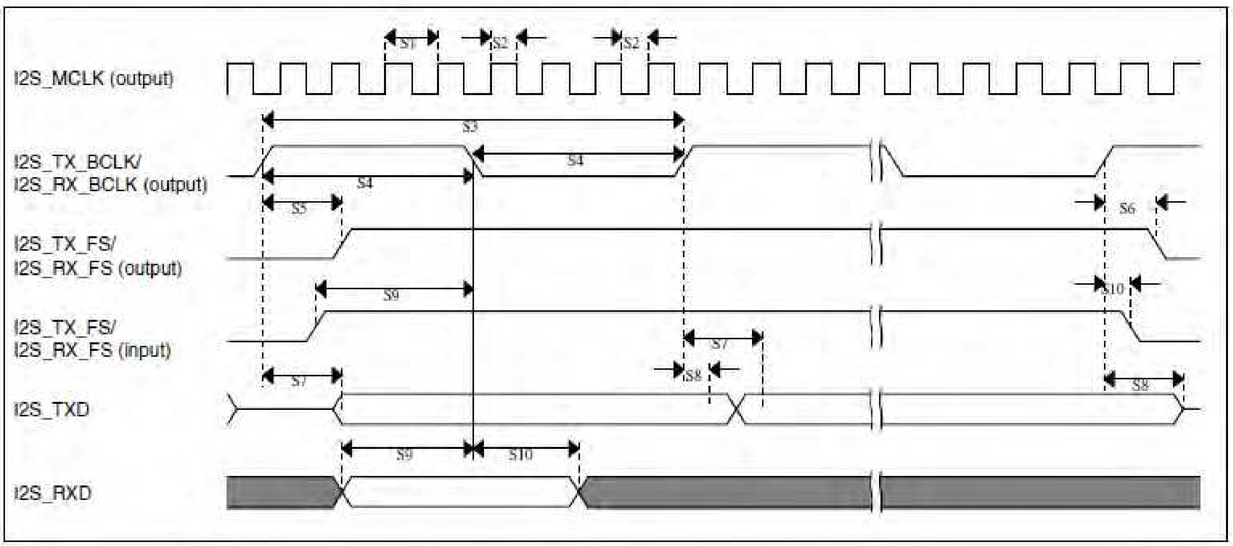


Figure 22. I2S/SAI timing — master modes

I2S/SAI slave mode timing in VLPR, VLPW, and VLPS modes (full voltage range)

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S11	I2S_TX_BCLK/I2S_RX_BCLK cycle time (input)	250	—	ns
S12	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low (input)	45%	55%	MCLK period

Num.	Characteristic	Min.	Max.	Unit
S13	I2S_TX_FS/I2S_RX_FS input setup before I2S_TX_BCLK/I2S_RX_BCLK	30	—	ns
S14	I2S_TX_FS/I2S_RX_FS input hold after I2S_TX_BCLK/I2S_RX_BCLK	2	—	ns
S15	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output valid	—	87	ns
S16	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output invalid	0	—	ns
S17	I2S_RXD setup before I2S_RX_BCLK	30	—	ns
S18	I2S_RXD hold after I2S_RX_BCLK	2	—	ns
S19	I2S_TX_FS input assertion to I2S_TXD output valid[1]	—	72	ns

1. Applies to first bit in each frame and only if the TCR4[FSE] bit is clear

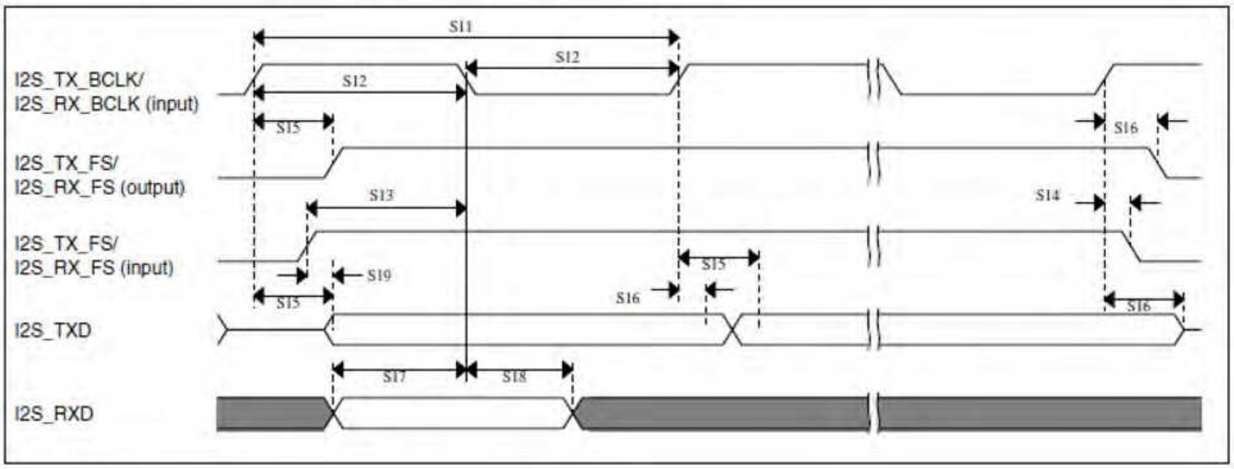


Figure 23. I2S/SAI timing — slave modes

9 Transceiver electrical characteristics

9.1 DC electrical characteristics

Table 10. DC electrical characteristics
(VBATT, VDDINT = 2.7 V, T_A=25°C, unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Power Supply Current (VBATT + VDDINT)					
Reset / power down[1]	$I_{leakage}$	—	<30	—	nA
Hibernate[1]	I_{CCH}	—	<1	—	µA
Doze (No CLK_OUT)	I_{CCD}	—	600	—	µA
Idle (No CLK_OUT)	I_{CCI}	—	700	—	µA
Transmit mode (0 dBm nominal output power)	I_{CCT}	—	15	18	mA
Receive mode	I_{CCR}	—	15	18	mA
Input current (VIN = 0 V or VDDINT) (All digital inputs)	IIN	—	—	±1	µA

Table 10. DC electrical characteristics (VBATT, VDDINT = 2.7 V, T_A=25°C, unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Input low voltage (all digital inputs)	VIL	0	—	30% VDDINT	V
Input high voltage (all digital inputs)	VIH	70% VDDINT	—	VDDINT	V
Output high voltage (IOH = -1 mA) (all digital outputs)	VOH	80% VDDINT	—	VDDINT	V
Output low voltage (IOL = 1 mA) (all digital outputs)	VOL	0	—	20% VDDINT	V

[1] To attain specified low power current, all GPIO and other digital IO must be handled properly.

9.2 AC electrical characteristics

Table 11. Receiver AC electrical characteristics
(VBATT, VDDINT=2.7 V, T_A=25 ℃, fref=32 MHz, unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Sensitivity for 1% packet error rate (PER) (–40 to +105 ℃)	SENSper	—	–99	–97	dBm
Sensitivity for 1% packet error rate (PER) (+25 ℃)	SENSper	—	–102		dBm
Saturation (maximum input level)	SENSmax	—	+10	—	dBm
Channel rejection for dual port mode (1% PER and desired signal –82 dBm)					
+5 MHz (adjacent channel)		—	38	—	dB
–5 MHz (adjacent channel)		—	34	—	dB
+10 MHz (alternate channel)		—	47	—	dB
–10 MHz (alternate channel)		—	47	—	dB
>= 15 MHz		—	55	—	dB
Frequency error tolerance		—	—	200	kHz
Symbol rate error tolerance		80	—	—	ppm

Table 12. Transmitter AC electrical characteristics
(VBATT, VDDINT=2.7 V, T_A=25℃, fref=32 MHz, unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Power spectral density[1], absolute limit from –40°C to +105°C		–30	—	—	dBm
Power Spectral Density[2], Relative limit from –40°C to +105°C		–20	—	—	dB
Nominal output power	Pout	–0.5	0	0.5	dBm
Maximum output power		—	10	—	dBm
Error vector magnitude	EVM	—	8	13	%
Output power control range[3]		—	40	—	dB
Over the air data rate		—	250	—	kbps
2nd harmonic[4]		—	<-50	<-40	dBm
3rd harmonic [4]		—	<-50	<-40	dBm

1 [f-fc] > 3.5 MHz, average spectral power is measured in 100 kHz resolution BW.

2 For the relative limit, the reference level is the highest reference power measured within ± 1 MHz of the carrier frequency

3 Measurement is at the package pin on the output of the Tx/Rx switch. It does not degrade more than ±2 dB across temperature and an additional ±1 dB across all processes. Power adjustment will span nominally from –30 dBm to +10 dBm in 21 steps @ 2 dBm / step.

4 Measured with output power set to nominal (0 dBm) and temperature @ 25℃. If trap filter is needed must meet reference board size requirements.

9.2.1 SPI timing: R_SSEL_B to R_SCLK

The following diagram describes timing constraints that must be guaranteed by the system designer.

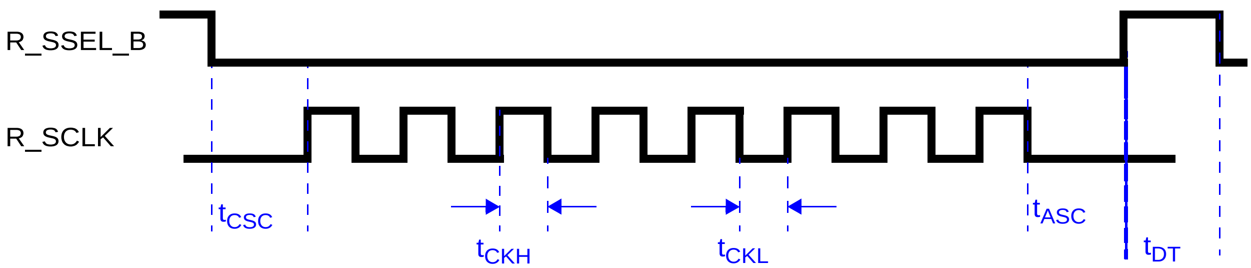


Figure 24. SPI timing: R_SSEL_B to R_SCLK

t_{CSC} (CS-to-SCK delay): 31.25 ns

t_{ASC} (After SCK delay): 31.25 ns

t_{DT} (Minimum CS idle time): 62.5 ns

t_{CKH} (Minimum R_SCLK high time): 31.25 ns (for SPI writes); 55.55 ns (for SPI reads)

t_{CKL} (Minimum R_SCLK low time): 31.25 ns (for SPI writes); 55.55 ns (for SPI reads)

NOTE

The SPI master device deasserts R_SSEL_B only on byte boundaries, and only after guaranteeing the t_{ASC} constraint shown above.

9.2.2 SPI timing: R_SCLK to R_MOSI and R_MISO

The following diagram describes timing constraints that must be guaranteed by the system designer. These constraints apply to the Master SPI (R_MOSI), and are guaranteed by the radio SPI (R_MISO).

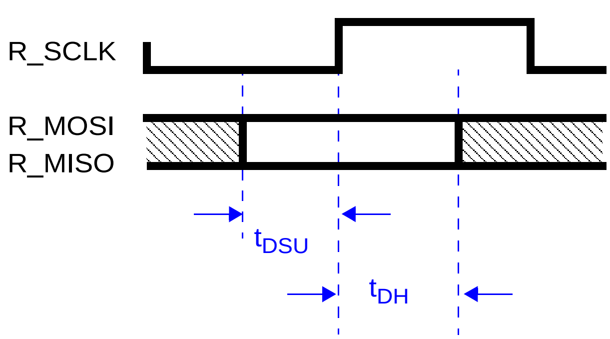


Figure 25. SPI timing: R_SCLK to R_MOSI and R_MISO

t_{DSU} (data-to-SCK setup): 10 ns

t_{DH} (SCK-to-data hold): 10 ns

Table 13. RF port impedance

Characteristic	Symbol	Typ	Unit
RFIN Pins for internal T/R switch configuration, TX mode 2.360 GHz 2.420 GHz 2.480 GHz	Zin	TBD	Ω
RFIN Pins for internal or external T/R switch configuration, RX mode 2.360 GHz 2.420 GHz 2.480 GHz	Zin	TBD	Ω
PAO Pins for external T/R switch configuration, TX mode 2.360 GHz 2.420 GHz 2.480 GHz	Zin	TBD	Ω

10 Crystal oscillator reference frequency

This section provides application specific information regarding crystal oscillator reference design and recommended crystal usage.

10.1 Crystal oscillator design considerations

The IEEE ® 802.15.4 Standard requires that frequency tolerance be kept within ±40 ppm accuracy. This means that a total offset up to 80 ppm between transmitter and receiver will still result in acceptable performance. The MKW22D512V transceiver provides on board crystal trim capacitors to assist in meeting this performance, while the bulk of the crystal load capacitance is external.

10.2 Crystal requirements

The suggested crystal specification for the MKW22D512V is shown in Table 14. A number of the stated parameters are related to desired package, desired temperature range and use of crystal capacitive load trimming.

Table 14. MKW22D512V **crystal specifications**

Parameter	Value	Unit	Condition
Frequency	32	MHz	
Frequency tolerance (cut tolerance)	±10	ppm	at 25℃
Frequency stability (temperature)	±25	ppm	Over desired temperature range
Aging[1]	±2	ppm	max
Equivalent series resistance	60	Ω	max
Load capacitance	5–9	pF	

Table 14. MKW22D512V crystal specifications (continued)

Parameter	Value	Unit	Condition
Shunt capacitance	<2	pF	max
Mode of oscillation			fundamental

[1] A wider aging tolerance may be acceptable if application uses trimming at production final test.

11 Pin assignments

Table 15. MKW22D512V pin assignments (Sheet 1 of 4)

Typical feature	MKW22D 512V (USB)	MKW21D xxxV	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
RADIO	1	1	EXTAL_32M	EXTAL_32M	—	—	—	—	—	—	—	—
RADIO	2	2	GPIO1	GPIO1	—	—	—	—	—	—	—	—
RADIO	3	3	GPIO2	GPIO2	—	—	—	—	—	—	—	—
SPI0	4	4	PTC4/LLWU_P8	DISABLED	—	PTC4/LLWU_P8	SPI0_PCS0	UART1_TX	FTM0_CH3	—	CMP1_OUT	—
SPI0	5	5	PTC5/LLWU_P9	DISABLED	—	PTC5/LLWU_P9	SPI0_SCK	LPTMR0_ALT2	I2S0_RXD0	—	CMP0_OUT	—
SPI0	6	6	PTC6/LLWU_P10	CMP0_IN0	CMP0_IN0	PTC6/LLWU_P10	SPI0_SOUT	PDB0_EXTRG	I2S0_RX_BCLK	—	I2S0_MCLK	—
SPI0	7	7	PTC7	CMP0_IN1	CMP0_IN1	PTC7	SPI0_SIN	USB_SOF_OUT	I2S0_RX_FS	—	—	—
I2C	8	8	PTD1	ADC0_SE5b	ADC0_SE5b	PTD1	SPI0_SCK	UART2_CTS_b	—	—	—	—
I2C	9	9	PTD2/LLWU_P13	DISABLED	—	PTD2/LLWU_P13	SPI0_SOUT	UART2_RX	I2C_SDA	—	—	GPIO4_BSM_DATA
	10	10	PTD3	DISABLED	—	PTD3	SPI0_SIN	UART2_TX	I2C_SCL	—	—	GPIO5_BSM_CLK
UART0	11	11	PTD4/LLWU_P14	mADC0_SE21	mADC0_SE21	PTD4/LLWU_P14	SPI0_PCS1	UART0_RTS_b	FTM0_CH4	—	EWM_IN	GPIO_BSM_FRAME
UART0	12	12	PTD5	ADC0_SE6b	ADC0_SE6b	PTD5	SPI0_PCS2	UART0_CTS_b/UART0_COL_b	FTM0_CH5	—	EWM_OUT_b	—
UART0	13	13	PTD6/LLWU_P15	ADC0_SE7b	ADC0_SE7b	PTD6/LLWU_P15	SPI0_PCS3	UART0_RX	FTM0_CH6	—	FTM0_FLT0	—
UART0	14	14	PTD7	mADC0_SE22	mADC0_SE22	PTD7	CMT_IRO	UART0_TX	FTM0_CH7	—	FTM0_FLT1	—

Table 15. MKW22D512V pin assignments (Sheet 2 of 4)

Typical feature	MKW22D512V (USB)	MKW21DxxxV	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
TRACE,UART1,I2C	15	15	PTE0	mADC0_SE10	mADC0_SE10	PTE0	SPI1_PCS1	UART1_TX	—	mTRACE_CLKOUT	I2C1_SDA	RTC_CLKOUT
TRACE,	16	16	PTE1/LLWU_P0	mADC0_SE11	mADC0_SE11	PTE1/LLWU_P0	SPI1_SOUT	UART1_RX	—	mTRACE_D3	I2C1_SCL	SPI1_SIN
TRACE,	17	17	PTE2/LLWU_P1	mADC0_DP1	mADC0_DP1	PTE2/LLWU_P1	SPI1_SCK	UART1_CTS_b	—	mTRACE_D2	—	—
TRACE,	18	18	PTE3	mADC0_DM1	mADC0_DM1	PTE3	SPI1_SIN	UART1_RTS_b	—	mTRACE_D1	—	SPI1_SOUT
TRACE,	19	19	PTE4/LLWU_P2	DISABLED		PTE4/LLWU_P2	SPI1_PCS0	UART3_TX	—	mTRACE_D0	—	—
—	20	20	VDD_MCU	VDD_MCU	VDD_MCU	—	—	—	—	—	—	—
—	—	21	PTE16	ADC0_SE4a	ADC0_SE4a	PTE16	SPI0_PCS0	UART2_TX	FTM_CLKIN0	—	FTM0_FLT3	—
—	—	22	PTE17	ADC0_SE5a	ADC0_SE5a	PTE17	SPI0_SCK	UART2_RX	FTM_CLKIN1	—	LPTMR0_ALT3	—
—	—	23	PTE18	ADC0_SE6a	ADC0_SE6a	PTE18	SPI0_SOUT	UART2_CTS_b	I2C0_SDA	—	—	—
—	—	24	PTE19	ADC0_SE7a	ADC0_SE7a	PTE19	SPI0_SIN	UART2_RTS_b	I2C0_SCL	—	—	—
USB	21	—	USB0_DP	USB0_DP	USB0_DP	—	—	—	—	—	—	—
USB	22	—	USB0_DM	USB0_DM	USB0_DM	—	—	—	—	—	—	—
USB	23	—	VOUT33	VOUT33	VOUT33	—	—	—	—	—	—	—
USB	24	—	VREGIN	VREGIN	VREGIN	—	—	—	—	—	—	—
Analog Power	25	25	VDDA	VDDA	VDDA	—	—	—	—	—	—	—
Analog Power	26	26	VREFH	VREFH	VREFH	—	—	—	—	—	—	—

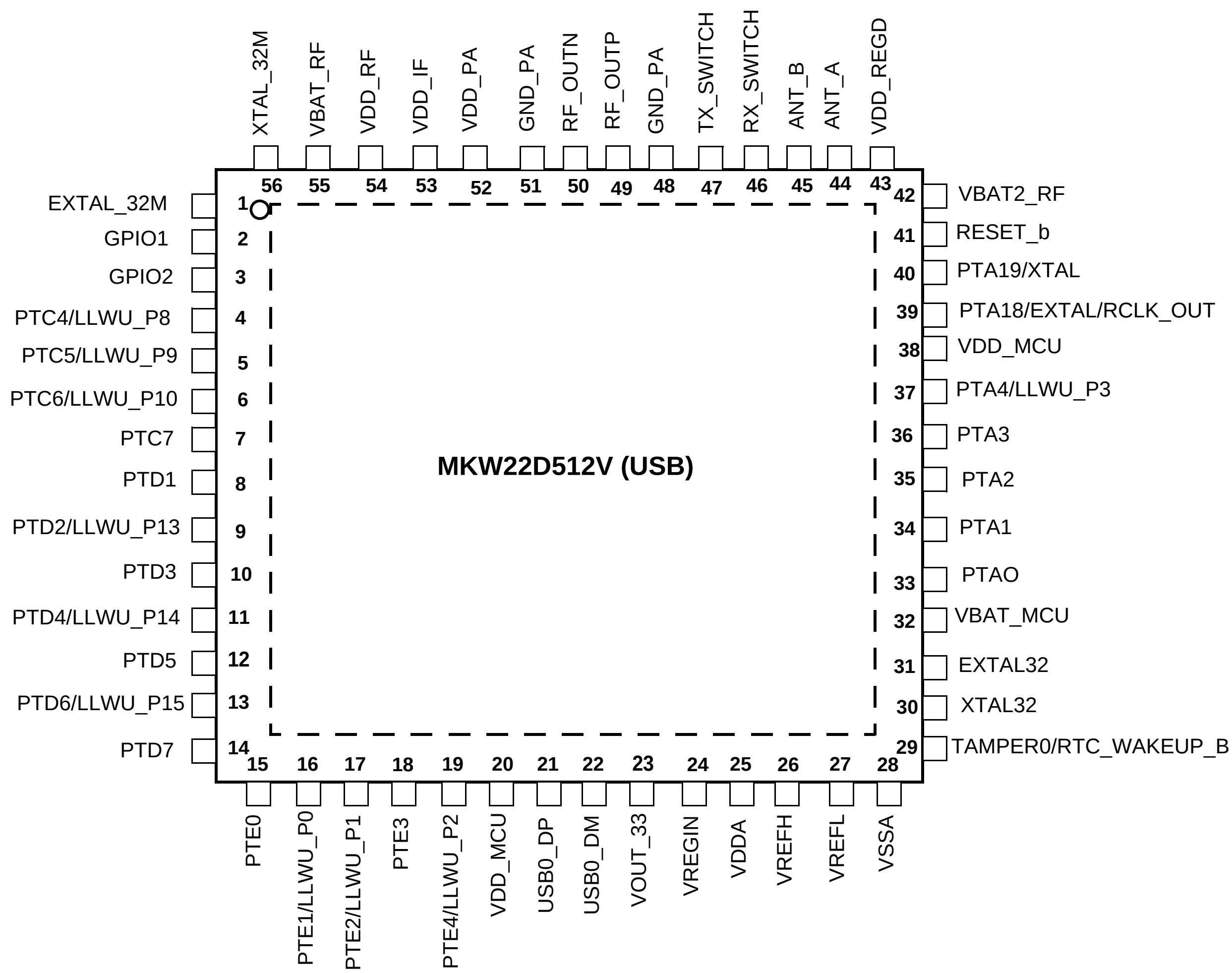
Table 15. MKW22D512V pin assignments (Sheet 3 of 4)

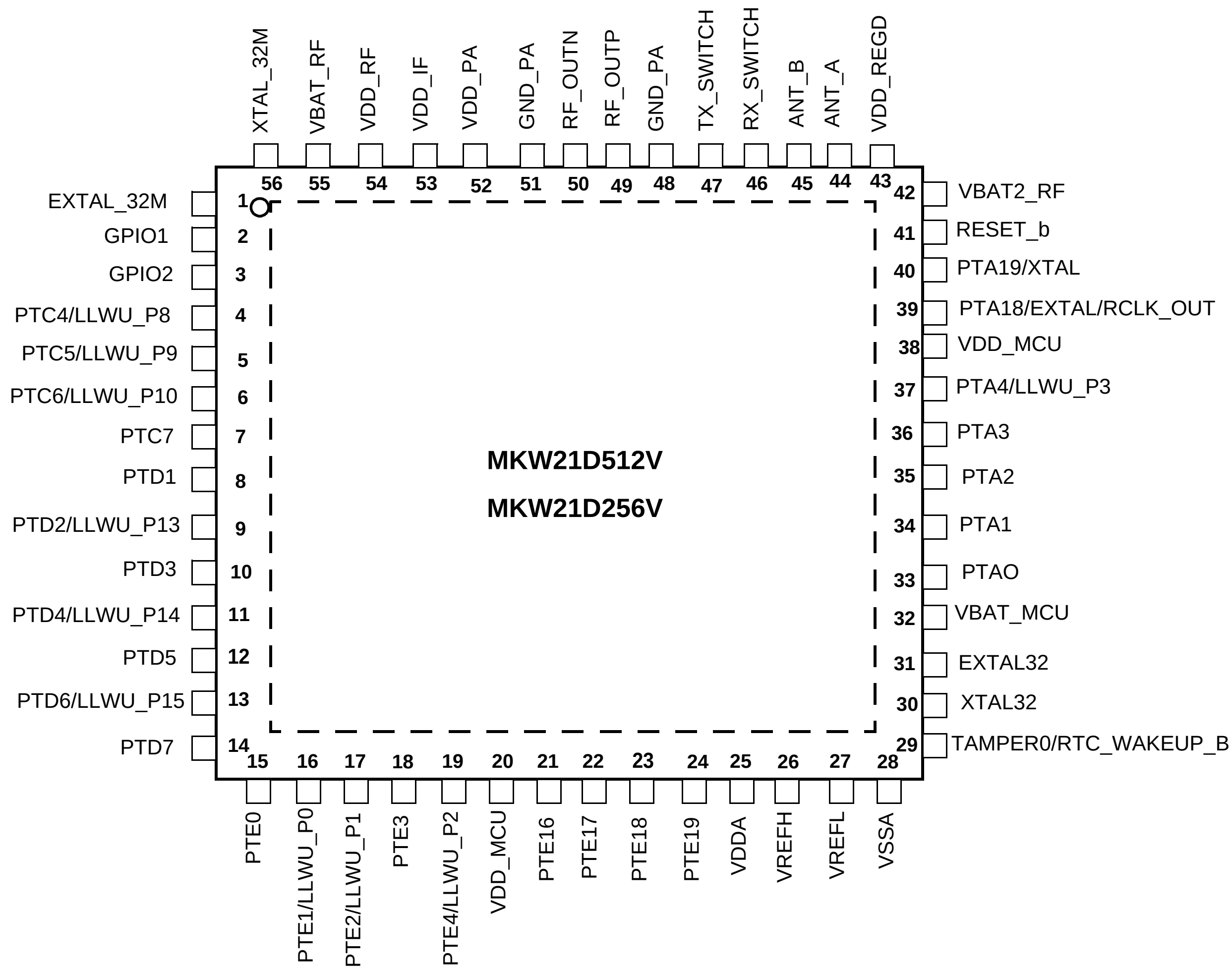
Typical feature	MKW22D 512V (USB)	MKW21D xxxV	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
Analog Power	27	27	VREFL	VREFL	VREFL	—	—	—	—	—	—	—
Analog Power	28	28	VSSA	VSSA	VSSA	—	—	—	—	—	—	—
Tamper	29	29	TAMPER0/ RTC_ WAKEUP_B	TAMPER0/ RTC_ WAKEUP_B	TAMPER0/ RTC_ WAKEUP_B	—	—	—	—	—	—	—
VBAT, 32KHz OSC	30	30	XTAL32	XTAL32	XTAL32	—	—	—	—	—	—	—
VBAT, 32KHz OSC	31	31	EXTAL32	EXTAL32	EXTAL32	—	—	—	—	—	—	—
VBAT, 32KHz OSC	32	32	VBAT_ MCU	VBAT_ MCU	VBAT_ MCU	—	—	—	—	—	—	—
JTAG, Timer	33	33	PTA0	JTAG_ TCLK/ SWD_ CLK/ EZP_ CLK	—	PTA0	UART0 _CTS_ b/ UART0 _COL_ b	FTM0_ CH5	—	—	—	JTAG_ TCLK/ SWD_ CLK
JTAG, Timer	34	34	PTA1	JTAG_ TDI/ EZP_DI	—	PTA1	UART0 _RX	FTM0_ CH6	—	—	—	JTAG_ TDI
JTAG, Timer	35	35	PTA2	JTAG_ TDO/ TRACE _SWO/ EZP_ DO	—	PTA2	UART0 _TX	FTM0_ CH7	—	—	—	JTAG_ TDO/ TRACE _SWO
JTAG, Timer	36	36	PTA3	JTAG_ TMS/ SWD_ DIO	—	PTA3	UART0 _RTS_ b	FTM0_ CH0	—	—	—	JTAG_ TMS/ SWD_ DIO
NMI	37	37	PTA4/ LLWU_ P3	NMI_b/ EZP_ CS_b	—	PTA4/ LLWU_ P3	—	FTM0_ CH1	—	—	—	NMI_b
—	38	38	VDD_ MCU	VDD_ MCU	VDD_ MCU	—	—	—	—	—	—	—
MCU XTAL	39	39	PTA18	EXTAL0	EXTAL0	PTA18	—	FTM0_ FLT2	FTM_ CLKIN0	—	—	—

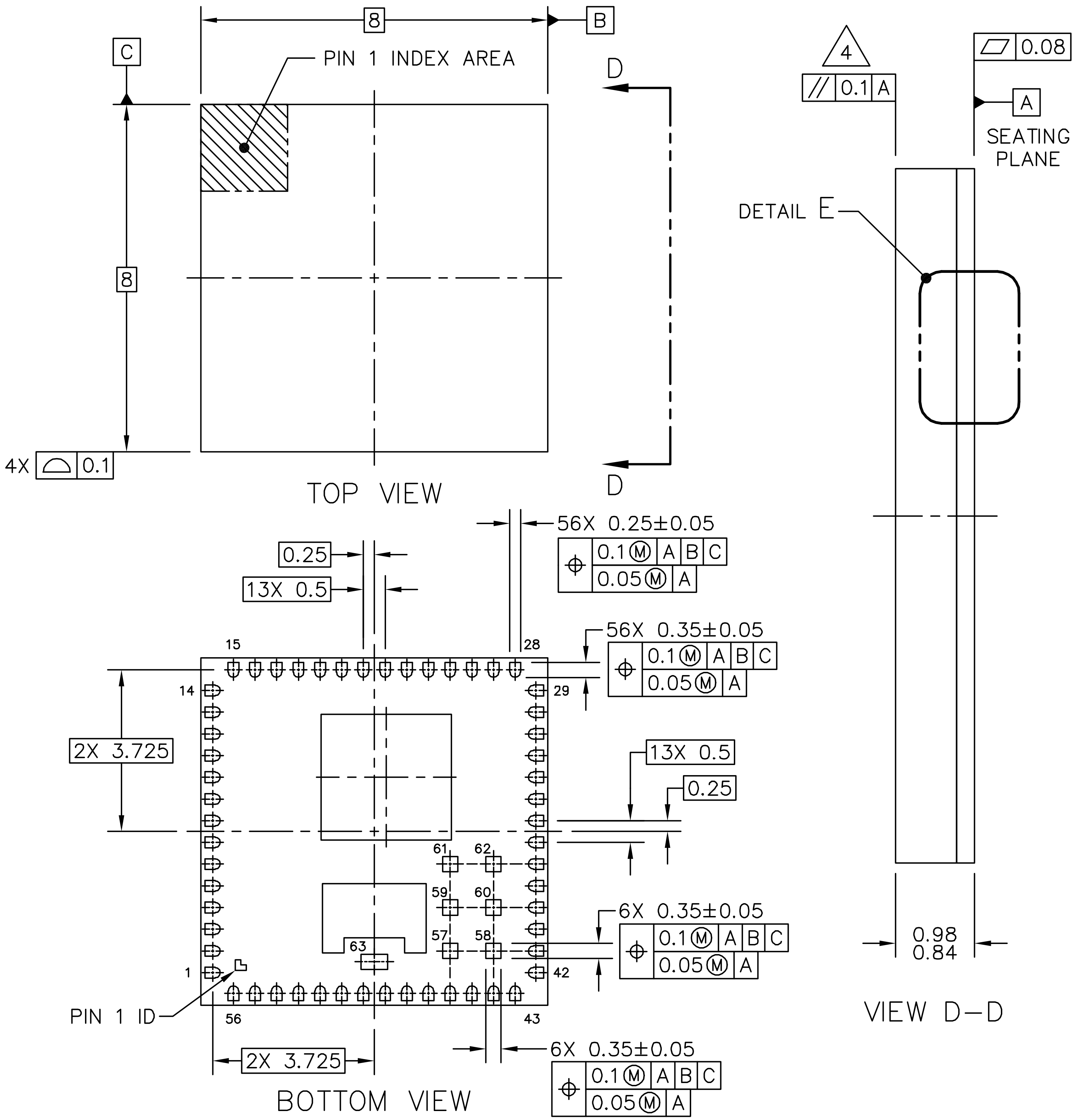
Table 15. MKW22D512V pin assignments (Sheet 4 of 4)

Typical feature	MKW22D 512V (USB)	MKW21D xxxV	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
MCU XTAL	40	40	PTA19	XTAL0	XTAL0	PTA19	—	FTM1_ FLT0	FTM_ CLKIN1	—	LPTMR 0_ALT1	—
RESET	41	41	RESET _b	RESET _b	RESET _b	—	—	—	—	—	—	—
RADIO	42	42	VBAT2 _RF	VBAT3 _RF	—	—	—	—	—	—	—	—
RADIO	43	43	VDD_ REGD	VDD_ REGD	—	—	—	—	—	—	—	—
RADIO	44	44	ANT_A	ANT_A	—	—	—	—	—	—	—	—
RADIO	45	45	ANT_B	ANT_B	—	—	—	—	—	—	—	—
RADIO	46	46	RX_ SWITC H	RX_ SWITC H	—	—	—	—	—	—	—	—
RADIO	47	47	TX_ SWITC H	TX_ SWITC H	—	—	—	—	—	—	—	—
RADIO	48	48	GND_ PA	GND_ PA	—	—	—	—	—	—	—	—
RADIO	49	49	RF_ OUTP	RF_ OUTP	—	—	—	—	—	—	—	—
RADIO	50	50	RF_ OUTN	RF_ OUTN	—	—	—	—	—	—	—	—
RADIO	51	51	GND_ PA	GND_ PA	—	—	—	—	—	—	—	—
RADIO	52	52	VDD_ PA	VDD_ PA	—	—	—	—	—	—	—	—
RADIO	53	53	VDD_IF	VDD_IF	—	—	—	—	—	—	—	—
RADIO	54	54	VDD_ RF	VDD_ RF	—	—	—	—	—	—	—	—
RADIO	55	55	VBAT_ RF	VBAT_ RF	—	—	—	—	—	—	—	—
RADIO	56	56	XTAL_ 32M	XTAL_ 32M	—	—	—	—	—	—	—	—

12 Packaging information




MKW21D512V
MKW21D256V
EXTAL_32M 1
GPIO1 2
GPIO2 3
PTC4/LLWU_P8 4
PTC5/LLWU_P9 5
PTC6/LLWU_P10 6
PTC7 7
PTD1 8
PTD2/LLWU_P13 9
PTD3 10
PTD4/LLWU_P14 11
PTD5 12
PTD6/LLWU_P15 13
PTD7 14
PTE0 15
PTE1/LLWU_P0 16
PTE2/LLWU_P1 17
PTE3 18
PTE4/LLWU_P2 19
VDD_MCU 20
PTE16 21
PTE17 22
PTE18 23
PTE19 24
VDDA 25
VREFH 26
VREFL 27
VSSA 28
TAMPER0/RTC_WAKEUP_B 29
XTAL32 30
EXTAL32 31
VBAT_MCU 32
PTAO 33
PTA1 34
PTA2 35
PTA3 36
PTA4/LLWU_P3 37
VDD_MCU 38
PTA18/EXTAL/RCLK_OUT 39
PTA19/XTAL 40
RESET_b 41
VBAT2_RF 42
VDD_REGD 43
ANT_A 44
ANT_B 45
RX_SWITCH 46
TX_SWITCH 47
GND_PA 48
RF_OUTP 49
RF_OUTN 50
GND_PA 51
VDD_PA 52
VDD_IF 53
VDD_RF 54
VBAT_RF 55
XTAL_32M 56



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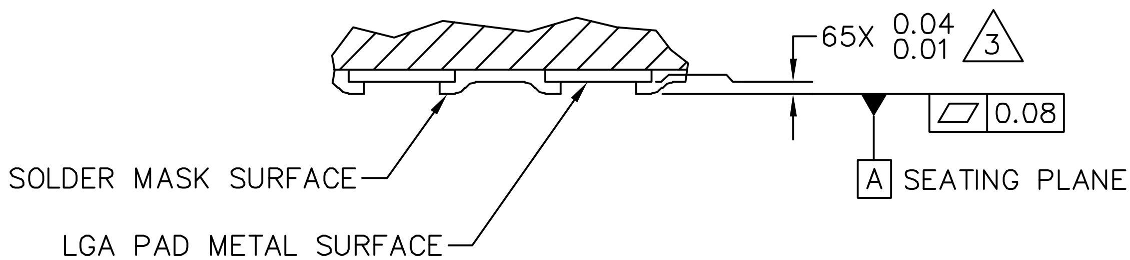
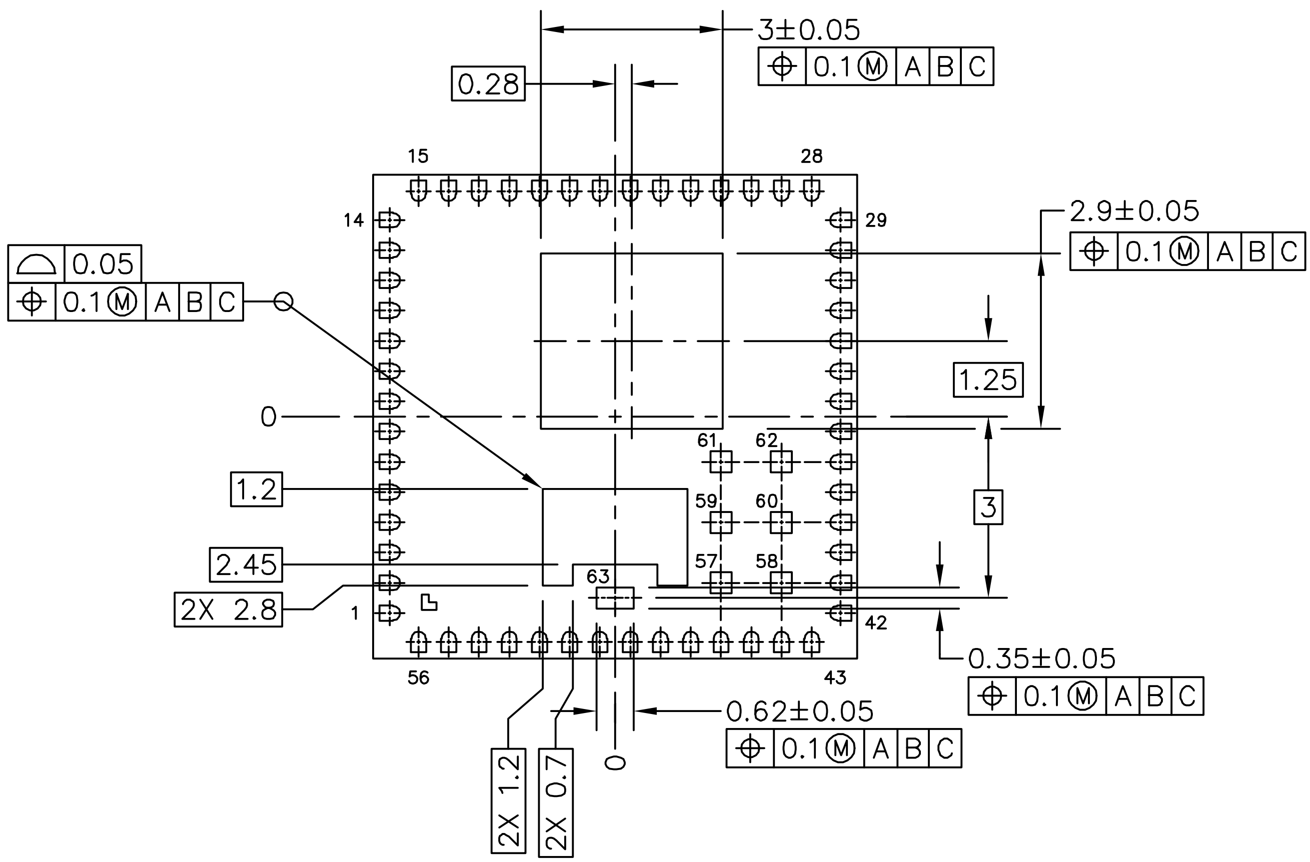
	STANDARD: NON–JEDEC	



DETAIL E
VIEW ROTATED 90° CW



BOTTOM VIEW

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	CASE NUMBER: 2234–01	27 FEB 2012
	STANDARD: NON–JEDEC	

NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.

2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M—1994.

3. DIMENSION APPLIES TO ALL LEADS AND FLAG AREAS.

4. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: MAPLGA, THIN PROFILE, 8 X 8 X 0.91 PKG, 0.5 MM PITCH, 63 I/O	DOCUMENT NO: 98ASA00393D	REV: A
	CASE NUMBER: 2234—01	27 FEB 2012
	STANDARD: NON—JEDEC	