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# RF7234A

## 3V TD-SCDMA LINEAR PA MODULE 1880MHz TO 2025MHz

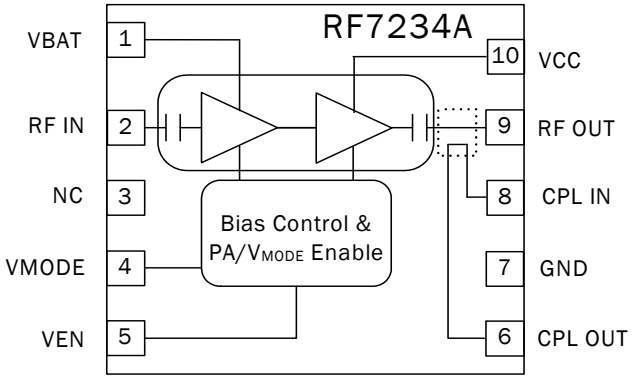
Package Style: Module, 10-Pin, 3mmx3mmx1.0mm

## Features

- TD-SCDMA Compliant
- Low Voltage Positive Bias Supply (3.4V to 4.2V)
- +28dBm Output Power TD-SCDMA
- High Efficiency Operation 37% at $P_{OUT}$=+28dBm (TD-SCDMA)
- Internal Voltage Regulator Eliminates the Need for External Reference Voltage ($V_{REF}$)
- 2-Mode Gain States with Digital Control Interface
- Supports DC/DC Converter Operation
- Integrated Power Coupler
- Integrated Blocking and Collector Decoupling Capacitors

## Applications

- TD-SCDMA Wireless Handsets and Data Cards




Functional Block Diagram

## Product Description

The RF7234A is a high-power, high-efficiency, linear power amplifier designed for use as the final RF amplifier in 3V, 50Ω TD-SCDMA mobile cellular equipment and spread-spectrum systems. This PA is developed for TD-SCDMA 1880MHz to 1920MHz and 2010MHz to 2025MHz frequency band. The RF7234A has a digital control pin to select one of two gain modes to optimize performance at lower power levels. The part also has an integrated directional coupler which eliminates the need for an external discrete coupler at the output. The RF7234A is fully TD-SCDMA-compliant and is assembled in a 10-pin, 3mmx3mm module.

### Ordering Information

| | |
|---|---|
| RF7234A | 3V TD-SCDMA Linear PA Module 1880MHz to 2025MHz |
| RF7234APCBA-410 | Fully Assembled Evaluation Board |

### Optimum Technology Matching® Applied

| | | | |
|---|---|---|---|
| ☐ GaAs HBT | ☐ SiGe BiCMOS | ☐ GaAs pHEMT | ☐ GaN HEMT |
| ☐ GaAs MESFET | ☑ Si BiCMOS | ☐ Si CMOS | ☐ RF MEMS |
| ☑ InGaP HBT | ☐ SiGe HBT | ☐ Si BJT | ☐ LDMOS |





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## Absolute Maximum Ratings

| Parameter | Rating | Unit |
|---|---|---|
| Supply Voltage in Standby Mode | 5.5 | V |
| Supply Voltage in Idle Mode | 5.5 | V |
| Supply Voltage in Operating Mode, 50Ω Load | 5.5 | V |
| Supply Voltage, $V_{BAT}$ | 5.5 | V |
| Control Voltage, VMODE | 5.5 | V |
| Control Voltage, $V_{EN}$ | 5.5 | V |
| RF - Input Power | +10 | dBm |
| RF - Output Power | +30 | dBm |
| Output Load VSWR (Ruggedness) | 10:1 | |
| Operating Ambient Temperature | -30 to +110 | °C |
| Storage Temperature | -55 to +150 | °C |

**Caution!** ESD sensitive device.

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability. Specified typical performance or functional operation of the device under Absolute Maximum Rating conditions is not implied.

RoHS status based on EUDirective2002/95/EC (at time of this document revision).



| Parameter | Specification | | | Unit | Condition |
|---|---|---|---|---|---|
| | Min. | Typ. | Max. | | |
| **Recommended Operating Conditions** | | | | | T=25°C, $V_{CC}$=$V_{BATT}$=3.4V, $V_{EN}$=1.8V, 50Ω, TD-SCDMA Modulation, unless otherwise specified. |
| Operating Frequency Range | 1880 | | 1920 | MHz | TD-SCDMA |
| | 2010 | | 2025 | Hz | TD-SCDMA |
| $V_{BAT}$ | +3.0[1] | +3.4 | +4.2 | V | |
| $V_{CC}$ | +0.5[1] | +3.4 | +4.2 | V | |
| $V_{EN}$ | 0 | | 0.5 | V | PA disabled. |
| | 1.35 | 1.8 | 3.10 | V | PA enabled. |
| $V_{MODE}$ | 0 | | 0.5 | V | Logic “low”. |
| | 1.35 | 1.8 | 3.10 | V | Logic “high”. |
| $P_{OUT}$ | | | | | |
| Maximum Linear Output (HGM) | 28.0[2] | | | dBm | High Gain Mode (HGM) TD-SCDMA |
| Maximum Linear Output (LGM) | 16.0[2] | | | dBm | Low Gain Mode (LGM) |
| Ambient Temperature | -25 | +25 | +85 | °C | |

Notes:
[1]Minimum $V_{CC}$ for max $P_{OUT}$ is indicated. $V_{CC}$ down to 0.5V may be used for backed-off power when using DC/DC converter to conserve battery current.
[2]For operation at below $V_{CC}$=3.4V, derate $P_{OUT}$ by 1.0dB.


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| Parameter | Specification | | | Unit | Condition |
|---|---|---|---|---|---|
| | Min. | Typ. | Max. | | |
| **Electrical Specifications - TD-SCDMA** | | | | | T=+25°C, $V_{CC}$=$V_{BAT}$=+3.4V, $V_{EN}$=+1.8V, 50Ω, TD-SCDMA modulation unless otherwise specified. |
| Gain | 26 | 28 | | dB | HGM, $P_{OUT}$=28dBm |
| | 11[1] | 14.5 | | dB | LGM, $P_{OUT}$≤16dBm |
| Gain Linearity | | ±0.2 | | dB | HGM, 16.0dBm≤$P_{OUT}$≤28dBm |
| ACLR - 1.6MHz Offset | | -40 | | dBc | HGM, $P_{OUT}$=28dBm |
| | | -40 | | dBc | LGM, $P_{OUT}$=16dBm |
| ACLR - 3.2MHz Offset | -54 | -56 | | dBc | HGM, $P_{OUT}$=28dBm |
| | | -58 | | dBc | LGM, $P_{OUT}$=16dBm |
| PAE Without DC/DC Converter | | 37 | | % | HGM, $P_{OUT}$=28dBm |
| | | 8 | | % | LGM, $P_{OUT}$=16dBm |
| Current Drain | | 500 | | mA | HBM, $P_{OUT}$=28dBm (during active timeslot) |
| | | 140 | | mA | LGM, $P_{OUT}$=16dBm (during active timeslot) |
| Quiescent Current | | 95 | | mA | HGM, DC only |
| Enable Current | | 0.1 | 1.0 | mA | Source or sink current. $V_{EN}$=1.8V. |
| Mode Current ($I_{MODE0}$) | | 0.1 | 1.0 | mA | Source or sink current. $V_{MODE}$=1.8V. |
| Leakage Current | | 1.0 | 10.0 | µA | DC only. $V_{EN}$=$V_{MODE}$=0.5V. |
| Noise Power in Receive Band | | -140 | | dBm/Hz | Measured in DCS and alternate TDSCDMA 33/34 |
| Input Impedance | | 1.8:1 | | VSWR | No ext. matching, $P_{OUT}$≤28dBm, all modes. |
| Harmonic, 2FO | | -13 | | dBm | $P_{OUT}$≤28dBm, HGM. TDSCDMA |
| Harmonic, 3FO | | -30 | | dBm | $P_{OUT}$≤28dBm, HGM. |
| SEM Margin | | 5 | | dB | $P_{OUT}$=28dBm, HGM |
| Spurious Output Level | | | -70 | dBc | All spurious, $P_{OUT}$≤28dBm, all conditions, load VSWR≤6:1, all phase angles. |
| Insertion Phase Shift | -30 | | +30 | ° | Phase shift at 16dBm when switching from HGM to LGM at 16dBm. |
| DC Enable Time | | | 10 | µS | DC only. Time from $V_{EN}$=high to stable idle current (90% of steady state value). |
| RF Rise/Fall Time | | | 6 | µS | $P_{OUT}$≤28dBm, all modes. 90% of target, DC settled prior to RF. |
| Coupling Factor | | -20 | | dB | $P_{OUT}$≤28dBm, all modes. |
| Coupling Accuracy - Temp/Voltage | | ±0.5 | | dB | $P_{OUT}$≤28dBm, all modes. -25°C≤T≤85°C. |
| Coupling Accuracy - VSWR | | ±0.25 | | dB | $P_{OUT}$≤28dBm, all modes, load VSWR=2:1. |
| EVM | | 1.8 | | % | $P_{OUT}$=28dBm, $V_{CC}$=3.4V |

Note: [1]Excludes DC/DC converter operation. Gain may be lower when using DC/DC converter to conserve battery current.


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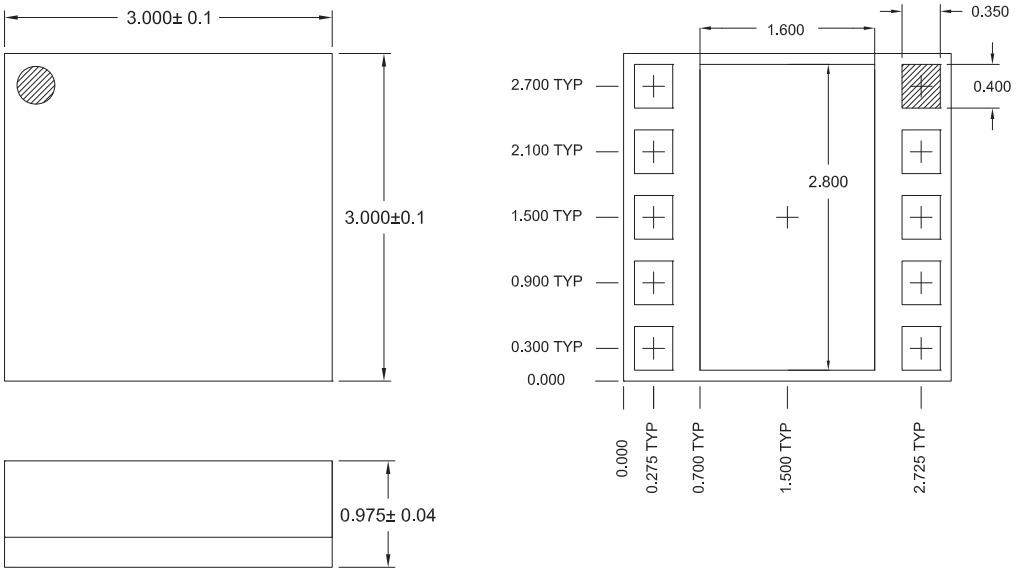
| Pin | Function | Description |
|---|---|---|
| 1 | VBAT | Supply voltage for bias circuitry and the first stage amplifier. |
| 2 | RF IN | RF input internally matched to 50Ω and DC blocked. |
| 3 | NC | Not connected. |
| 4 | VMODE | Digital control input for gain mode selection (see Operating Modes truth table). |
| 5 | VEN | Digital control input for PA enable and disable (see Operating Modes truth table). |
| 6 | CPL_OUT | Coupler output. |
| 7 | GND | This pin must be grounded. |
| 8 | CPL_IN | Coupler input used for cascading couplers in series. Terminate this pin with a 50Ω resistor if not connected to another coupler. |
| 9 | RF OUT | RF output internally matched to 50Ω and DC blocked. |
| 10 | VCC | Supply voltage for the second stage amplifier which can be connected to battery supply or output of DC-DC converter. |
| Pkg Base | GND | Ground connection. The package backside should be soldered to a topside ground pad connecting to the PCB ground plane with multiple ground vias. The pad should have a low thermal resistance and low electrical impedance to the ground plane. |

| $V_{EN}$ | $V_{MODE1}$ | $V_{BAT}$ | $V_{CC}$ | Conditions/Comments |
|---|---|---|---|---|
| Low | Low | 3.0V to 4.2V | 3.0V to 4.2V | Power down mode |
| Low | X | 3.0V to 4.2V | 3.0V to 4.2V | Standby Mode |
| High | Low | 3.0V to 4.2V | 3.0V to 4.2V | High gain mode |
| High | High | 3.0V to 4.2V | 3.0V to 4.2V | Low gain mode |
| High | High | 3.0V to 4.2V | ≥0.5V | Optional lower $V_{CC}$ in low gain mode |

## Package Drawing




NOTES:
1. SHADED AREAS REPRESENT PIN 1 LOCATION.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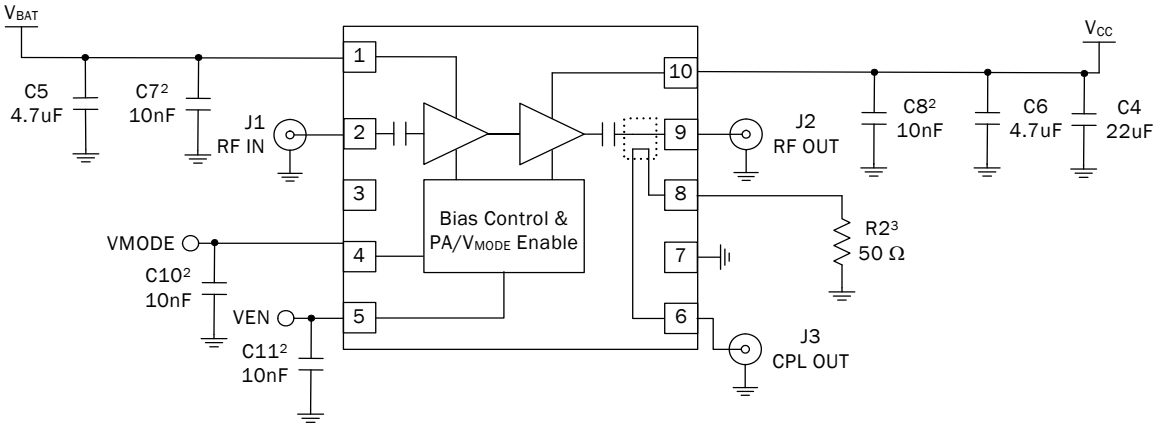
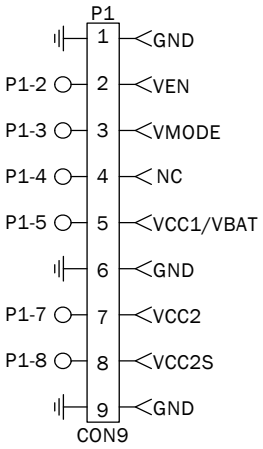
## Preliminary Application Schematic




**NOTES:**
1 VCC and VBAT are connected together if DC-DC converter is not used.
2 Place these capacitors as close to PA as possible.
3 50 Ω resistor will be removed if pin 8 is connected to another coupler.



## PCB Design Requirements

### PCB Surface Finish

The PCB surface finish used for RFMD's qualification process is electroless nickel, immersion gold. Typical thickness is 3μinch to 8μinch gold over 180μinch nickel.

### PCB Land Pattern Recommendation

PCB land patterns for RFMD components are based on IPC-7351 standards and RFMD empirical data. The pad pattern shown has been developed and tested for optimized assembly at RFMD. The PCB land pattern has been developed to accommodate lead and package tolerances. Since surface mount processes vary from company to company, careful process development is recommended.

### PCB Metal Land Pattern

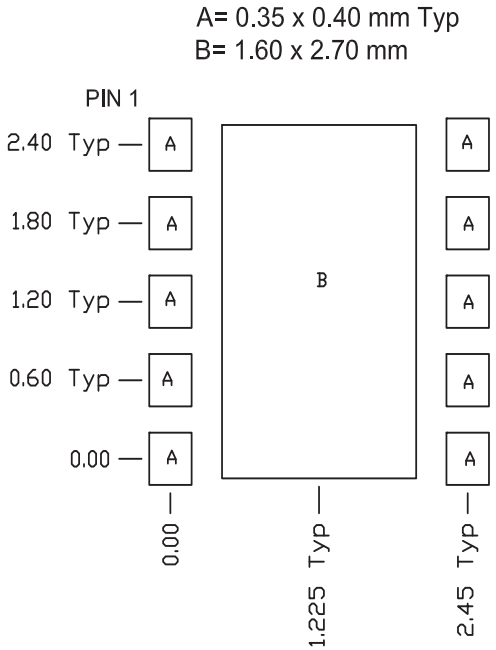



Figure 1. PCB Metal Land Pattern (Top View)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### PCB Solder Mask Pattern

Liquid Photo-Imageable (LPI) solder mask is recommended. The solder mask footprint will match what is shown for the PCB metal land pattern with a 2mil to 3mil expansion to accommodate solder mask registration clearance around all pads. The center-grounding pad shall also have a solder mask clearance. Expansion of the pads to create solder mask clearance can be provided in the master data or requested from the PCB fabrication supplier.

A= 0.45 x 0.50 mm Typ
B= 1.70 x 2.80 mm

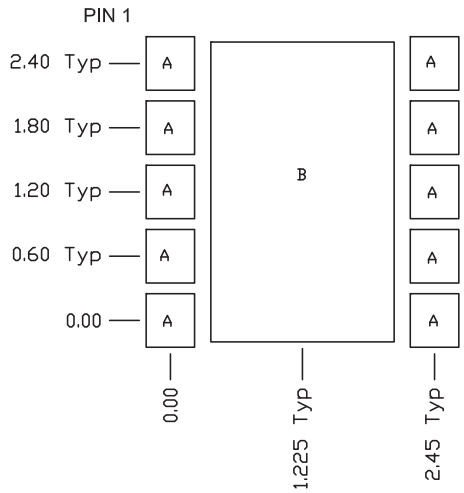


**Figure 2. PCB Solder Mask Pattern (Top View)**

### Thermal Pad and Via Design

The PCB land pattern has been designed with a thermal pad that matches the die paddle size on the bottom of the device.

Thermal vias are required in the PCB layout to effectively conduct heat away from the package. The via pattern has been designed to address thermal, power dissipation and electrical requirements of the device as well as accommodating routing strategies.

The via pattern used for the RFMD qualification is based on thru-hole vias with 0.203mm to 0.330mm finished hole size on a 0.5mm to 1.2mm grid pattern with 0.025mm plating on via walls. If micro vias are used in a design, it is suggested that the quantity of vias be increased by a 4:1 ratio to achieve similar results.

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