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FPD7612P70

LOW NOISE HIGH FREQUENCY PACKAGED pHEMT

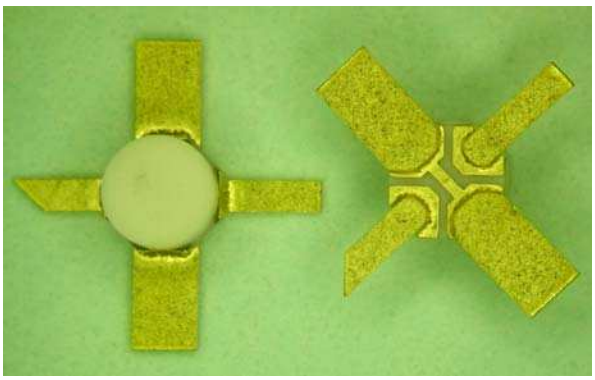
Package: P70

Product Description

The FPD7612P70 is a low parasitic, surface mountable packaged depletion mode pseudomorphic High Electron Mobility Transistor (pHEMT) optimized for low noise, high frequency applications.

Optimum Technology Matching® Applied

- ☐ GaAs HBT
- ☐ GaAs MESFET
- ☐ InGaP HBT
- ☐ SiGe BiCMOS
- ☐ Si BiCMOS
- ☐ SiGe HBT
- ✓ GaAs pHEMT
- ☐ Si CMOS
- ☐ Si BJT
- ☐ GaN HEMT
- ☐ InP HBT
- ☐ RF MEMS
- ☐ LDMOS



Features

- 22dBm Output Power (P1dB)
- 21dB Gain at 1.85GHz
- 0.5dB Noise Figure at 1.85GHz
- 30dB Output IP_3 at 1.85GHz
- 45% Power-Added Efficiency at 1.85GHz
- Usable Gain to 24GHz

Applications

- Gain blocks and medium power stages
- WiMax (2GHz to 11GHz)
- WLAN 802.11a (5.8GHz)
- Point-to-Point Radio (to 18GHz)

RF Parameter	Typical Performance			Unit	Condition
	Min.	Typ.	Max.		
P_{1dB} at Gain Compression		20		dBm	V_{DS}=5V, I_{DS}=30mA
Small-Signal Gain (SSG)	19	21		dB	V_{DS}=5V, I_{DS}=30mA
PAE		45		%	V_{DS}=5V, I_{DS}=30mA, P_{OUT}=P_{1dB}
Maximum Stable Gain (|S21/S12|)		14			V_{DS}=5V, I_{DS}=30mA, f=12GHz
		10			V_{DS}=5V, I_{DS}=30mA, f=18GHz
Noise Figure (NF)		0.5		dB	V_{DS}=5V, I_{DS}=15mA
OIP_3		30		dBm	V_{DS}=5V, I_{DS}=30mA, P_{OUT}=10dBm SCL
Saturated Drain-Source Current (I_{DSS})	45	60	75	mA	V_{DS}=1.3V, V_{GS}=0V
Maximum Drain-Source Current (I_{MAX})		120		mA	V_{DS}=1.3V, V_{GS}=+1V
Transconductance (GM)		80		ms	V_{DS}=1.3V, V_{GS}=0V
Gate-Source Leakage Current (I_{GSO})		1	10	µA	V_{GS}=-5V
Pinch-Off Voltage (V_P)	|0.7|	|0.9|	|1.3|	V	V_{DS}=1.3V, I_{DS}=0.2mA
Gate-Source Breakdown Voltage (V_{BDGS})	|12|	|14|		V	I_{GS}=0.2mA
Gate-Drain Breakdown Voltage (V_{BDGD})	|14.5|	|16|		V	I_{DS}=0.2mA
Thermal Resistivity (θJC) *		335		°C/W	

*Note: $T_{AMBIENT}$=22°C, RF specification measured at f=1.85GHz using CW signal (except as noted).

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Absolute Maximum Ratings[1]

Parameter	Rating	Unit
Drain-Source Voltage (V_{DS}) ($-3V<V_{GS}<-0.5V$)	8	V
Gate-Source Voltage (V_{GS}) ($0V<V_{DS}<+8V$)	-3	V
Drain-Source Current (I_{DS}) (For $V_{DS}<2V$)	I_{DSS}	
Gate Current (I_G) (Forward or reverse)	5	mA
RF Input Power (P_{IN})[2] (Under any acceptable bias state)	16	dBm
Channel Operating Temperature (T_{CH}) (Under any acceptable bias state)	175	°C
Storage Temperature (T_{STG}) (Non-Operating Storage)	-40 to 150	°C
Total Power Dissipation (P_{TOT})[3, 4, 5]	450	mW
Simultaneous Combination of Limits[6] (2 or more max. limits)	80	%

Notes:
[1] $T_{AMBIENT}$ = 22 °C unless otherwise noted; exceeding any one of these absolute maximum ratings may cause permanent damage to the device.
[2] Max. RF input limit must be further limited if input VSWR > 2.5:1.
[3] Users should avoid exceeding 80% of 2 or more Limits simultaneously.
[4] Total Power Dissipation (P_{TOT}) defined as $(P_{DC}+P_{IN})-P_{OUT}$, where P_{DC}: DC Bias Power, P_{IN}: RF Input Power, P_{OUT}: RF Output Power.
Total Power Dissipation to be de-rated as follows above 22 °C:
$P_{TOT}=0.45-(1/R\theta JC)xT_{PACK}$, where T_{PACK} = source tab lead temperature above 22 °C.
Example: For a 65°C carrier temperature: $P_{TOT}=470mW-(3x(65-22))=321mW$

Caution! ESD sensitive device.

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability. Specified typical performance or functional operation of the device under Absolute Maximum Rating conditions is not implied.

RoHS status based on EUDirective2002/95/EC (at time of this document revision).

Biasing Guidelines

Active bias circuits provide good performance stabilization over variations of operating temperature, but require a larger number of components compared to self-bias or dual-biased. Such circuits should include provisions to ensure that gate bias is applied before drain bias, otherwise the pHEMT may be induced to self-oscillate.

Dual-bias circuits are relatively simple to implement, but will require a regulated negative voltage supply for depletion-mode devices such as the FPD7612P70.

For standard Class A operation, a 50% of I_{DSS} bias point is recommended. A small amount of RF gain expansion prior to the onset of compression is normal for this operating point. Class AB of 25% to 33% of I_{DSS} offers an optimized solution for NF and OIP_3.

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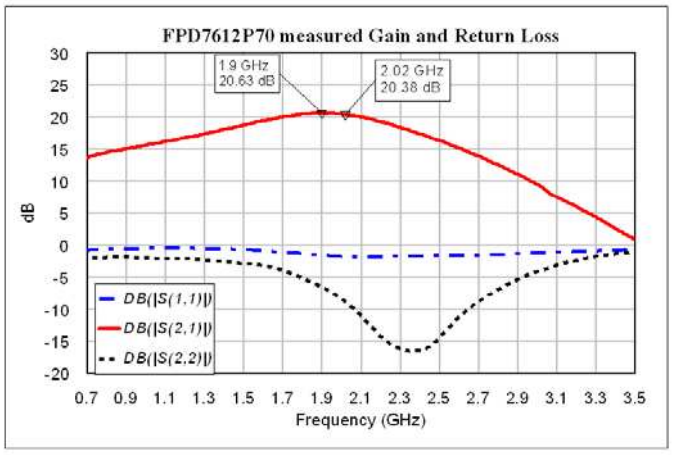
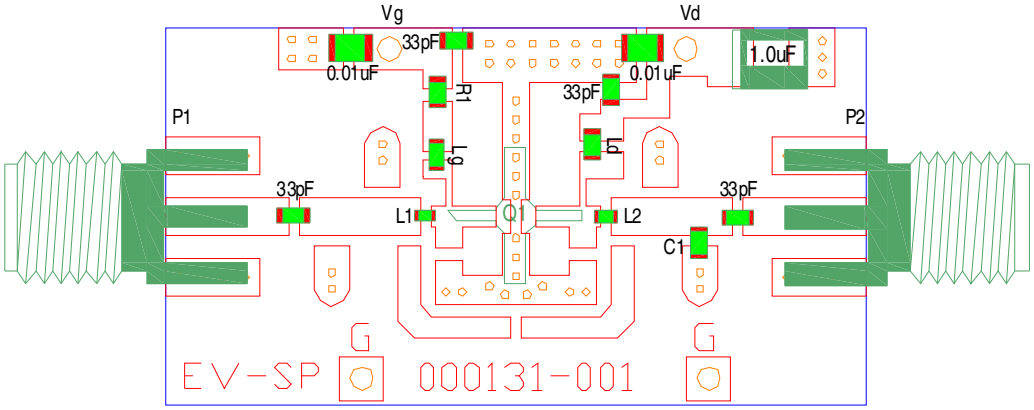
Reference Design (2.0GHz)

Parameter	Typ at 1.90GHz	Typ at 1.96GHz	Typ at 2.02GHz	Unit	Bias
Gain	20.6	20.5	20.4	dB	V_D=3V, I_D=30mA
P1dB	15.0	14.8	14.8	dBm	
OIP3[1]	27.5	27.5	28.0	dBm	
NF	0.65	0.58	0.65	dB	
Gain	20.0	19.7	20.4	dB	V_D=5V, I_D=30mA
P1dB	17.5	17.8	18.0	dBm	
OIP3[1]	27.0	27.0	27.1	dBm	
NF	0.67	0.60	0.65	dB	

[1]OIP3 measured at POUT of 2dBm per tone with spacing=5MHz.



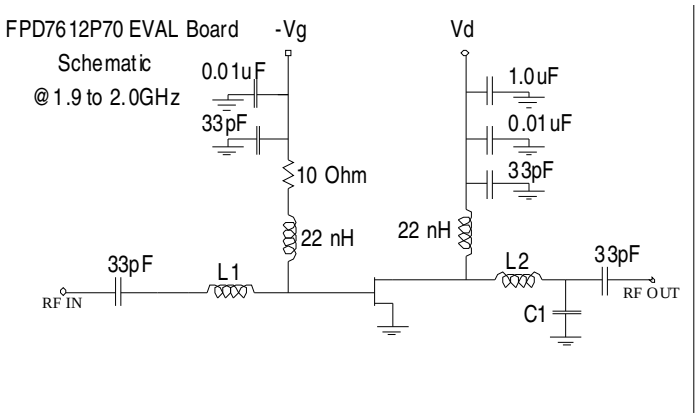
Evaluation Board Layout



Component Values

Component	Value	Description
Lg, Ld	22nH	LL 1608FSL Toko chip inductor
L1	4.7nH	LL 1005FHL Toko chip inductor
L2	3.9nH	LL 1005FHL Toko chip inductor
C1	0.5pF	ATC 600S chip capacitor
33pFx4	33pF	ATC 600S chip capacitor
0.01µFx4	0.01µF	ATC 0805X7R chip capacitor
1.0µF	1.0µF	B-Case Tantallum chip capacitor
R1	10Ω	0603 size chip resistor (100mW)
P1, P2		PCB Edge mount RF connector

Evaluation board material: 31mil thick Rogers 4003 with 1/2oz. Cu on both sides.



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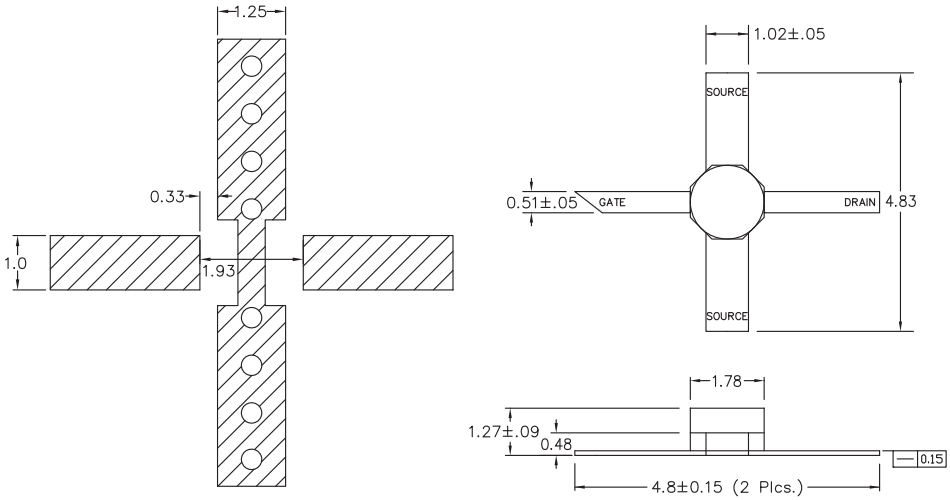
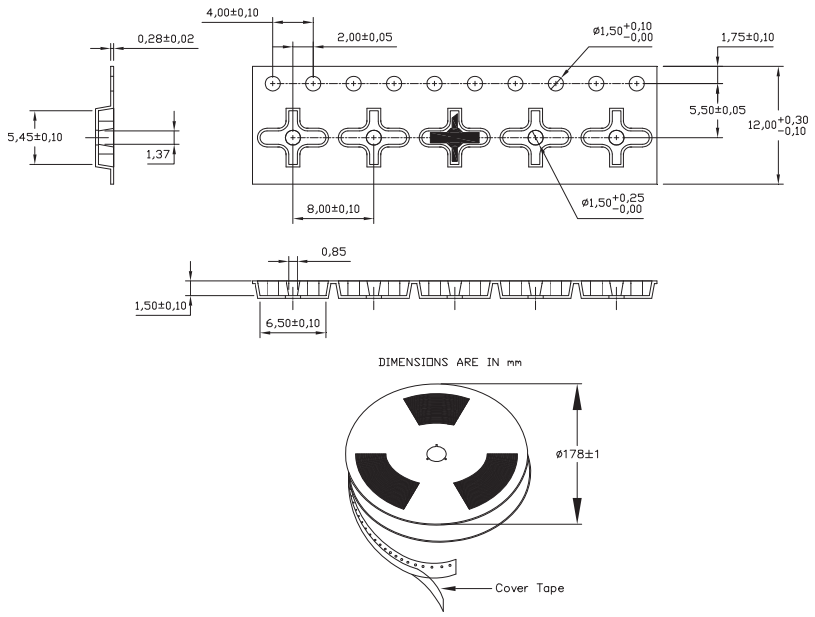
P70 Package Outline and Recommended PC Board Layout

Dimensions in millimeters



Tape and Reel Dimensions and Part Orientation

Tape and reel information on this material is in accordance with EIA-481-1 except where exceptions are identified.



PACKAGE MARKING CODE

Example:
ABC

A=product type
B=week code
C=year code
Reel:

Terminal tape=40mm (min)
Leader tape with empty cavities=350mm (min)
Trailer tape with empty cavities=160mm (min)
Devices per reel=1000

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Preferred Assembly Instructions

This package is compatible with both lead free and leaded solder reflow processes as defined within IPC/JEDEC J-STD-020C. The maximum package temperature should not exceed 260 °C. Package leads are gold plated.

Handling Precautions

To avoid damage to the devices, care should be exercised during handling. Proper Electrostatic Discharge (ESD) precautions should be observed at all stages of storage, handling, assembly, and testing. storage, handling, assembly, and testing.

ESD Rating

These devices should be treated as Class 0 (0V to 250V) using the human body model as defined in JEDEC Standard No. 22-A114. Further information on ESD control measures can be found in MIL-STD-1686 and MIL-HDBK-263.

MSL Rating

The device has an MSL rating of Level 1. To determine this rating, preconditioning was performed to the device per the Pb-free solder profile defined within IPC/JEDEC J-STD-020C, moisture / reflow sensitivity classification for non-hermetic solid state surface mount devices.

Application Notes and Design Data

Application Notes and design data including S-parameters, noise parameters, and device model are available on request and from www.rfmd.com.

Reliability

An MTTF of 4.2 million hours at a channel temperature of 150 °C is achieved for the process used to manufacture this device.

Disclaimers

This product is not designed for use in any space-based or life-sustaining/supporting equipment.

Ordering Information

Description	Ordering Code
RoHS-Compliant Packaged pHEMT	FPD7612P70
2.0GHz Evaluation Board	EB7612P70-AC

Quantity	Ordering Code
Reel of 1000	FPD7612P70
Reel of 100	FPD7612P70SR
Bag of 25	FPD7612P70SQ
Bag of 5	FPD7612P70SB

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