RFHA1042

225MHz TO 450MHz 125W GaN POWER AMPLIFIER

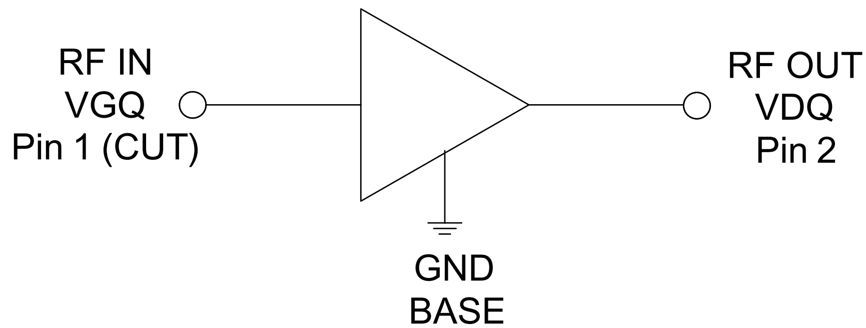
Package: Flanged Ceramic, 2-Pin, RF400-2

Features

- Advanced GaN HEMT Technology
- Peak Power 125W Wideband
- Single Circuit for 225 - 450MHz
- 48V Modulated Typical Performance
  - P_{OUT} 45.2dBm
  - Gain 18.5dB
  - Drain Efficiency 42%
  - ACP -26dBc
- 48V CW Typical Broadband Performance
  - P_{OUT} 51.4dBm
  - Gain 16dB
  - Drain Efficiency 60%
- -40°C to 85°C Operating Temperature
- Optimized for Video Bandwidth and Minimized Memory Effects
- Large Signal Models Available

Applications

- Military Communications
- Commercial Wireless Infrastructure
- General Purpose UHF Amplifiers
- Public Mobile Radios



Functional Block Diagram

Product Description

The RFHA1042 is optimized for military communications, commercial wireless infrastructure and general purpose applications in the 225MHz to 450MHz frequency band. Using an advanced 48V high power density Gallium Nitride (GaN) semiconductor process optimized for high peak to average ratio applications, these high-performance amplifiers achieve 125W power with high efficiency and flat gain over a broad frequency range in a single amplifier design. The RFHA1042 is an input matched GaN transistor packaged in an air cavity ceramic package which provides excellent thermal stability. Ease of integration is accomplished through the incorporation of simple, optimized matching networks external to the package that provide wideband gain, efficiency, and linearizable performance in a single amplifier.

Ordering Information

RFHA1042	225-450MHz, 125W GaN Power Amplifier
RFHA1042PCBA-410	225-450MHz, Fully Assembled Evaluation Board

Optimum Technology Matching® Applied

☐ GaAs HBT	☐ SiGe BiCMOS	☐ GaAs pHEMT	☑ GaN HEMT
☐ GaAs MESFET	☐ Si BiCMOS	☐ Si CMOS	☐ BiFET HBT
☐ InGaP HBT	☐ SiGe HBT	☐ Si BJT	

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Absolute Maximum Ratings

Parameter	Rating	Unit
Drain Voltage (V_D)	150	V
Gate Voltage (V_G)	-8 to 2	V
Gate Current (I_G)	105	mA
Ruggedness (VSWR)	10:1	
Storage Temperature Range	-55 to +125	°C
Operating Temperature Range (T_L)	-40 to +85	°C
Operating Junction Temperature (T_J)	250	°C
Human Body Model	Class 1A	
MTTF (T_J < 200°C, 95% Confidence Limits)*	1.8E + 07	Hours
MTTF (T_J < 250°C, 95% Confidence Limits)*	1.1E + 05	Hours
Thermal Resistance, Rth (junction to case) measured at T_C = 85°C, DC bias only	1.4	°C/W
Thermal Resistance, Rth (junction to case) measured at T_C = 85°C, CW	1.27	°C/W

* MTTF - median time to failure for wear-out failure mode (30% I_{DSS} degradation) which is determined by the technology process reliability. Refer to product qualification report for FIT(random) failure rate.
Operation of this device beyond any one of these limits may cause permanent damage. For reliable continuous operation, the device voltage and current must not exceed the maximum operating values.
Bias Conditions should also satisfy the following expression: $P_{DISS} < (T_J - T_C)/R_{TH}$ J - C and $T_C = T_{CASE}$

Caution! ESD sensitive device.

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability. Specified typical performance or functional operation of the device under Absolute Maximum Rating conditions is not implied.

RFMD Green: RoHS compliant per EU Directive 2002/95/EC, halogen free per IEC 61249-2-21, < 1000ppm each of antimony trioxide in polymeric materials and red phosphorus as a flame retardant, and <2% antimony in solder.

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Recommended Operating Conditions					
Drain Voltage (V_{DSQ})		48		V	
Gate Voltage (V_{GSQ})	-4.5	-3.1	-2.5	V	
Drain Bias Current		600		mA	
Frequency of Operation	225		450	MHz	
DC Function Test					
$I_{G (OFF)}$ – Gate Leakage			2	mA	V_G = -8V, V_D = 0V
$I_{D (OFF)}$ – Drain Leakage			2.5	mA	V_G = -8V, V_D = 48V
$V_{GS (TH)}$ – Threshold Voltage		-3.5		V	V_D = 48V, I_D = 28mA
$V_{DS (ON)}$ – Drain Voltage at High Current		0.25		V	V_G = 0V, I_D = 1.5A
Capacitance					
C_{RSS}		12.5		pF	V_G = -8V, V_D = 0V
C_{ISS}		160.5		pF	V_G = -8V, V_D = 0V
C_{OSS}		36		pF	V_G = -8V, V_D = 0V
RF Functional Test					[1], [2]
V_{GS}		-3.2		V	V_D = 48V, I_D = 600mA
Gain		18		dB	IS95 (9 channel model, 9.8dB PAR at 0.01% CCDF), P_{OUT} = 45.2dBm, f = 450MHz
Drain Efficiency		42		%	IS95 (9 channel model, 9.8dB PAR at 0.01% CCDF), P_{OUT} = 45.2dBm, f = 450MHz

[1] Test Conditions: V_{DSQ} = 48V, I_{DQ} = 600mA, T = 25°C.
[2] Performance in a standard tuned test fixture. ACP: ±1.23MHz at 1.5MHz BW

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Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
RF Functional Test (continued)					[1], [2]
Input Return Loss		-13.5		dB	IS95 (9 channel model, 9.8dB PAR at 0.01% CCDF), P_{OUT} = 45.2dBm, f = 450MHz
PAR		5.7		dB	IS95 (9 channel model, 9.8dB PAR at 0.01% CCDF), P_{OUT} = 45.2dBm, f = 450MHz
RF Typical Performance					[1], [2]
Gain		20		dB	3GPP (TM1, 7.5dB PAR at 0.01% CCDF), P_{OUT} = 45dBm
Drain Efficiency		41		%	3GPP (TM1, 7.5dB PAR at 0.01% CCDF), P_{OUT} = 45dBm
Input Return Loss		-9		dB	3GPP (TM1, 7.5dB PAR at 0.01% CCDF), P_{OUT} = 45dBm
Adjacent Channel Power		-36		dBc	3GPP (TM1, 7.5dB PAR at 0.01% CCDF), P_{OUT} = 45dBm
Power Gain		17		dB	CW, f = 225MHz
P3dB Power		51.6		dBm	CW, f = 225MHz
Saturated Drain Efficiency		75		%	CW, f = 225MHz
Power Gain		16		dB	CW, f = 450MHz
P3dB Output Power		50.4		dBm	CW, f = 450MHz
Drain Efficiency		47		%	CW, f = 450MHz

[1] Test Conditions: V_{DSQ} = 48V, I_{DQ} = 600mA, T = 25 °C.
[2] Performance in a standard tuned test fixture. ACP: ±1.23MHz at 1.5MHz BW

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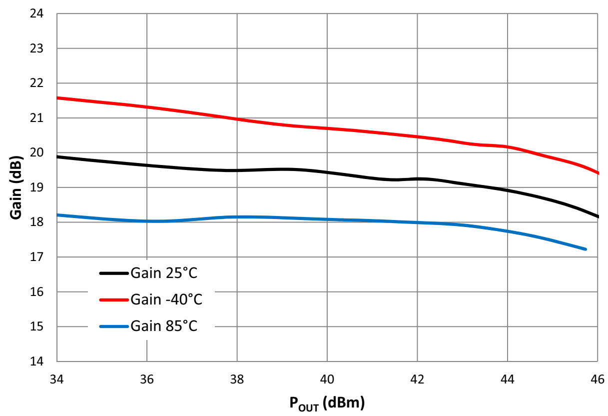
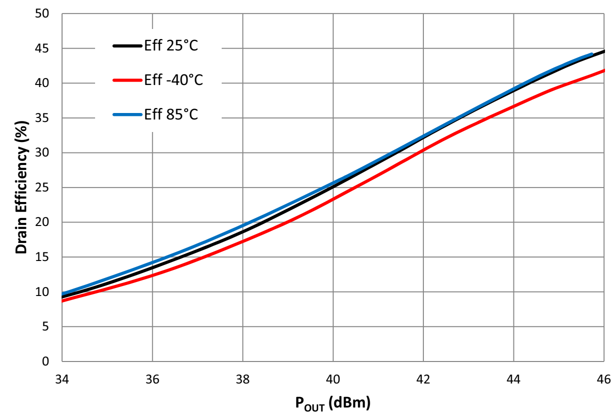
Typical Performance in Fixed Tuned Test Fixture (T = 25°C, unless noted)

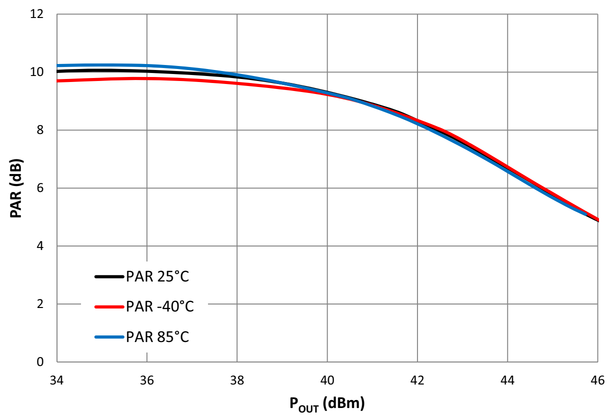
Gain versus P_{OUT}, Freq = 450MHz
IS95 9 Channel 9.8dB PAR at 0.01% CCDF, V_D = 48V, I_{DQ} = 600mA



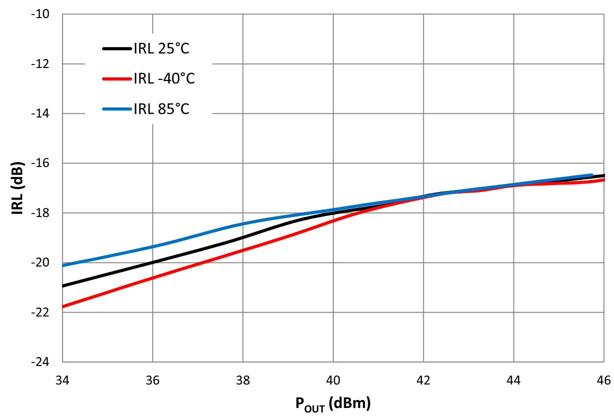
Efficiency versus P_{OUT}, Freq = 450MHz
IS95 9 Channel 9.8dB PAR at 0.01% CCDF, V_D = 48V, I_{DQ} = 600mA



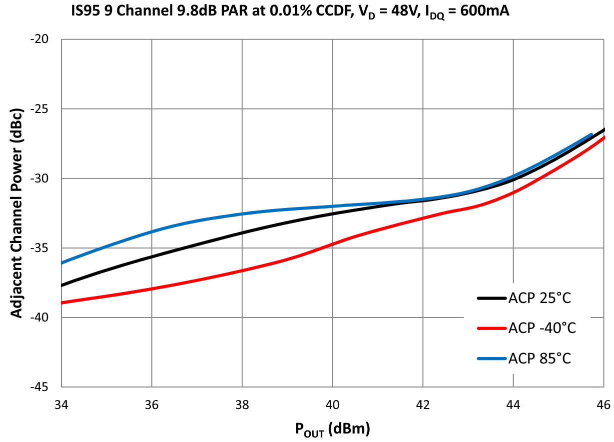
PAR versus P_{OUT}, Freq = 450MHz
IS95 9 Channel 9.8dB PAR at 0.01% CCDF, V_D = 48V, I_{DQ} = 600mA



IRL versus P_{OUT}, Freq = 450MHz
IS95 9 Channel 9.8dB PAR at 0.01% CCDF, V_D = 48V, I_{DQ} = 600mA



ACP versus P_{OUT}, Freq = 450MHz
IS95 9 Channel 9.8dB PAR at 0.01% CCDF, V_D = 48V, I_{DQ} = 600mA



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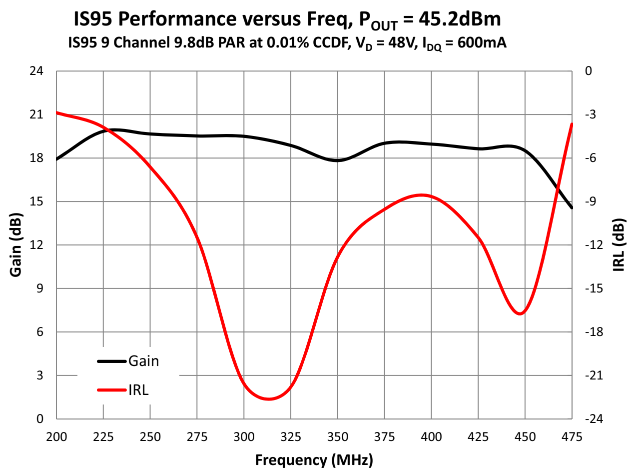
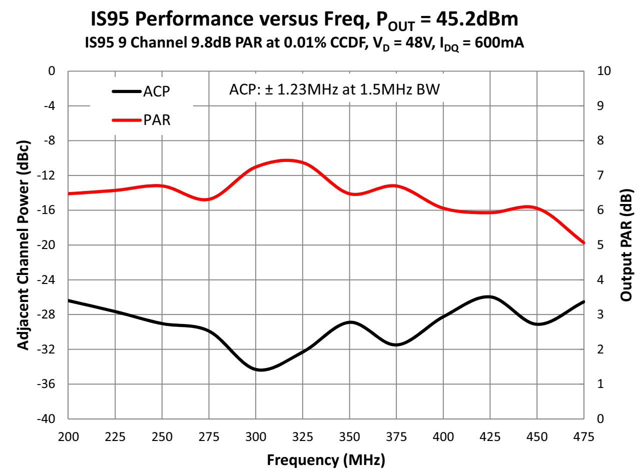
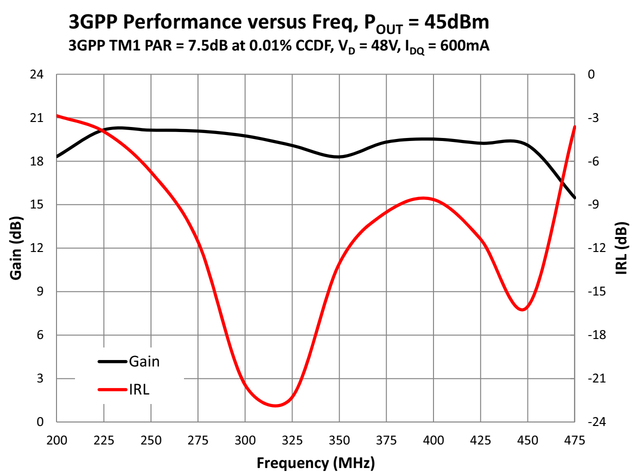
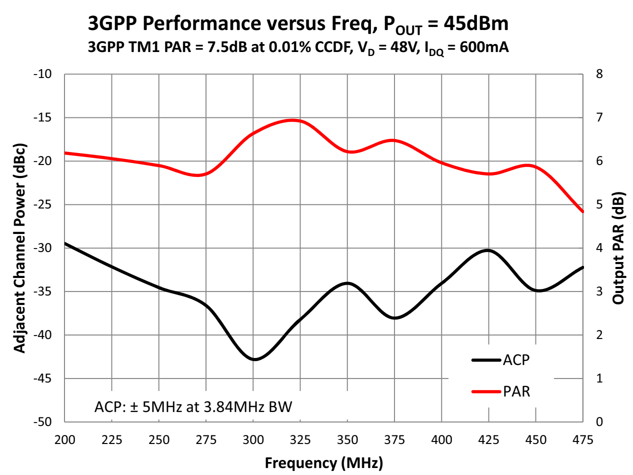
Typical Performance in Fixed Tuned Test Fixture (T = 25°C, unless noted)

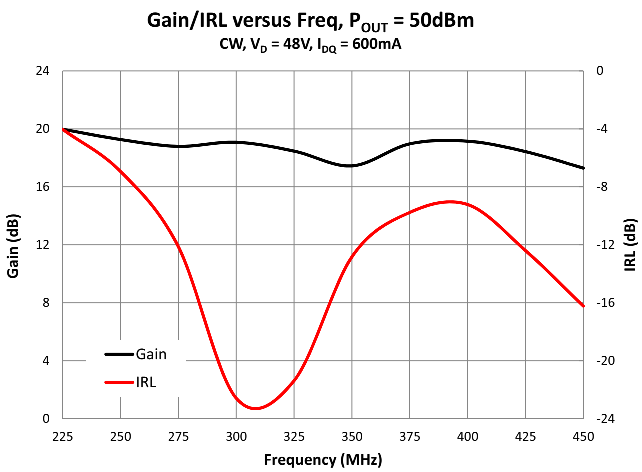


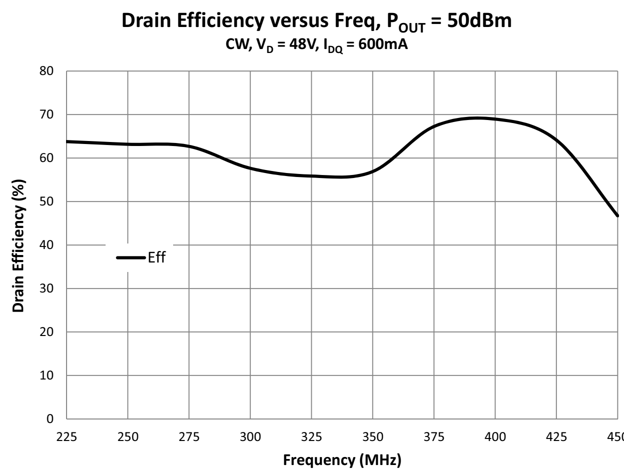


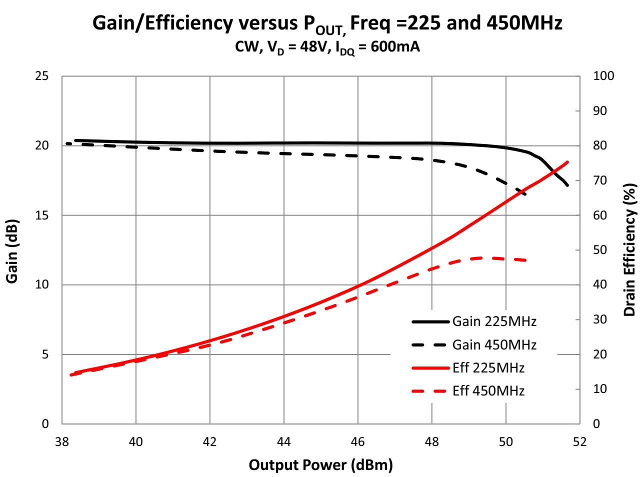


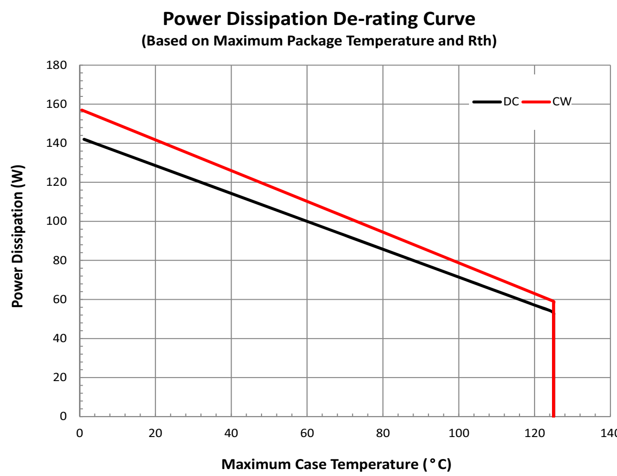


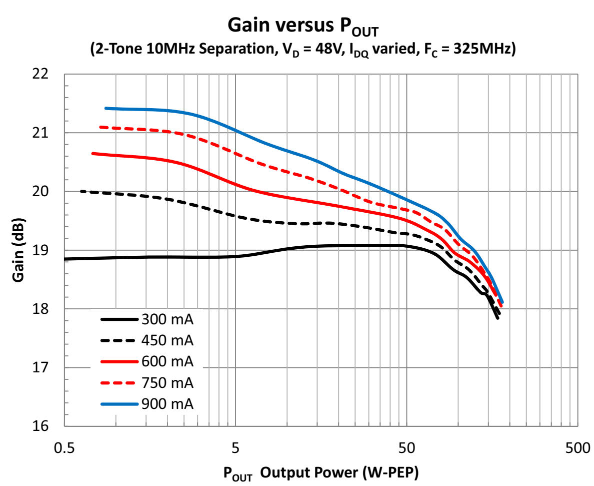
Typical Performance in Fixed Tuned Test Fixture (T = 25°C, unless noted)

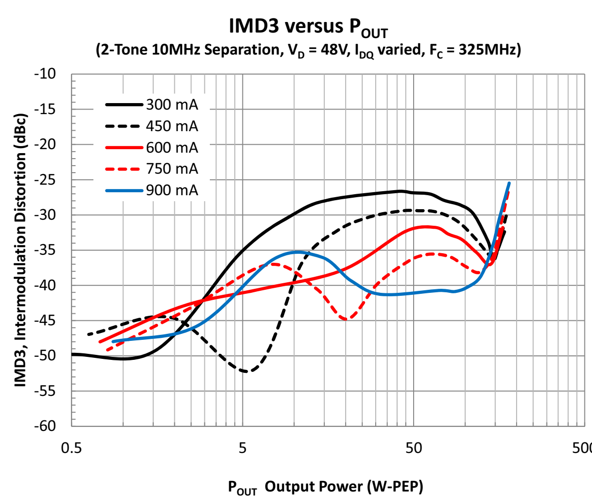




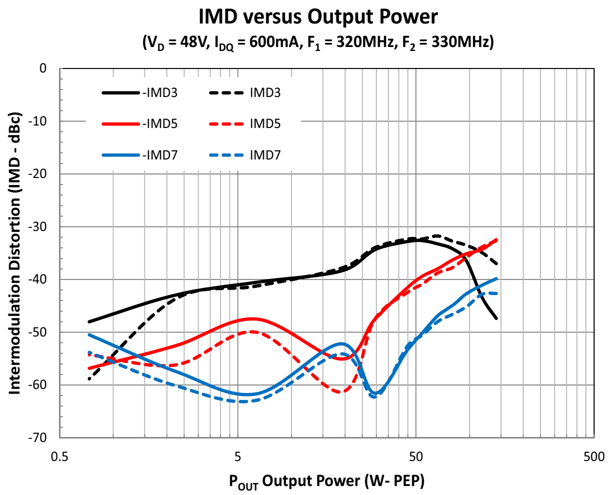


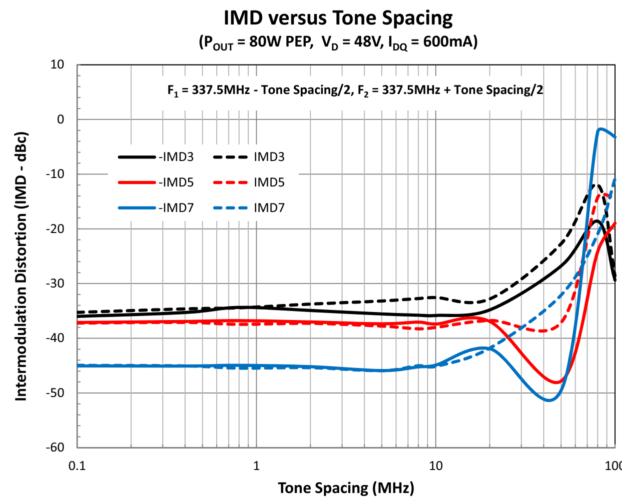






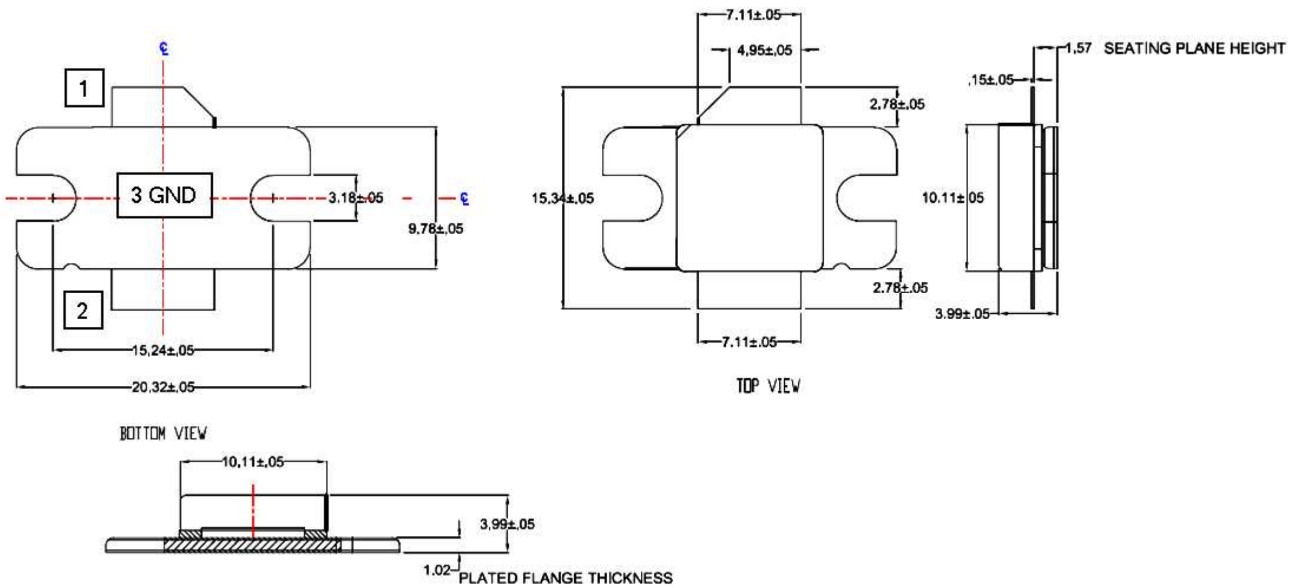
Typical Performance in Fixed Tuned Test Fixture
(T = 25°C, unless noted)





Package Drawing

(All dimensions in mm.)



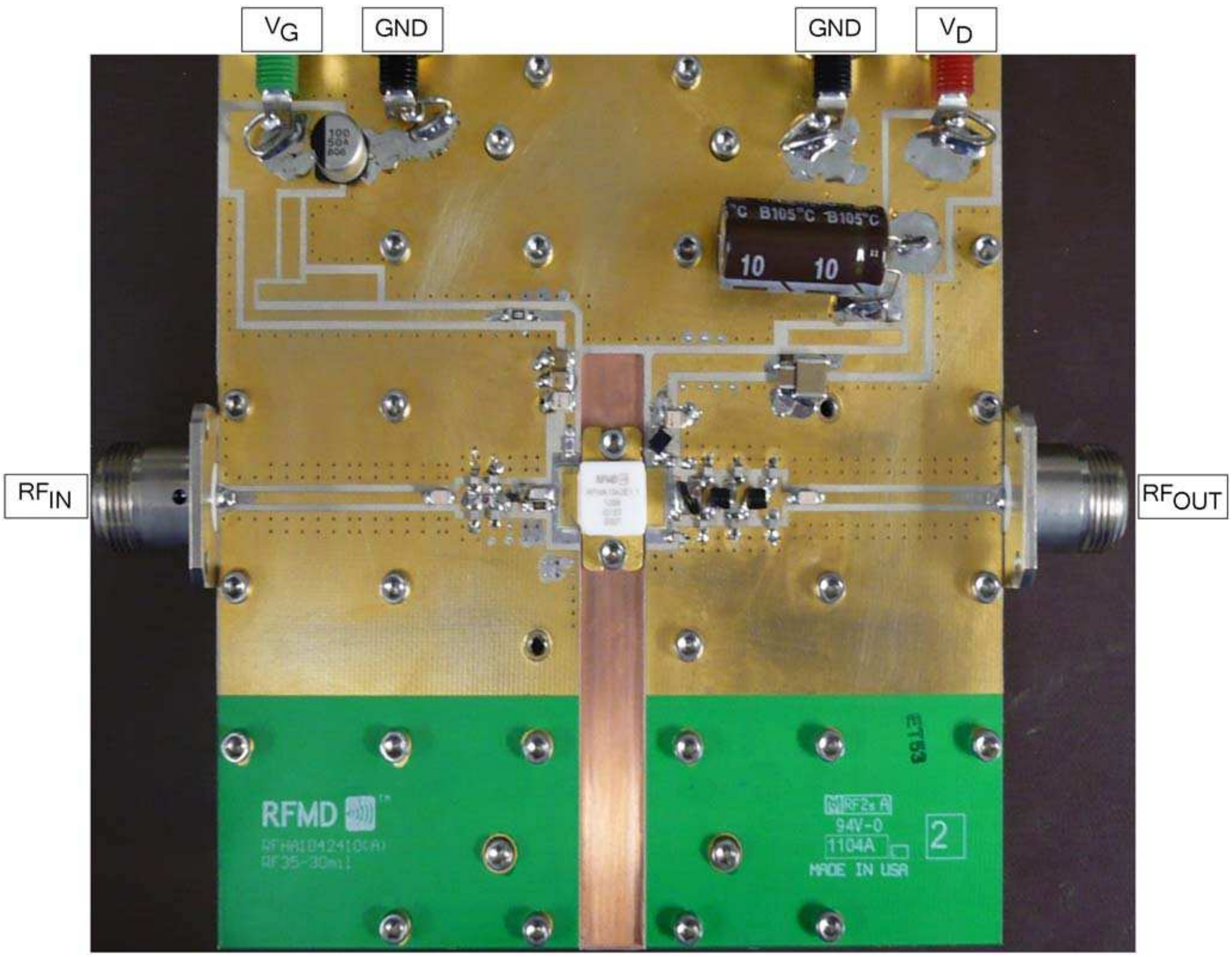
Pin Names and Descriptions

Pin	Name	Description
1	**Gate**	Gate – V_{GQ} RF Input
2	**Drain**	Drain – V_{DQ} RF Output
3	**Source**	Source – Ground Base

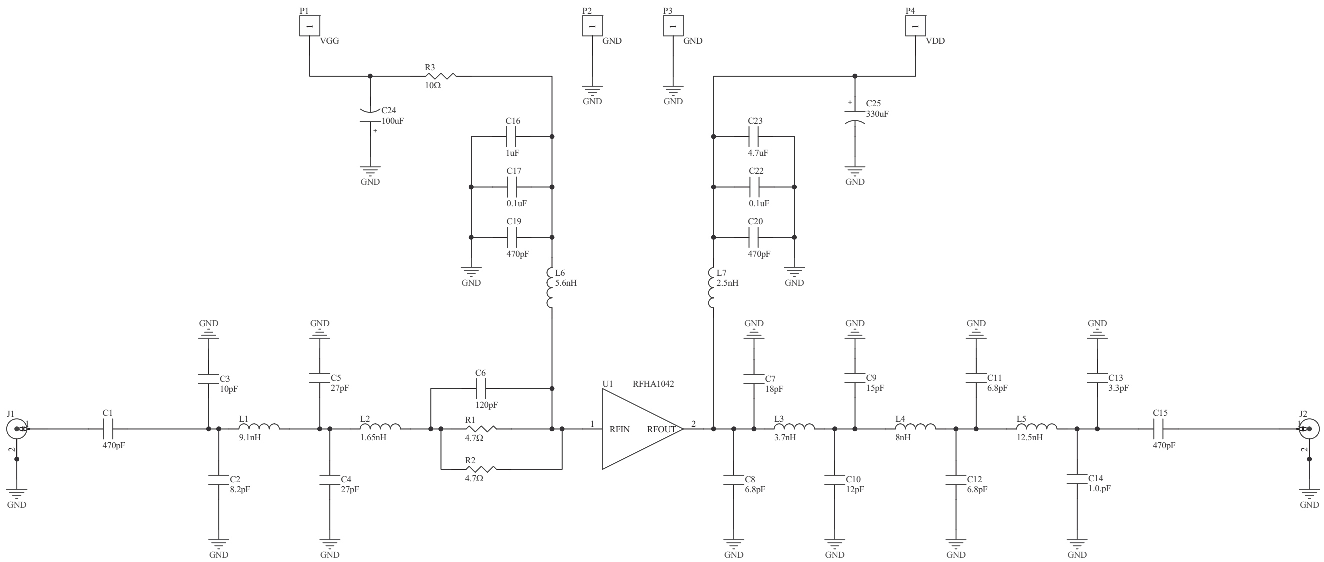
Bias Instruction for RFHA1042 Evaluation Board

ESD Sensitive Material. Please use proper ESD precautions when handling devices of evaluation board. Evaluation board requires additional external fan cooling. Connect all supplies before powering evaluation board.

1. Connect RF cables at RFIN and RFOUT.
2. Connect ground to the ground supply terminal, and ensure that both the VG and VD grounds are also connected to this ground terminal.
3. Apply -5V to V_G.
4. Apply 48V to V_D.
5. Increase V_G until drain current reaches 600mA or desired bias point.
6. Turn on the RF input.



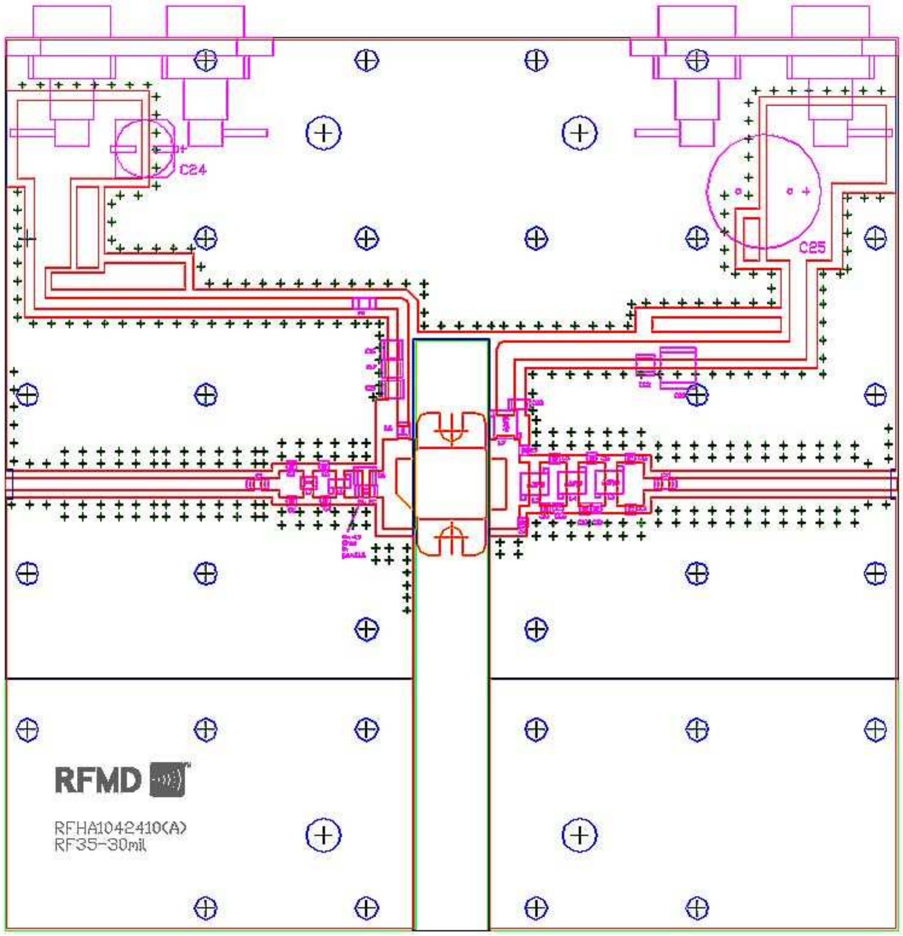
Evaluation Board Schematic



Evaluation Board Bill of Materials

Description	Reference Designator	Manufacturer	Manufacturer's P/N
CAP, 470pF, 5%, 500 WVDC,.110x.110	C1, C15, C19, C20	ATC	ATC100B471JT
8.2pF 800A Chip Capacitor	C2	ATC	ATC800A8R2JT
10pF 800A Chip Capacitor	C3	ATC	ATC800A100JT
27pF 800A Chip Capacitor	C4, C5	ATC	ATC800A270JT
18pF 800A Chip Capacitor	C7	ATC	ATC800A180JT
120pF 800B Chip Capacitor	C6	ATC	ATC800B121JT
15pF 800A Chip Capacitor	C9	ATC	ATC800A150JT
12pF 800A Chip Capacitor	C10	ATC	ATC800A120JT
6.8pF 800A Chip Capacitor	C8, C11, C12	ATC	ATC800A6R8JT
3.3pF 800A Chip Capacitor	C13	ATC	ATC800A3R3JT
1.0pF 800A Chip Capacitor	C14	ATC	ATC800A1R0BT
CAP CER 1.0uF 100V 10% X7R 1210	C16	Murata	GRM32CR72A105KA35B
CAP, 0.1uF, 10%, 100V, X7R, 1210	C17, C22	Murata Electronics	GRM32NR72A104KA01L
CAP, 4.7uF, 10%, 100V, X7R, 2220	C23	Murata Electronics	GRM55ER72A475KA01L
CAP, 100uF, 20%, 50V, AL ELEC, SMD	C24	PANASONIC INDUSTRIAL CO	ECE-V1HA101UP
CAP, 330uF, +/-20%, 100V, FC, RAD	C25	PANASONIC INDUSTRIAL CO	EEU-FC2A331
9.1nH 0805HT (2012) Ceramic Chip Inductor	L1	Coilcraft	0805HT-9N1TJL
1.65nH Micro Spring™ Air Core Inductor	L2	Coilcraft	0906-2KL_
3.7nH Air Core Inductor	L3	Coilcraft	GA3092-ALB
8nH Mini Spring™ Air Core Inductor	L4	Coilcraft	A03TGL_
12.5nH Mini Spring™ Air Core Inductor	L5	Coilcraft	A04TJL_
5.6nH 0805HT (2012) Ceramic Chip Inductors	L6	Coilcraft	0805HT-5N6TJL
2.5nH Mini Spring™ Air Core Inductor	L7	Coilcraft	A01TKL_
RES, 4.7Ω, 5%, 1/4W, 1206	R1, R2	PANASONIC INDUSTRIAL CO	ERJ-8GEYJ4R7V
RES, 10Ω,, 5%, 1/4W, 1206	R3	PANASONIC INDUSTRIAL CO	ERJ-8GEYJ100V

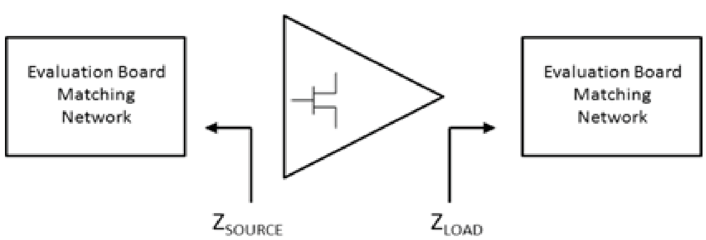
Evaluation Board Layout



Device Impedances

Frequency (MHz)	Z Source (Ω)	Z Load (Ω)
225	7.7 + j1.7	4.4 + j6.0
300	6.3 + j2.2	6.9 + j3.3
375	7.0 + j2.2	6.6 + j3.6
450	3.0 + j0.4	7.2 + j2.3

NOTE: Device impedances reported are the measured evaluation board impedances chosen for a trade-off of efficiency, peak power, and linearity performance across the entire frequency bandwidth.



Device Handling/Environmental Conditions

RFMD does not recommend operating this device with typical drain voltage applied and the gate pinched off in a high humidity, high temperature environment.

GaN HEMT devices are ESD sensitive materials. Please use proper ESD precautions when handling devices or evaluation boards.

GaN HEMT Capacitances

The physical structure of the GaN HEMT results in three terminal capacitors similar to other FET technologies. These capacitances exist across all three terminals of the device. The physical manufactured characteristics of the device determine the value of the C_{DS} (drain to source), C_{GS} (gate to source) and C_{GD} (gate to drain). These capacitances change value as the terminal voltages are varied. RFMD presents the three terminal capacitances measured with the gate pinched off (V_{GS} = -8V) and zero volts applied to the drain. During the measurement process, the parasitic capacitances of the package that holds the amplifier is removed through a calibration step. Any internal matching is included in the terminal capacitance measurements. The capacitance values presented in the typical characteristics table of the device represent the measured input (C_{ISS}), output (C_{OSS}), and reverse (C_{RSS}) capacitance at the stated bias voltages. The relationship to three terminal capacitances is as follows:

$$C_{ISS} = C_{GD} + C_{GS}$$

$$C_{OSS} = C_{GD} + C_{DS}$$

$$C_{RSS} = C_{GD}$$

DC Bias

The GaN HEMT device is a depletion mode high electron mobility transistor (HEMT). At zero volts V_{GS} the drain of the device is saturated and uncontrolled drain current will destroy the transistor. The gate voltage must be taken to a potential lower than the source voltage to pinch off the device prior to applying the drain voltage, taking care not to exceed the gate voltage maximum limits. RFMD recommends applying V_{GS} = -5V before applying any V_{DS}.

RF Power transistor performance capabilities are determined by the applied quiescent drain current. This drain current can be adjusted to trade off power, linearity, and efficiency characteristics of the device. The recommended quiescent drain current (I_{DQ}) shown in the RF typical performance table is chosen to best represent the operational characteristics for this device, considering manufacturing variations and expected performance. The user may choose alternate conditions for biasing this device based on performance trade-offs.

Mounting and Thermal Considerations

The thermal resistance provided as R_{TH} (junction to case) represents only the packaged device thermal characteristics. This is measured using IR microscopy capturing the device under test temperature at the hottest spot of the die. At the same time, the package temperature is measured using a thermocouple touching the backside of the die embedded in the device heatsink but sized to prevent the measurement system from impacting the results. Knowing the dissipated power at the time of the measurement, the thermal resistance is calculated.

In order to achieve the advertised MTTF, proper heat removal must be considered to maintain the junction at or below the maximum of 200°C. Proper thermal design includes consideration of ambient temperature and the thermal resistance from ambient to the back of the package including heatsinking systems and air flow mechanisms. Incorporating the dissipated DC power, it is possible to calculate the junction temperature of the device.

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