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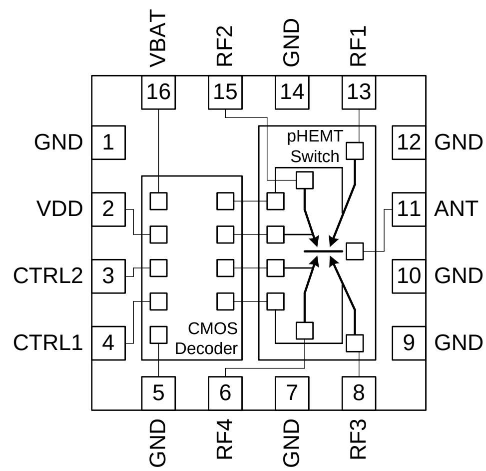
RF1450

BROADBAND HIGH POWER SP4T SWITCH

Package Style: QFN, 16-pin, 3mmx3mm



Functional Block Diagram

Features

- Low Frequency - 2.5GHz Operation
- Low Insertion Loss: 0.4dB at 1GHz
- High Isolation: 29dB at 1GHz
- V_{DD}=2.5V to 2.85V, Down to 1.8V for low power applications
- Compatible With Low Voltage Logic (V_{HIGH} Min=1.3V)
- High Linearity: IMD <-115dBm
- Excellent Harmonic Performance: -80dBc at 1GHz
- GaAs pHEMT Process

Applications

- Cellular Handset Applications
- Multi-Mode GSM, WCDMA Applications
- GSM/GPRS/EDGE Switch Applications
- Cellular Infrastructure Applications

Product Description

The RF1450 is a single-pole four-throw (SP4T) switch designed for general purpose switching applications which require very low insertion loss and high power handling capability. Excellent linearity performance achieved by the RF1450 makes it ideal for multimode GSM/EDGE/WCDMA applications. The RF1450 is ideally suited for battery operated applications requiring high performance switching with very low DC power consumption. Additionally, RF1450 includes integrated decoding logic, allowing just two control lines needed for switch control. The RF1450 is packaged in a very compact 3mmx3mmx0.9mm, 16-pin, leadless QFN package.

Ordering Information

RF1450	Broadband High Power SP4T Switch
RF1450PCBA-410	Fully Assembled Evaluation Board

Optimum Technology Matching® Applied

☐ GaAs HBT	☐ SiGe BiCMOS	☑ GaAs pHEMT	☐ GaN HEMT
☐ GaAs MESFET	☐ Si BiCMOS	☑ Si CMOS	☐ BiFET HBT
☐ InGaP HBT	☐ SiGe HBT	☐ Si BJT	☐ LDMOS

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Absolute Maximum Ratings

Parameter	Rating	Unit
V_{BATT}	6.0	V
V_{DD}	3.0	V
Maximum Input Power (2.5V Control)	38dBm, 0.88GHz, T=25°C 35dBm, 1.88GHz, T=25°C	dBm
Operating Temperature	-20 to +85	°C
Storage Temperature	-35 to +100	°C

Caution! ESD sensitive device.

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability. Specified typical performance or functional operation of the device under Absolute Maximum Rating conditions is not implied.

RoHS status based on EU Directive 2002/95/EC (at time of this document revision).

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Electrical Characteristics					Active Mode: $V_{HIGH} \geq 1.3V$, $V_{LOW} \leq 0.3V$; Temp=25°C; V_{DD}=2.4V to 2.85V P_{IN}=34.5dBm at 0.9GHz or 31.5dBm at 1.8GHz; All RF ports terminated to $Z_0 = 50\Omega$.
Insertion Loss		0.40	0.50	dB	0.5GHz to 1.0GHz
RF1-ANT, RF2-ANT, RF3-ANT, RF4-ANT		0.45	0.60	dB	1.0GHz to 2.0GHz
		0.50	0.60	dB	2.1GHz
		0.60	0.80	dB	2.5GHz
Isolation	27	29		dB	0.5GHz to 1.0GHz
RF1-ANT, RF2-ANT, RF3-ANT, RF4-ANT	22	24		dB	1.0GHz to 2.0GHz
	21	23		dB	2.1GHz
	19	21		dB	2.5GHz
RF Port Return Loss	15			dB	0.5GHz to 2.2GHz, All RF ports in Insertion Loss state.
Operating Characteristics					
Input Power at 0.1dB Compression Point	37			dBm	f=0.9GHz
	34			dBm	f=1.8GHz
Second Harmonic ($2f_0$)		-80	-75	dBc	f=0.9GHz, P_{IN}=34.5dBm
		-85	-75	dBc	f=1.8GHz, P_{IN}=31.5dBm
Third Harmonic ($3f_0$)		-80	-75	dBc	f=0.9GHz, P_{IN}=34.5dBm
		-80	-75	dBc	f=1.8GHz, P_{IN}=31.5dBm
Second Harmonic ($2f_0$)		-80	-75	dBc	f=0.12GHz, P_{IN}=+10dBm, RF 1-4: 10nF DC Block
		-90	-80	dBc	f=0.4GHz, P_{IN}=+10dBm, RF 1-4: 10nF DC Block
Third Harmonic ($3f_0$)		-90	-80	dBc	f=0.12GHz, P_{IN}=+10dBm, RF 1-4: 10nF DC Block
		-90	-80	dBc	f=0.4GHz, P_{IN}=+10dBm, RF 1-4: 10nF DC Block
IMD		-115		dBm	Fundamental Frequency Power Level=+20dBm at 1950MHz Blocker Power Level=-15dBm at 1760MHz
Power Handling into Mismatched Condition		34.5		dBm	VSWR>20; f=0.9GHz
		31.0		dBm	VSWR>20; f=1.8GHz
Switching Speed			5	µs	

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Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Operating Characteristics, cont.					
Start-Up Time			100	µs	Maximum set up time for the switch to reach fully compliant operation
IIP2					
RF1-ANT, RF2-ANT, RF3-ANT, RF4-ANT (Cell)	110	121		dBm	Tone 1: 824MHz at 26dBm, Tone 2: 1693MHz at -20dBm, Receive Freq: 869MHz
RF1-ANT, RF2-ANT, RF3-ANT, RF4-ANT (AWS)	110	114		dBm	Tone 1: 1710MHz at 26dBm, Tone 2: 3820MHz at -20dBm, Receive Freq: 2110MHz
RF1-ANT, RF2-ANT, RF3-ANT, RF4-ANT (PCS)	110	119		dBm	Tone 1: 1850MHz at 26dBm, Tone 2: 3780MHz at -20dBm, Receive Freq: 1930MHz
Triple Beat Ration (TBR)					
RF1-ANT, RF2-ANT, RF3-ANT, RF4-ANT (Cell)	81	88		dBc	VSWR=2:1; Temp=15°C, 25°C, 60°C; Jammer Freq=881.5MHz
RF1-ANT, RF2-ANT, RF3-ANT, RF4-ANT (PCS)	81	88		dBc	VSWR=2:1; Temp=15°C, 25°C, 60°C; Jammer Freq=1960MHz
VDD=1.8V<2.4V, Temp=25°C					
Second Harmonic $2f_0$		-80		dBc	f=0.9GHz, P_{IN}=34.5dBm
		-80		dBc	f=1.8GHz, P_{IN}=31.5dBm
Third Harmonic $3f_0$		-75		dBc	f=0.9GHz, P_{IN}=34.5dBm
		-75		dBc	f=1.8GHz, P_{IN}=31.5dBm
IMD		-105		dBm	Fundamental Frequency Power Level=+20dBm at 1950MHz Blocker Power Level=-15dBm at 1760MHz
Supply and Control Signal Characteristics					
Supply Voltage (V_{BATT})	2.4		4.4*	V	$V_{BAT(min)}$-$V_{DD(max)}$>-0.2V
Supply Current (V_{BATT})					
Standby Mode			0.1	µA	
Active Mode		0.55	1.50	µA	
Switched Supply Voltage (V_{DD})					
V_{HIGH}	1.80	2.50	2.85	V	With reduced specifications below 2.4V V_{DD}, see electrical parameters table.
V_{LOW}		0	0.4	V	
Switched Supply Current (V_{DD})					
I_{HIGH}		160	250	µA	
I_{LOW}		0		mA	
Control Voltage (CTRL1, CTRL2)					
V_{HIGH}	1.3		2.7	V	
V_{LOW}		0	0.3	V	Noise on control lines cannot exceed 0.3V.
Control Current (CTRL1, CTRL2)					
I_{HIGH}		0.5		µA	
I_{LOW}		0.5		µA	

*When V_{BAT} and V_{DD} are tied together $V_{BAT(MAX)}$=2.85V.

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Pin	Function	Description
1	GND	Ground.
2	VDD	Supply. The voltage at this node will be switched and it is important that the switch is operating within the specified start up time. This signal might be used as a mode control.
3	CTRL2	Control signal 2.
4	CTRL1	Control signal 1.
5	GND	Ground.
6	RF4	RF output 4.
7	GND	Ground.
8	RF3	RF output 3.
9	GND	Ground.
10	GND	Ground.
11	ANT	RF input (connected to antenna).
12	GND	Ground.
13	RF1	RF output 1.
14	GND	Ground.
15	RF2	RF output 2.
16	VBAT	Constant supply.
Pkg Base	GND	Ground.

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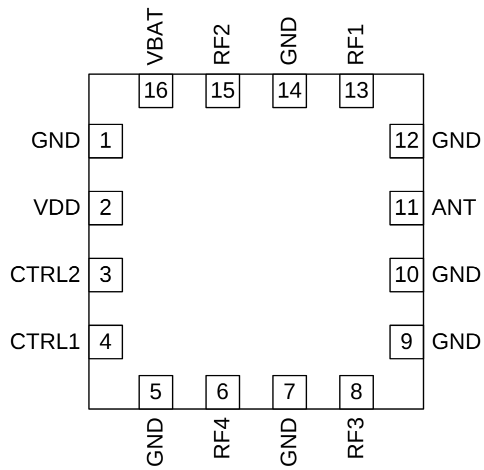
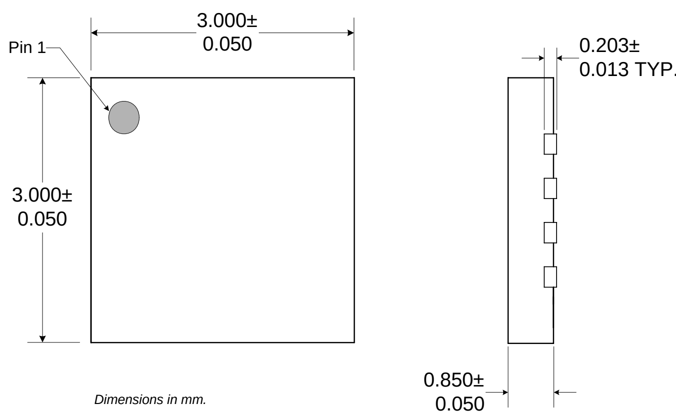
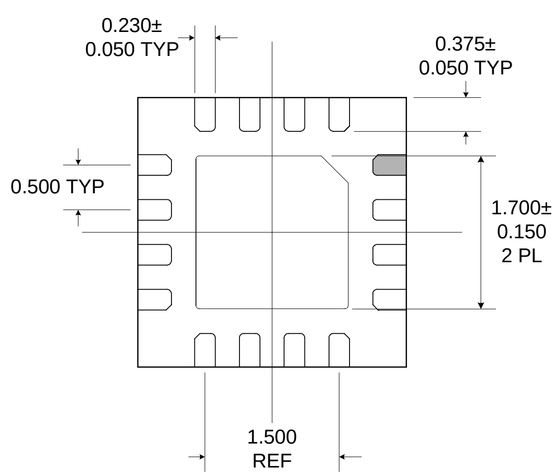
Pin Out



Package Drawing



Dimensions in mm.
Shaded lead is pin 1.



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General Information

Control Logic

The switch is operable in four states (see Truth table, below). The switch is designed for two modes: Active and Stand-by. These modes are controlled by the V_{DD} signal. When VDD is high, the switch is active. The start-up time is defined as the switch activated is critical.

Truth Table for Switch States

State	CTRL1	CTRL2	RF Path
1	V_{LOW}	V_{LOW}	ANT-RF1
2	V_{LOW}	V_{HIGH}	ANT-RF2
3	V_{HIGH}	V_{LOW}	ANT-RF3
4	V_{HIGH}	V_{HIGH}	ANT-RF4

Turn On Sequence

	VBATT	VDD	CTRL1	CTRL2	RF Power
1	ON	OFF	OFF	OFF	OFF
2	X	ON	OFF	OFF	OFF
3	X	X	ON	ON	OFF
4	X	X	X	X	ON

Turn Off Sequence

	VBATT	VDD	CTRL1	CTRL2	RF Power
1	ON	ON	ON	ON	OFF
2	ON	ON	OFF	OFF	X
3	ON	OFF	X	X	X
4	OFF	X	X	X	X

Note: 1:V_{BATT} and V_{DD} can be tied together. In the event V_{BATT} and V_{DD} are supplied from different sources, V_{BATT} must be applied before applying V_{DD} during Turn-On. The part must be turned OFF in reverse order, V_{DD} first then V_{BATT}. Not following these recommendations could damage the part. 2: If V_{BATT} and V_{DD} are tied together $V_{BATT(MAX)}$=2.85V.

Electrical Test Methods

The electrical parameters for the switch were measured on test PWB provided by the switch supplier. The test PWB includes means for decoupling RF signals from control signal port (shunt capacitor at control signal ports).

All measurements are done with calibration plane at switch pins. The effect of test board losses and phase delay has been removed from the results.

Reflected Harmonics Measurement

The reflected harmonics should be measured with the output ports connected to open-circuit or short-circuit impedances. An outline of the measurement set-up is shown in Figure 1. The power in and reflected signal levels are calibrated to the DUT input (reference plane). Note that the power is calibrated in a 50Ω system. The assumption is made that the measurement system is designed so that the harmonic levels of external PA, etc., are far below the signals produced by the DUT.

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The phase delay for RFOUT1 is altered between 0° and 360°, so that all possible load phases are scanned. The VSWR at the connection shall be 20:1at0.9GHz, 15:1at1.8GHz. The other outputs, shall be connected to open-circuit (P_{IN} left open) or signal ground; both options should be tested. After testing RFOUT1, the same test should be done for the other outputs.

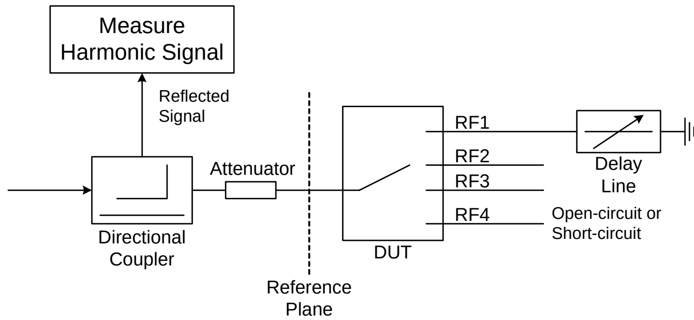
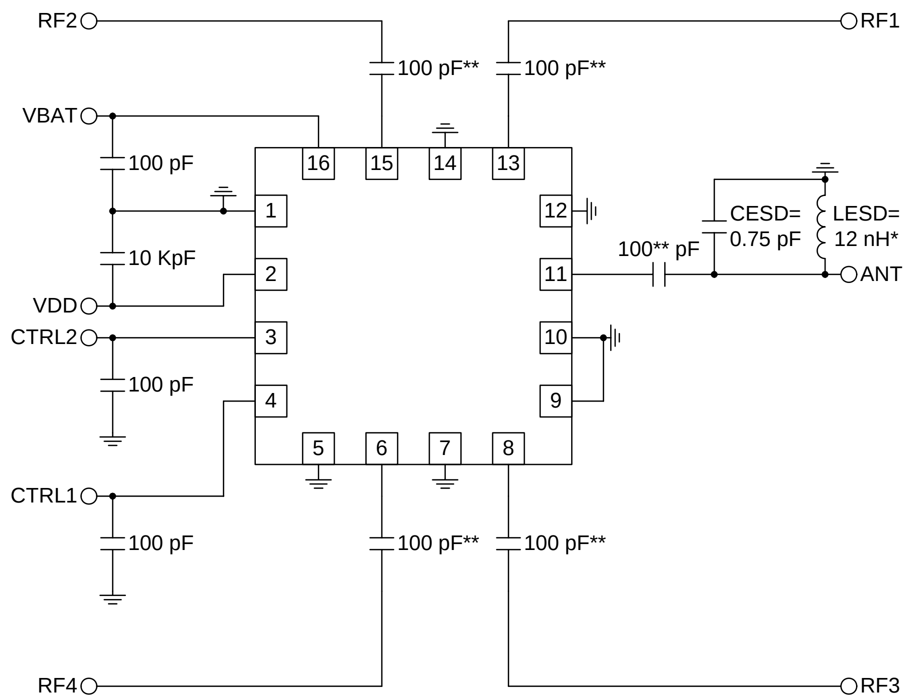


Figure 1. Reflected Harmonics Measurement Set-up

Application Schematic



Application Diagram and Guidelines

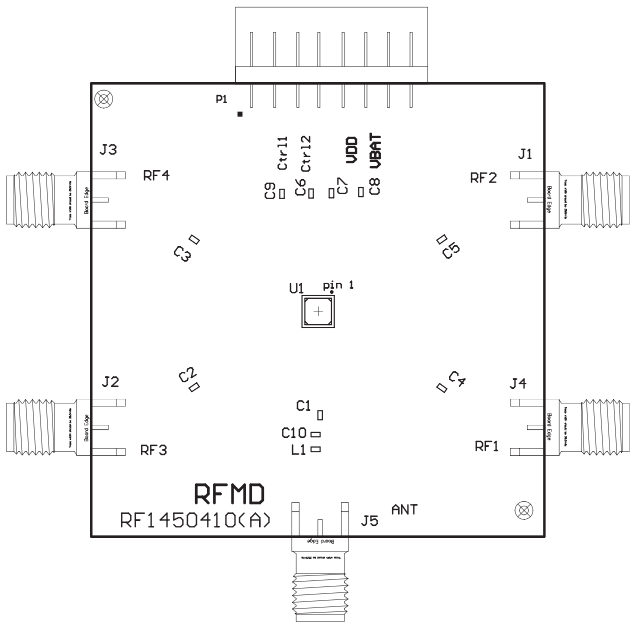
The decoupling capacitors are optional and, if necessary, may be used for noise reduction. Decoupling capacitors on the control pins protect the control circuitry from possible RF leakage. If the switch were to be used in a SP3T configuration, any unused RF ports should be terminated using a capacitor to ground as there is DC on the lines. An ESD filter is needed to protect the switch from antenna ESD events. The filter is formed by LESD inductor and CESD capacitor. The switch has a supply input to feed the built-in logic decoding.

*LESD value will depend on the level of ESD protection and the loss acceptable in a given application.

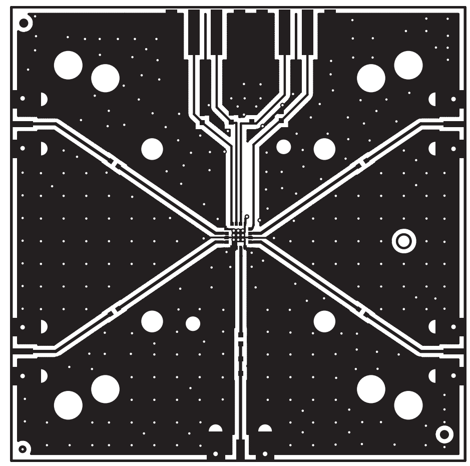
**For ports RF1-RF4 and ANT: need 10nF DC blocking capacitors instead of 100pF (for applications in 100MHz to 700MHz range).

Evaluation Board Layout
Board Size 2.0” x 2.0”
Board Thickness 0.0658”, Board Material FR-4

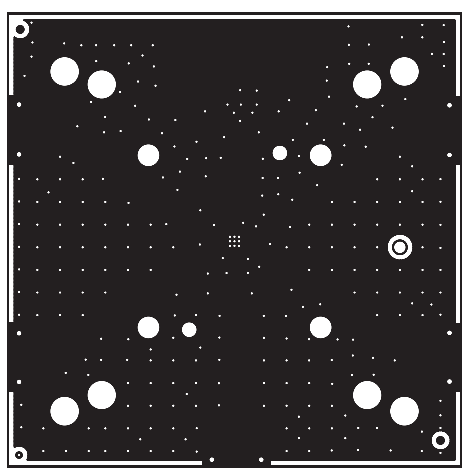
Component Layer



Topside RF Layer



Ground Plane Layer



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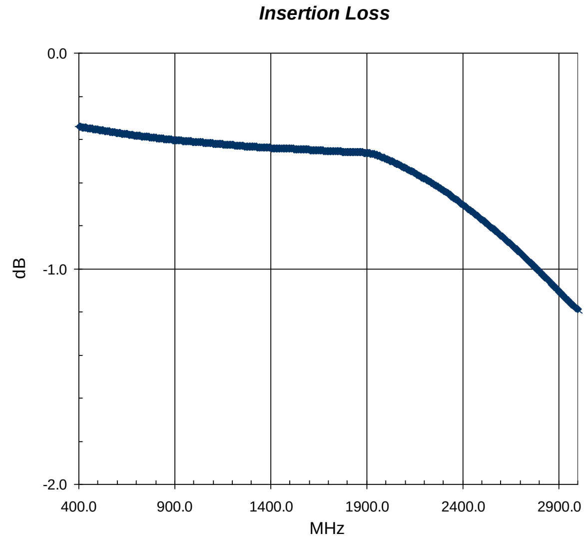
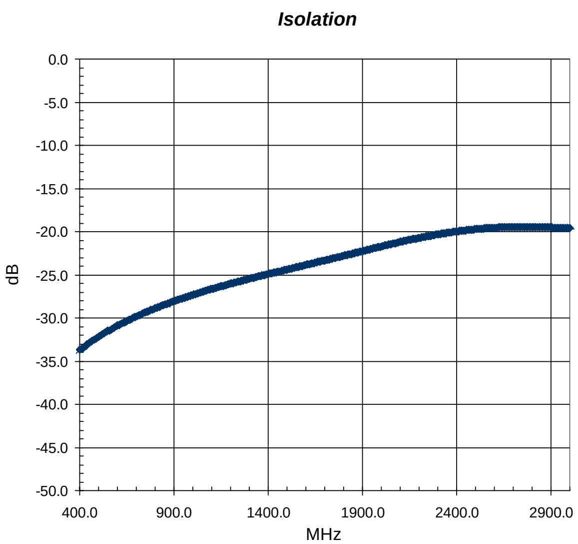
Typical Performance





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PCB Design Requirements

PCB Surface Finish

The PCB surface finish used for RFMD's qualification process is electroless nickel, immersion gold. Typical thickness is 3 μinch to 8 μinch gold over 180 μinch nickel.

PCB Land Pattern Recommendation

PCB land patterns for RFMD components are based on IPC-7351 standards and RFMD empirical data. The pad pattern shown has been developed and tested for optimized assembly at RFMD. The PCB land pattern has been developed to accommodate lead and package tolerances. Since surface mount processes vary from company to company, careful process development is recommended.

PCB Metal Land Pattern

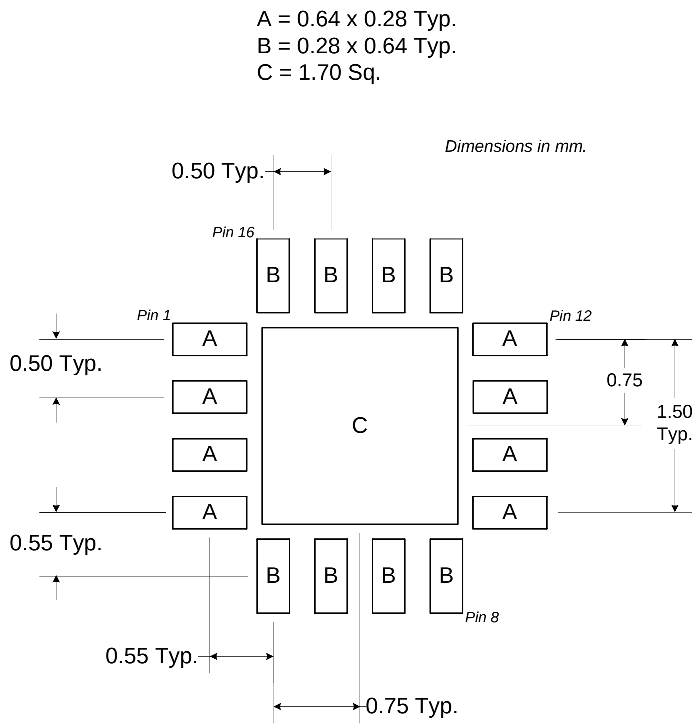

Figure 1. PCB Metal Land Pattern (Top View)

PCB Solder Mask Pattern

Liquid Photo-Imageable (LPI) solder mask is recommended. The solder mask footprint will match what is shown for the PCB metal land pattern with a 2 mil to 3 mil expansion to accommodate solder mask registration clearance around all pads. The center-grounding pad shall also have a solder mask clearance. Expansion of the pads to create solder mask clearance can be provided in the master data or requested from the PCB fabrication supplier.

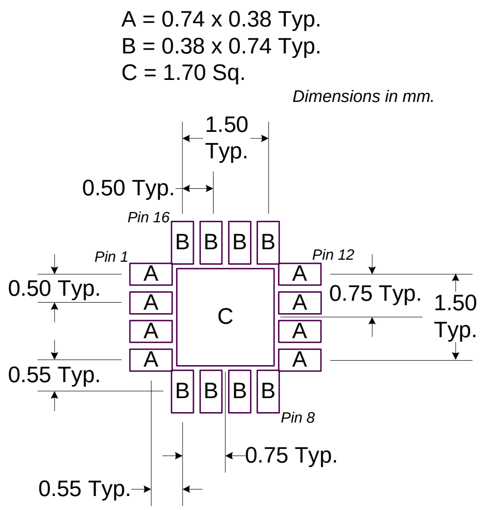

Figure 2. PCB Solder Mask Pattern (Top View)

Thermal Pad and Via Design

The PCB land pattern has been designed with a thermal pad that matches the die paddle size on the bottom of the device.

Thermal vias are required in the PCB layout to effectively conduct heat away from the package. The via pattern has been designed to address thermal, power dissipation and electrical requirements of the device as well as accommodating routing strategies.

The via pattern used for the RFMD qualification is based on thru-hole vias with 0.203 mm to 0.330 mm finished hole size on a 0.5 mm to 1.2 mm grid pattern with 0.025 mm plating on via walls. If micro vias are used in a design, it is suggested that the quantity of vias be increased by a 4:1 ratio to achieve similar results.