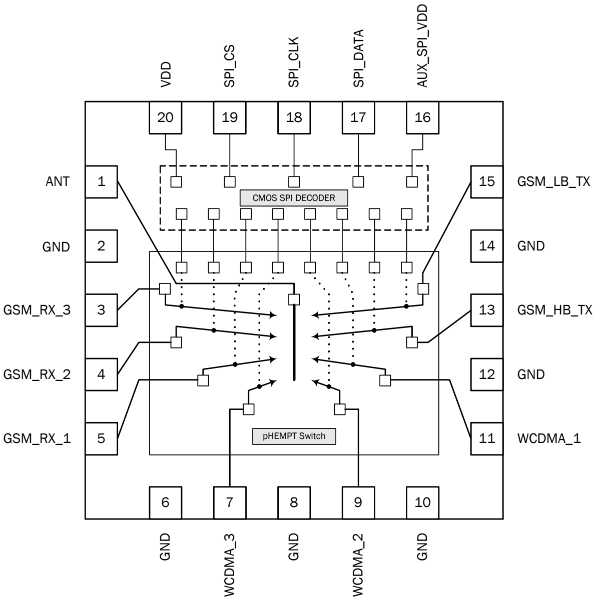
RF1480

SP8T SWITCH

RoHS Compliant & Pb-Free Product
Package Style: QFN, 20-pin, 3.5mmx3.5mm



Functional Block Diagram

Features

- Low Insertion Loss 0.4dB at 1GHz
- High Isolation 26dB at 1GHz
- Controlled by 3-Wire SPI Bus
- Compatible with 1.8V Logic: V_{CTL} High=1.3V to 2.7V
- V_{DD}=1.5V to 3.0V
- AuxSPI V_{DD}=1.5V to 3.0V
- High Linearity IMD3 <-108dBm, IMD2 <-103dBm
- Harmonics: -83dBc at 1GHz
- GaAs pHEMT Process

Applications

- Cellular Handset Applications
- Multi-Mode GSM, WCDMA Applications
- GSM/GPRS/EDGE Switch Applications
- Cellular Infrastructure Applications

Product Description

The RF1480 is a single-pole eight-throw (SP8T) high power switch specially designed for GSM and WCDMA applications. Excellent linearity performance achieved by the RF1480 makes it ideal for multimode GSM/EDGE/WCDMA applications. Additionally, RF1480 includes integrated three wire SPI interface for switch control. The RF1480 is packaged in a very compact 3.5mmx3.5mmx0.85mm, 20-pin, leadless QFN package.

Ordering Information

RF1480	SP8T Switch
RF1480PCBA-410	Fully Assembled Evaluation Board

Optimum Technology Matching® Applied

☐ GaAs HBT	☐ SiGe BiCMOS	☑ GaAs pHEMT	☐ GaN HEMT
☐ GaAs MESFET	☐ Si BiCMOS	☑ Si CMOS	
☐ InGaP HBT	☐ SiGe HBT	☐ Si BJT	

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Absolute Maximum Ratings

Parameter	Rating	Unit
VDD	3.0	V
AUX_SPI_VDD	3.0	V
Maximum Input Power		
GSM_LB_TX	+36	dBm
GSM_HB_TX	+34	dBm
WCDMA 1, 2, 3	+26	dBm
Operating Temperature	-30 to +85	°C
Storage Temperature	-55 to +125	°C

Caution! ESD sensitive device.

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability. Specified typical performance or functional operation of the device under Absolute Maximum Rating conditions is not implied.

RoHS status based on EU Directive 2002/95/EC (at time of this document revision).

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Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
					Nominal Conditions. Unless otherwise specified. $V_{DD}=2.7V$, AuxSPI $V_{DD}=1.8V$, Temp = 25°C
Insertion Loss					
WCDMA 1, 2, 3 to ANT					
1920MHz to 2170MHz		0.75	0.90	dB	GTC3 25.5dBm
1710MHz to 1990MHz		0.70	0.85	dB	GTC3 25.5dBm
824MHz to 960MHz		0.55	0.65	dB	GTC3 25.5dBm
GSM_HB to ANT					
1710MHz to 1910MHz		0.70	0.80	dB	33dBm
GSM_LB to ANT					
824MHz to 915MHz		0.55	0.60	dB	35dBm
GSM_RX 1, 2, 3 to ANT					
869MHz to 960MHz		0.85	0.95	dB	-15dBm
1805MHz to 1990MHz		1.25	1.45	dB	-15dBm
Return Loss					
ANT to Any Port					
824MHz to 2170MHz	11	23		dB	-15dBm
WCDMA 1, 2, 3 to ANT					
824MHz to 2170MHz	17	25		dB	25.5dBm
GSM_HB_TX to ANT					
1710MHz to 1910MHz	20	27		dB	33dBm
GSM_LB_TX to ANT					
824MHz to 915MHz	19	22		dB	35dBm
ANT to Any GSM_RX					
869MHz to 1990MHz	11	20		dB	-15dBm
Forward Isolation					
GSM_HB_TX to ANT					
1710MHz to 1910MHz	26	27		dB	33dBm
GSM_LB_TX to ANT					
824MHz to 915MHz	23	27		dB	35dBm

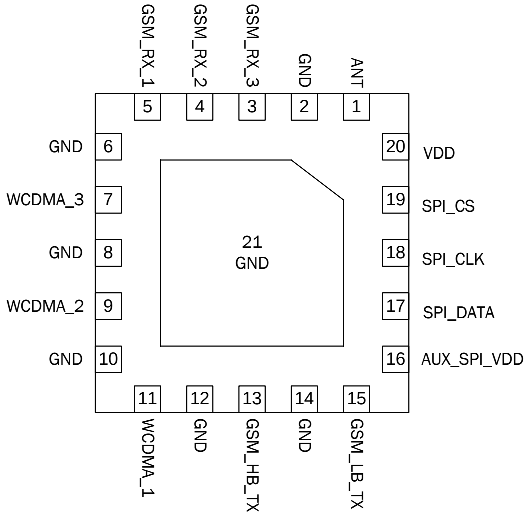
Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Pin to Pin Isolation					
WCDMA 1, 2, 3 to Any RX Port (GSM and W-CDMA)					
1710MHz to 1980MHz	26	27		dB	25.5dBm
GSM_HB_TX to Any RX Port (GSM)					
1710MHz to 1910MHz	35	38		dB	33dBm
GSM_HB_TX to any RX Port (W-CDMA 1, 2, 3)					
1710MHz to 1910MHz	26	27		dB	33dBm
GSM_LB_TX to Any RX Port (GSM)					
824MHz to 915MHz	41	44		dB	35dBm
GSM_LB_TX to any RX Port (W-CDMA 1, 2, 3)					
824MHz to 915MHz	28	29		dB	35dBm
Operating Characteristics					
IIP2	110	113		dBm	WCDMA_1, 2, 3 to Ant
IIP3	64	67		dBm	
Second Harmonic ($2f_0$)					
900MHz		-83		dBc	GSM_LB_TX
1800MHz		-83		dBc	GSM_HB_TX
824MHz to 1980 MHz		-89		dBc	WCDMA_1, 2, 3
Third Harmonic ($3f_0$)					
900MHz		-83		dBc	GSM_LB_TX
1800MHz		-83		dBc	GSM_HB_TX
824MHz to 1980 MHz		-89		dBc	WCDMA_1, 2, 3
IMD3					
F_{TX}=1950MHz F_{INT}=1760		-111.0	-104.5	dBm	TX power level=+20dBm, 50Ω
IMD2					
F_{TX}=1950MHz F_{INT}=190		-107	-104	dBm	Interferer=-15dBm, 50Ω WCDMA_1, 2, 3 to Ant
Spectrum Emissions					
824MHz to 1980 MHz TX			-83	dBc	WCDMA_1, 2, 3 to Ant 25.5 dBm, 75% duty cycle
1710MHz to 19180 MHz TX			-83	dBc	GSM_HB_TX to Ant 33 dBm, 75% duty cycle
824MHz to 915 MHz TX			-83	dBc	GSM_LB_TX to Ant 35 dBm, 75% duty cycle
869MHz to 1990 MHz RX			-132.5	dBm	Ant to any GSM_RX RBW=180kHz
869MHz to 2170 MHz RX			-114	dBm	Ant to WCDMA_1, 2, 3 RBW=3.84MHz

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Operating Characteristics (continued)					
Power Handling in Mismatched Condition					
900MHz		35		dBm	VSWR > 20:1
1800MHz		33		dBm	VSWR > 20:1
Switching Speed		0.5	2	µs	
Start-up Time		7	10	µs	Time for the switch to be operational from the time that the switched supply voltage (V_{DD}) goes high.
Supply and Control Signal Characteristics					
Switch Supply Voltage (V_{DD})	2.5	2.7	3.0	V	Continuously
Switch Supply Current (V_{DD})		500	850	µA	Active Mode DC DC Converter on
		400	650	µA	Active Mode DC DC Converter off
		20	30	µA	Standby Mode (Switch disabled)
SPI Supply Voltage ($AuxSpiV_{DD}$)	1.5	1.8	3.0	V	SPI Controller enabled
		0	0.3	V	Standby Mode (Switch disabled)
SPI Supply Current ($AuxSpiI_{DD}$)		250	400	µA	During SPI read
SPI Controller Enable			150	µs	
SPI Control Voltage					
V_{HIGH}		1.8		V	SPI_EN, SPI_CLK
V_{LOW}		0		V	SPI_DATA

*Through phase is defined as measured normalized using a reference calibration PWB.

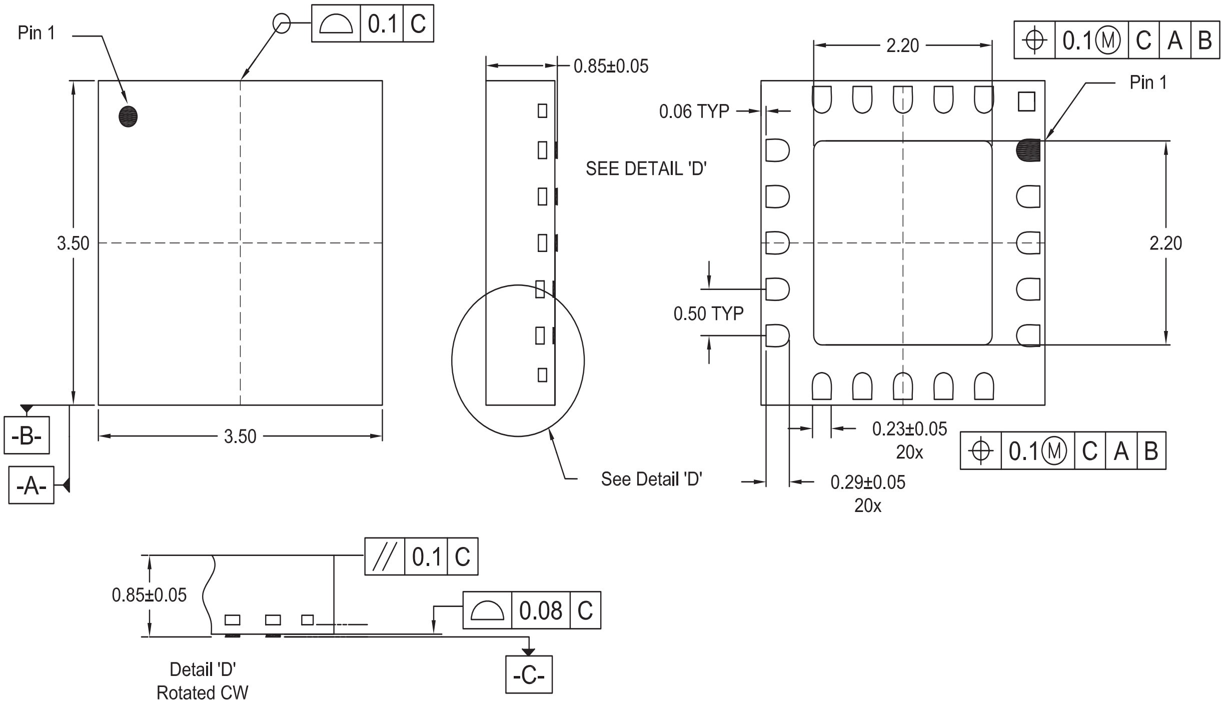
Pin	Function	Description
1	ANT	RF Input (connected to antenna).
2	GND	Ground.
3	GSM_RX_3	GSM RF Output 3.
4	GSM_RX_2	GSM RF Output 2.
5	GSM_RX_1	GSM RF Output 1.
6	GND	Ground.
7	WCDMA_3	WCDMA RF Input/Output 3.
8	GND	Ground.
9	WCDMA_2	WCDMA RF Input/Output 2.
10	GND	Ground.
11	WCDMA_1	WCDMA RF Input/Output 1.
12	GND	Ground.
13	GSM_LB_TX	GSM RF Input (High Band).
14	GND	Ground.
15	GSM_HB_TX	GSM RF Input (Low Band).
16	AUX_SPI_VDD	SPI Supply Voltage.
17	SPI_DATA	SPI Data Input.
18	SPI_CLK	SPI Clock Input.
19	SPI_CS	SPI Chip select.
20	VDD	Supply. The voltage at this node will be switched on before AUX_SPI_VDD is powered up.
Pkg Base	GND	

Pin Out


GSM_RX_1
GSM_RX_2
GSM_RX_3
GND
ANT
5
4
3
2
1
GND 6
WCDMA_3 7
GND 8
WCDMA_2 9
GND 10
20 VDD
19 SPI_CS
18 SPI_CLK
17 SPI_DATA
16 AUX_SPI_VDD
21
GND
11
12
13
14
15
WCDMA_1
GND
GSM_HB_TX
GND
GSM_LB_TX

Top View
(Through Package)

Package Drawing


Pin 1
0.1 C
3.50
3.50
-B-
-A-
0.85±0.05
SEE DETAIL 'D'
See Detail 'D'
2.20
0.1Ⓜ C A B
Pin 1
0.06 TYP
2.20
0.50 TYP
0.23±0.05
20x
0.1Ⓜ C A B
0.29±0.05
20x
0.1 C
0.85±0.05
0.08 C
-C-
Detail 'D'
Rotated CW

General Information

Data Write
The SP8T switch is controlled by a 30-bit 3-wire SPI bus.

This section describes how the SP8T is programmed through the 30-bit 3-wire SPI bus.

Bit	Function	Set	Description
29	Read/Write Mode	1	Not used for front end switch
		0	Write to the switch
28	Address (Slave Type)	0	001 used for front end switches
27		0	
26		1	
25	Address (Slave Identifier)	0	This is a non-volatile value programmed by the vendor. 00000=FE switch module for single antenna radios or for TX path FE switch module in multi-antenna radios. 00001=Diversity front end switch (not used on this “main” switch)
24		0	
23		0	
22		0	
21		0	
20	Address (Slave SPI Register)	0	Only one SPI register will be used on the front end switch
19		0	
18		0	
17		0	
16		0	
15	DCDC Converter Enable	1/0	A logic high enables the DCDC converter (if applicable).
14 13 12 11	FE Select 4=MSB FE Select 3 FE Select 2 FE Select 1=LSB	0000	Switch disabled (low current mode)
		0001	GSM_HB_TX enable
		0010	GSM_LB_TX enable
		0011	Not used/reserved
		0100	GSM_RX_1 enable
		0101	GSM_RX_2 enable
		0110	GSM_RX_3 enable
		0111	Not used/reserved
		1000	WCDMA_1 enable
		1001	WCDMA_2 enable
		1010	WCDMA_3 enable
		1011	Not used/reserved
10	Not Used	X	Not used/reserved
9	Not Used	X	Not used/reserved
8	Not Used	X	Not used/reserved
7	Not Used	X	Not used/reserved
6	Not Used	X	Not used/reserved
5	Not Used	X	Not used/reserved
4	Not Used	X	Not used/reserved
3	Not Used	X	Not used/reserved
2	Not Used	X	Not used/reserved
1	Not Used	X	Not used/reserved
0	Not Used	X	Not used/reserved

Global Command Write

A global command is when bits 28-21 are all sent with high logic level. In this mode, bits 20-16 are used to issue the command, and bits 15-0 are ignored. If bits 20-16 are all sent with high logic level, the switch will go into standby mode until a SPI command is issued to enable it. If bits 28-16 are not all "1", the command is ignored.

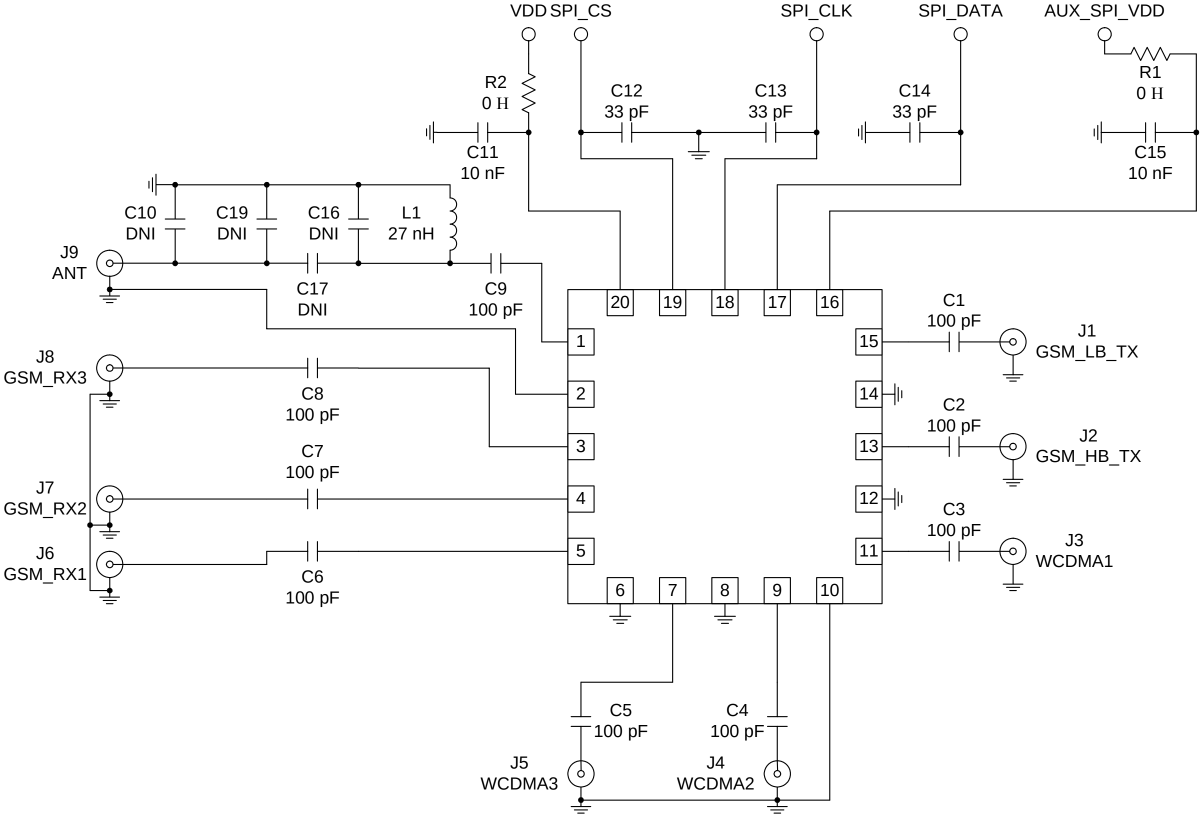
Bit	Function	Set	Description
29	Read/Write Mode	0	Logic low command puts device in read mode
28	Address (Slave Type)	1	111 used for global write
27		1	
26		1	
25	Address (Slave Identifier)	1	11111 used for global write
24		1	
23		1	
22		1	
21		1	
20	Command	1/0	A transmission of "11111" must put the switch into standby mode.
19		1/0	
18		1/0	
17		1/0	
16		1/0	
15	Not Used	X	Data bit must be ignored during Global Command Write
14	Not Used	X	Data bit must be ignored during Global Command Write
13	Not Used	X	Data bit must be ignored during Global Command Write
12	Not Used	X	Data bit must be ignored during Global Command Write
11	Not Used	X	Data bit must be ignored during Global Command Write
10	Not Used	X	Data bit must be ignored during Global Command Write
9	Not Used	X	Data bit must be ignored during Global Command Write
8	Not Used	X	Data bit must be ignored during Global Command Write
7	Not Used	X	Data bit must be ignored during Global Command Write
6	Not Used	X	Data bit must be ignored during Global Command Write
5	Not Used	X	Data bit must be ignored during Global Command Write
4	Not Used	X	Data bit must be ignored during Global Command Write
3	Not Used	X	Data bit must be ignored during Global Command Write
2	Not Used	X	Data bit must be ignored during Global Command Write
1	Not Used	X	Data bit must be ignored during Global Command Write
0	Not Used	X	Data bit must be ignored during Global Command Write

Electrical Test Methods

The electrical parameters for the switch are measured on test PWB provided by RFMD. The test PWB includes means for decoupling RF signals from control signal port (shunt capacitor at control signal ports).

All measurements are done with calibration plane at switch pins. The effect of test board losses and phase delay are removed from the results by calibrating using the calibration board.

Application Schematic


VDD
SPI_CS
SPI_CLK
SPI_DATA
AUX_SPI_VDD
R2
0 H
R1
0 H
C11
10 nF
C12
33 pF
C13
33 pF
C14
33 pF
C15
10 nF
C10
DNI
C19
DNI
C16
DNI
L1
27 nH
J9
ANT
C17
DNI
C9
100 pF
J8
GSM_RX3
C8
100 pF
J7
GSM_RX2
C7
100 pF
J6
GSM_RX1
C6
100 pF
C1
100 pF
J1
GSM_LB_TX
C2
100 pF
J2
GSM_HB_TX
C3
100 pF
J3
WCDMA1
C5
100 pF
C4
100 pF
J5
WCDMA3
J4
WCDMA2
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20

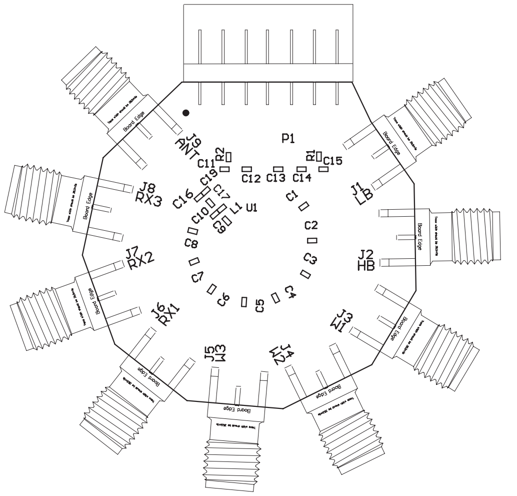
Application Environment

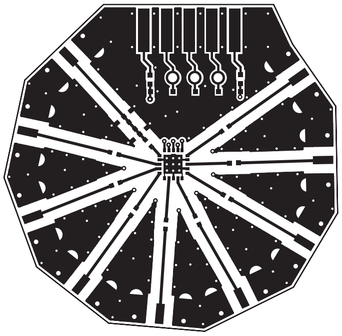
The switch can be placed directly under, or in close vicinity to, the antenna. Shielding cans covering the switch are not required, and they can be in close vicinity to the PA. The switch can be mounted on a flexible PWB.

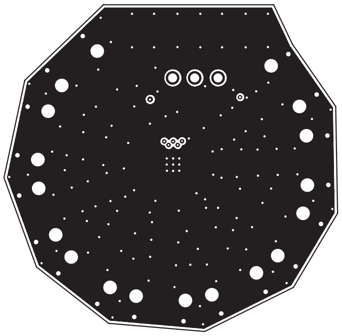
Application Diagram and Guidelines

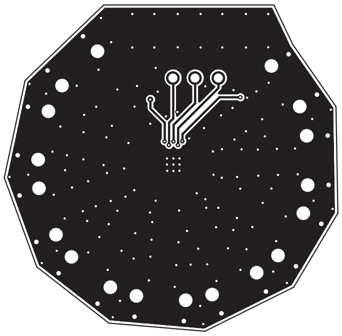
The series coupling capacitors are required for pins 1, 3, 4, 5, 7, 9, 11, 13, and 15. Decoupling capacitors on the control pins protect the control circuitry from possible RF leakage. To protect the switch from ESD from the antenna, an ESD filter (L1) is needed. The switch has a supply input to feed the built-in logic decoding. All unused ports require a series decoupling capacitor followed by a shunt 50Ω resistor to ground.

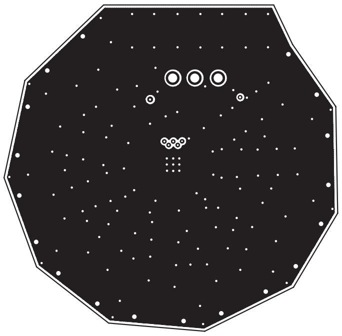
Evaluation Board Layout
Board Size 1.5” Diameter
Board Thickness 0.0656”, Board Material FR-4 and Rogers R04003

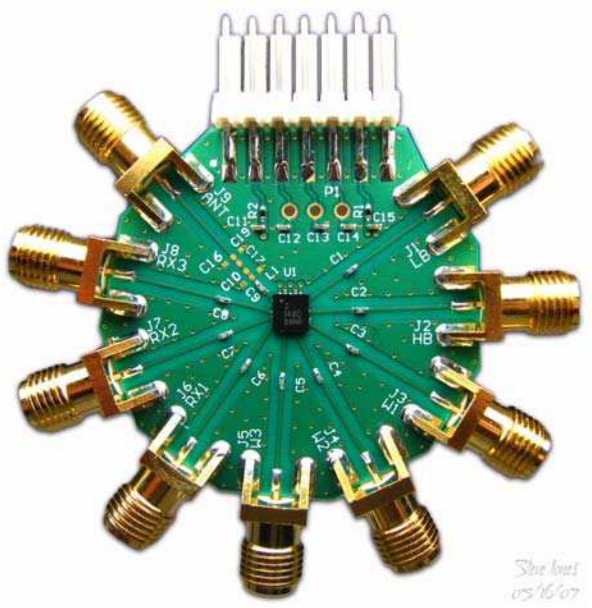

P1
J9
ANT
R2
C11
R1
C15
C12
C13
C14
C19
C17
C16
C10
L1
U1
C9
C1
C2
C3
C4
C5
C6
C7
C8
J8
RX3
J1
LB
J2
HB
J7
RX2
J6
RX1
J3
W1
J4
W2
J5
W3
Board Edge










J9
ANT
J8
RX3
J7
RX2
J6
RX1
J5
W3
J4
W2
J3
W1
J2
HB
J1
LB
P1
U1
Steve Jones
05/16/07