RF6650

POWER MANAGEMENT IC

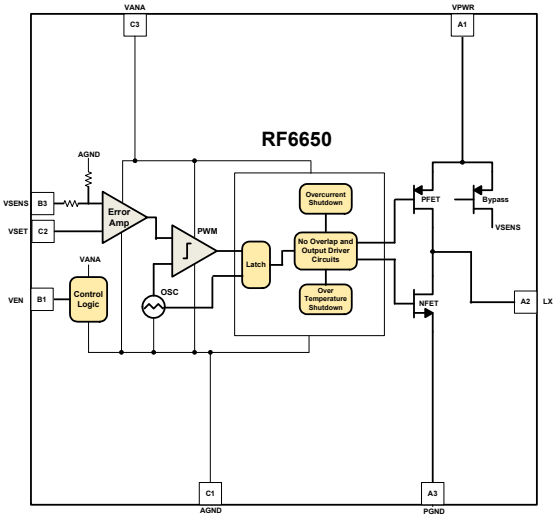
Package: 8-Bump WLCSP, 3x3 Array, 1.58mm x 1.57mm

Features

- High Efficiency >95%
- Transient Response <25µs
- 650mA Load Current Capability
- Programmable Output Voltage
- Bypass FET
- Constant Switching Frequency
- V_{BAT} Range=2.7V to 5.1V
- Over-Temperature Shutdown
- Over-Current Shutdown

Applications

- W-CDMA Handsets



Functional Block Diagram

Product Description

The RF6650 is a pulse width modulated (PWM), voltage-mode controlled DC-DC converter unit designed to supply power to a W-CDMA power amplifier. The output voltage is continuously programmable through the VSET analog input pin according to the transfer function $V_{OUT}=V_{SET}x2.5$. The converter has been optimized for high efficiency at light current load conditions, fast transient response times to meet W-CDMA 25µs slot-to-slot transition specifications, and low noise by maintaining a constant switching frequency, while supplying up to 650mA in PWM controlled or bypass modes. Bypass mode is automatically enabled when $V_{BAT}<3.3V$ and $V_{SET}>1.55V$. The converter is enabled when $V_{EN}>1.3V$. The RF6650 is a 1.58mm x 1.57mm, 8-bump, WLCSP device.

Ordering Information

RF6650	Power Management IC
RF6650PCBA-410	Fully Assembled Evaluation Board

Optimum Technology Matching® Applied

☐ GaAs HBT	☐ SiGe BiCMOS	☐ GaAs pHEMT	☐ GaN HEMT
☐ GaAs MESFET	☐ Si BiCMOS	☑ Si CMOS	☐ RF MEMS
☐ InGaP HBT	☐ SiGe HBT	☐ Si BJT	☐ LDMOS

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Absolute Maximum Ratings

Parameter	Rating	Unit
Input Supply Voltage (V_{PWR}, V_{ANA})	-0.2 to +6.0	V
Analog Input (V_{SET}, V_{EN})	-0.2 to V_{ANA}-0.2	V
Ground Voltage	-0.2 to +0.2	V
Operating Ambient Temperature (T_A)	-30 to +85	°C
Storage Temperature (T_{STORE})	-40 to +150	°C

Caution! ESD sensitive device.

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability. Specified typical performance or functional operation of the device under Absolute Maximum Rating conditions is not implied.

RoHS status based on EUDirective2002/95/EC (at time of this document revision).

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Operating Conditions					See app schematic for component values. Typ: V_{BAT}=3.6V, V_{EN}=1.3V, T_A=25 °C. Min/max: V_{BAT}=2.7V to 5.1V, T_A=-30 °C to +85 °C.
Supply Voltage	2.7	3.6	5.1	V	V_{BAT}=V_{PWR} and V_{ANA} connected together
Output Load Current			650	mA	
Junction Temperature	-30		+125	°C	
Operating Temperature	-30		+85	°C	
General Specifications					
Quiescent Current		700	1400	µA	V_{SET}=0V, no load
Shut Down Current			20	µA	V_{EN}=Low
Logic High Input Threshold V_{IH}	1.3			V	V_{EN}
Logic Low Input Threshold V_{IL}			0.5	V	V_{EN}
Input Current			1	µA	V_{EN}, V_{SET}
Thermal Shutdown		160		°C	Rising temperature
		30		°C	Hysteresis
Over-Current Shutdown Trip Point		2.2		A	Full FET. V_{OUT}=3.4V, V_{BAT} = 4.2V
		1.4		A	1/3 FET. V_{OUT}=0.6V.
DC Specifications					
V_{SET} Range	0.2		1.4	V	See note 1.
Transfer Function Gain (V_{OUT}/V_{SET})		2.50		V/V	$V_{OUT} \leq V_{BAT}$-V_{DO}
Efficiency		69		%	V_{OUT}=0.6V, I_{OUT}=25mA
		83		%	V_{OUT}=0.8V, I_{OUT}=65mA
		91		%	V_{OUT}=1.5V, I_{OUT}=200mA
		95		%	V_{OUT}=3.4V, I_{OUT}=460mA, $V_{BAT} \geq$4.2V
FET Segmentation Threshold		0.45		V	Rising V_{SET}, activates all FETs. Full FET mode.
		0.35		V	Falling V_{SET}, disables 2/3 of the FETs, 1/3 FET mode.
Output Voltage Ripple		10		mV_{PP}	V_{OUT}=1.5V
Dropout Voltage (V_{DO})		170		mV	V_{SET}=1.2V, V_{BAT}=3.0V, I_{OUT}=500mA Dropout=V_{BAT}-V_{OUT}
Load Regulation		5		mV/A	V_{OUT}=3.0V, I_{OUT}=100mA to 500mA
Line Regulation		2		mV/V	V_{OUT}=3.0V, I_{OUT}=300mA, V_{BAT}=3.6V to 5.5V

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Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
AC Specifications					
Switching Frequency		1.9		MHz	
V_{OUT} Startup Time			25	µs	V_{OUT}=0V to 0.6V±10%, I_{OUT}<1mA
			25	µs	V_{OUT}=0V to 3.4V±10%, I_{OUT}<1mA, V_{BAT}≥4.2V
V_{OUT} Response Time			25	µs	V_{OUT}=0.6V to 3.4V±100mV, R_{LOAD}=5Ω, V_{BAT}≥4.2V
			25	µs	V_{OUT}=3.4V to 0.6V±100mV, R_{LOAD}=25Ω, V_{BAT}≥4.2V
SMPS to BYPASS Time			5	µs	V_{SET}=1.0V to 1.7V, I_{OUT}=460mA, V_{BAT}=3.0V. See note 2.
			20	µs	V_{BAT}=4.6V to 3.0V, I_{OUT}=460mA, V_{SET}=1.7V. See note 2.
BYPASS to SMPS Time			50	µs	V_{SET}=1.7V to 1.0V, I_{OUT}=460mA, V_{OUT}=3.0V
			50	µs	V_{BAT}=3.0V to 4.6V, I_{OUT}=460mA, V_{SET}=1.7V
Load Transient			100	mVpk	V_{OUT}=1.8V, I_{OUT}=20mA to 200mA, T_{RISE}=T_{FALL}=10µs
			50	mVpk	V_{OUT}=3.4V, I_{OUT}=400mA to 550mA, V_{BAT}=4.2V, T_{RISE}=T_{FALL}=10µs
Line Transient			40	mVpk	V_{OUT}=600mV, I_{OUT}=25mA, ΔV_{BAT}=600mV, T_{RISE}=T_{FALL}=10µs
			150	mVpk	V_{OUT}=3.4V, I_{OUT}=450mA, ΔV_{BAT}=600mV, T_{RISE}=T_{FALL}=10µs, V_{BAT}=4.2V
Bypass Specifications					
Resistance		150		mΩ	V_{SET}=1.7V, V_{BAT}=3.0V, I_{OUT}=500mA
Enable Trip Point (V_{SET})		1.55		V	Rising V_{SET}, I_{OUT}=500mA, V_{BAT}=3.0V
Enable Trip Point (V_{BAT})		3.3		V	Falling V_{BAT}, I_{OUT}=500mA, V_{SET}=1.7V
Disable Trip Point (V_{SET})		1.45		V	Falling V_{SET}, I_{OUT}=500mA, V_{BAT}=3.0V
Disable Trip Point (V_{BAT})		3.5		V	Rising V_{BAT}, I_{OUT}=500mA, V_{SET}=1.7V
Dropout Voltage		75		mV	V_{SET}=1.7V, V_{BAT}=3.0V, I_{OUT}=500mA Dropout=V_{BAT}-V_{OUT}
V_{OUT} Startup Time			15	µs	V_{SET}=0V to 1.7V, V_{BAT}=3.0V, I_{OUT}≤1mA

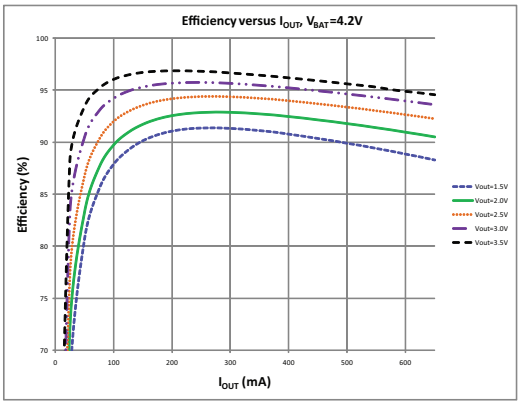
Notes:
1. The V_{SET} range under normal SMPS operation is 1.4V resulting in V_{OUT}=3.5V; however, the only limit to this value is imposed by the Absolute Maximum Rating of the VSET pin. This pin also is used to activate the bypass mode when supply voltage is low. For this reason, a value of V_{SET}=1.7V is often used in this specification to enable the bypass mode.
2. Differences in timing result from capacitance on triggered pin. For example, V_{BAT} has greater capacitance as seen in the application schematic.

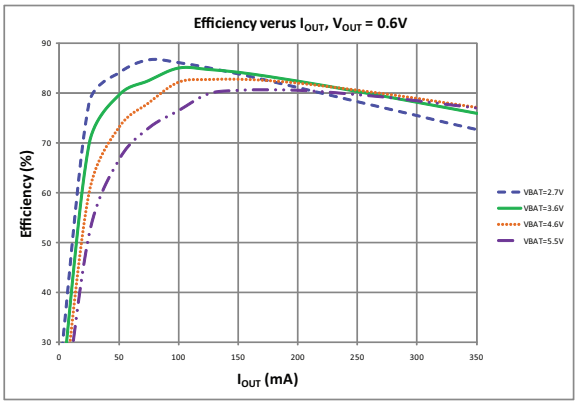
Bypass Control Table (both conditions must be met)

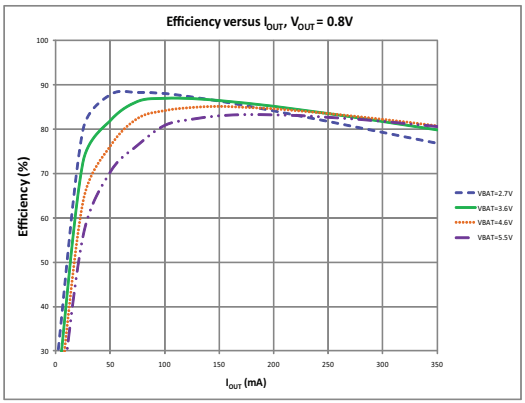
Mode	V_{SET}	V_{BAT}
Bypass Enable	>1.55V	<3.3V
Bypass Disable	<1.45V	>3.5V

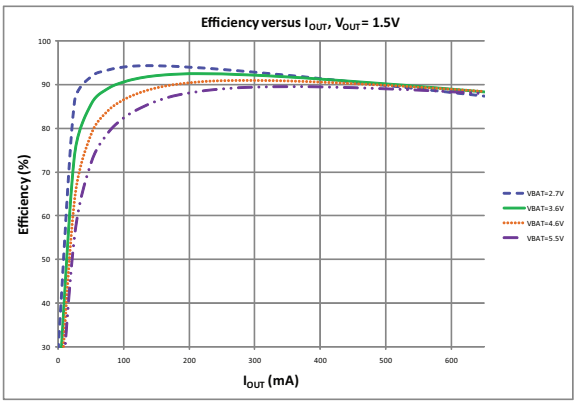
FET Segmentation Control Table

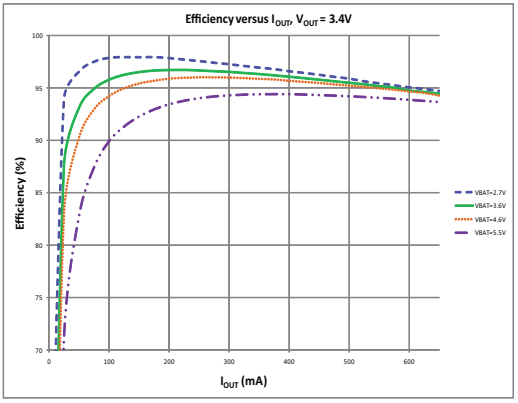
Mode	V_{SET}
Full FET	>0.45V
1/3 FET	<0.35V











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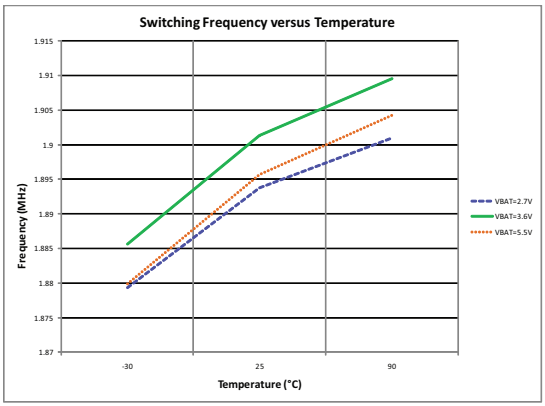
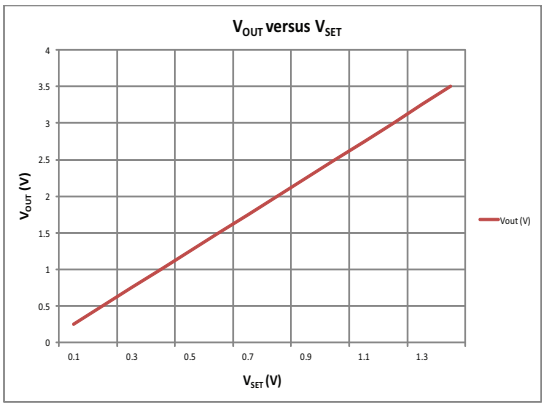
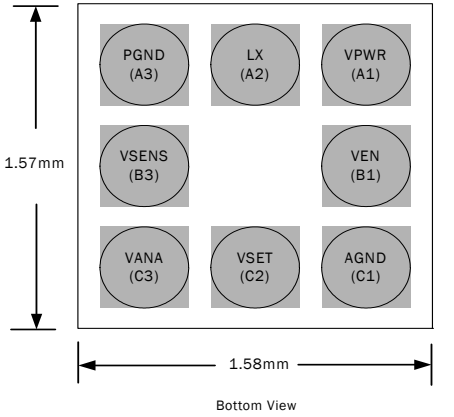

Switching Frequency versus Temperature
Frequency (MHz)
1.915
1.91
1.905
1.9
1.895
1.89
1.885
1.88
1.875
1.87
-30
25
90
Temperature (°C)
VBAT=2.7V
VBAT=3.6V
VBAT=5.5V


VOUT versus VSET
VOUT (V)
4
3.5
3
2.5
2
1.5
1
0.5
0
0.1
0.3
0.5
0.7
0.9
1.1
1.3
VSET (V)
Vout (V)

Pin	Function	Description
A1	VPWR	Supply used for the final output stage. Local 2.2µF decoupling capacitor required.
A2	LX	DC-DC Converter Switch Output. Connect to the filter inductor as recommended on application schematic.
A3	PGND	DC-DC Converter Power Ground.
B1	VEN	This pin enables the DC to DC converter.
B3	VSENS	Feedback node from the output. Connect to a point after the V_{OUT} inductor.
C1	AGND	Ground for the analog circuits. Isolate from PGND to help reduce noise.
C2	VSET	Analog reference input used to set the output voltage.
C3	VANA	Supply used for the analog circuitry inside the power management IC. Separate 2.2µF decoupling capacitor required.

Pin Out

3x3 array, 8 bumps. Bump diameter=0.300mm. Pitch=0.500mm. Die size=1.58mmx1.57mm=2.48mm^2.



Bottom View

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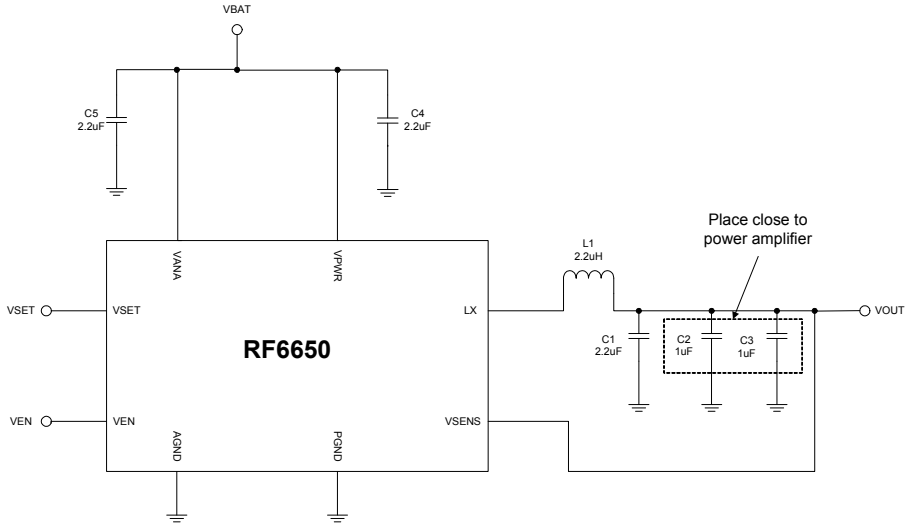
Application Schematic



Notes:

1. The LC filter (power filter) consists of L1 and C1 near the DUT and the distributed capacitances C2 and C3 near the load. The main loop of L1 and C1 should be as small as possible with a large ground plane connecting C1 to the PGND pin. Capacitors C2 and C3 are placed at the VDD pins of the load and should also have a clear return path to PGND. The loop filter is designed to have a total capacitance of 4.2µF (C1=2.2µF, C2=1µF, C3=1µF).
2. Capacitors C2 and C3 are placed a small distance away from the DUT on the evaluation board to emulate the distributed effects of the trace resistance as would be expected in the application. If the evaluation board is used to power a separate board that contains decoupling capacitors on the VOUT trace, capacitors C2 and C3 should be removed or decreased in value so that the total capacitance is approximately 4.2µF.
3. A separate decoupling capacitor should be used for the VPWR and VANA pins. The current return path for the analog and power sections should be kept separate. To decrease the number of component types, a value of 2.2µF is selected. Additional 100µF decoupling capacitors are used on the evaluation board to more closely model a battery at the DUT. The 100µF capacitors will not be needed in a battery-supplied system.
4. The parasitic resistance of L1 and C1 should be kept within the limits $R_{ESRL} < 100\,m\Omega$, $R_{ESRC} = 10\,m\Omega$. Recommended components are given in the table below. Selecting alternate components will have an impact on the reported performance including, but not limited to, changes in the efficiency.

Application Schematic Components

Designator	Case Size	Quantity	Value	Manufacturer	Part Number
L1	2.5x2.0x1.0	1	2.2µH	Murata	LQM2HPN2R2MG0L
C1, C4, C5	0603	3	2.2µF	Murata	GRM188R61A225KE34D
C2, C3	0603	2	1µF	Taiyo Yuden	RMTMK107BJ105KA-T

Theory of Operation

DC-DC buck converter operation involves the stepping down of a higher battery voltage to a lower output voltage by alternately switching a PFET and NFET pair through an external LC filter. At a 2MHz switching frequency the PFET is enabled every 500ns. The duty cycle at the LX switching node, which is continuously variable from 0% to 100%, is set by the PWM controller based on the V_{SET} analog voltage and V_{BAT} voltage to realize the desired output voltage. The PWM controller maintains accuracy, stability, and accounts for losses in the system by feedback through the VSENS pin. The controller has been designed with non-overlapping control circuitry to prevent V_{BAT} shoot-through current to ground.

The converter has been optimized for high efficiency at light load by balancing DC and AC switching losses incurred in the output FETs, the switching frequency, and the external LC filter. In addition, output FET segmentation and selective biasing have been employed to further enhance light load efficiencies.

Unlike other DC-DC converter solutions on the market, the RF6650 does not alter the switching frequency at light load conditions to boost efficiency. This type of efficiency enhancement has a severe detriment on the system by injecting spurious noise at various frequencies. With our expertise in front-end transmit module design, RFMD proposes to operate this converter at a constant switching frequency to minimize system level interference. The ripple voltage, also a major component of noise injection into the PA, has also been minimized by selecting a larger inductance value.

Despite the attention to high efficiency, the transient performance of the device, defined as an output voltage transient from 600mV to 3.4V or vice-versa, has not been overlooked. The PWM controller has been properly tuned with a fast type III loop filter to mate with an external LC filter (L=2.2μH and C=2.2 μF+1 μF+1 μF=4.2 μF). The result is a converter with sufficient bandwidth to meet 25μs W-CDMA slot-to-slot transition time requirements. The slew rate of the V_{SET} pin should be limited to 100mV/μs to achieve the best performance.

Lastly, the external inductor and capacitors were specifically selected to balance efficiency over the load current operating range and transient performance while minimizing total board area. Inductors and capacitors of different values may be used at risk to converter stability and performance (i.e., efficiency).

Shutdown

When V_{EN}<0.5V the device enters shutdown mode. In this mode all features are disabled to minimize battery quiescent current.

Over-Temperature Protection

An internal over-temperature shutdown circuit is employed to protect the device from excessively high junction temperatures. The shutdown occurs at typically 160°C and will re-enable when the temperature drops below the activation point typically by 30°C.

Over-Current Protection

For the RF6650, an over-current shutdown (OCSD) circuit is employed to provide over-current fault protection. This methodology deactivates the output FETs in the case of an over-current fault as opposed to limiting the current. In this way the device only experiences the over-current condition for a short transient period and is not subject to continuous high current flow. Once the DUT is shut down, it will not restart automatically if the fault condition is removed. Toggling the V_{EN} pin is required for restart.

Bypass Mode

The RF6650 contains a bypass mode that activates a large PFET device in parallel with the switched-mode power supply (SMPS) PFET when both V_{BAT}<3.3V and V_{SET}>1.55V. Such a condition results in a 100% duty cycle and activates the bypass FET to reduce the output resistance and dropout voltage.

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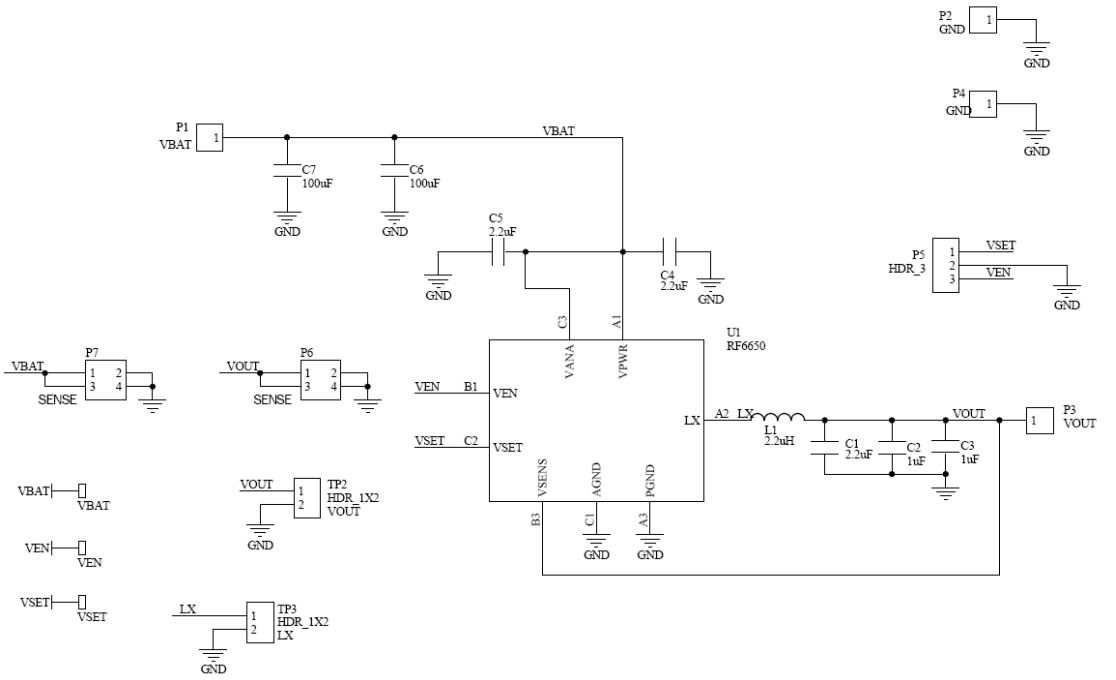
FET Segmentation

The main power FETs are designed in three sections to improve efficiency during light load conditions expected with low output voltages. When V_{SET} is raised to >0.45V, all three sections of the output FETs are on (full FET mode). When V_{SET} is reduced to <0.35V, one of the three sections is used (1/3 FET mode). Approximately 100mV of hysteresis is used to avoid switching between the modes unintentionally.

Board Layout

Good DC-DC converter layout practices in this application are strongly recommended to reduce radiated and conducted system noise. Placement of the VPWR bypass capacitor is critical and must be such to minimize the AC supply and ground return current loop through the PFET. In addition, the placements of the LC filter (L1 and C1) are also critical to minimize the AC supply and ground return current loop through the NFET.

Evaluation Board Schematic



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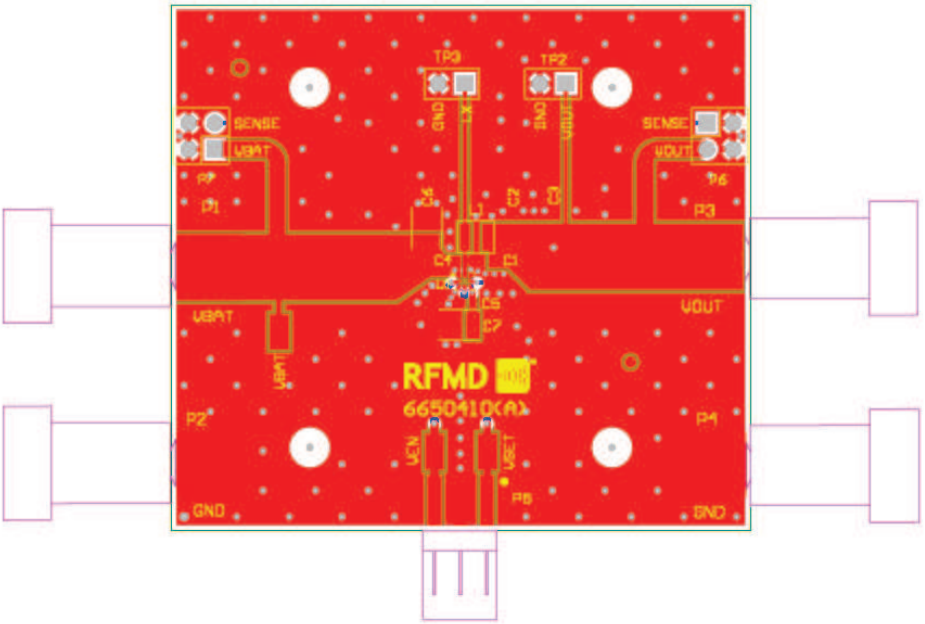
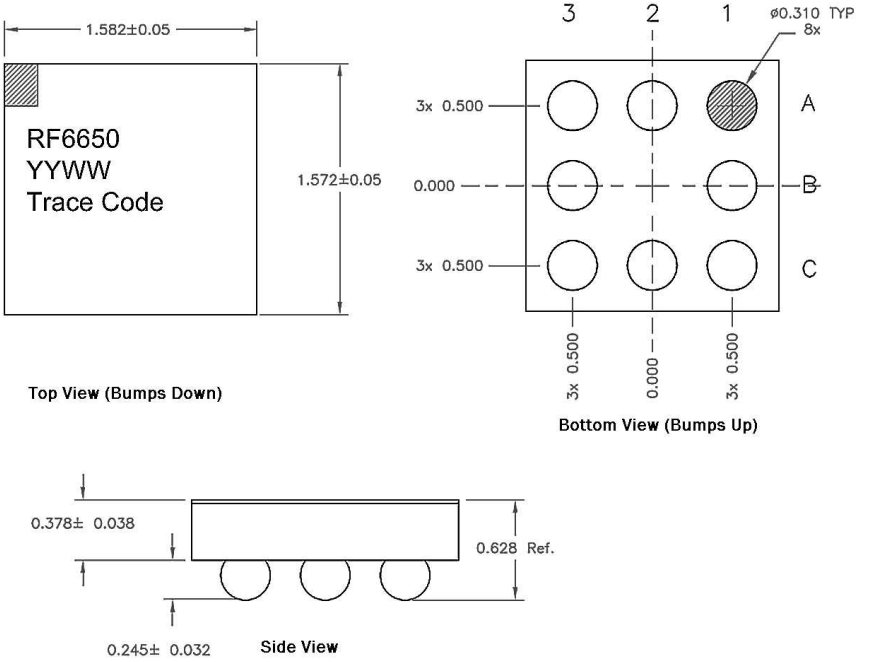
Evaluation Board Layout

Board size: 2.2" x 2.0"
Board thickness: 0.062", Board material: FR4, Multilayer



Package Drawing



Notes:

1. Shaded area represents Pin 1 location.
2. YY indicates year, WW indicates work week, and Trace Code is a sequential number assigned at device assembly.

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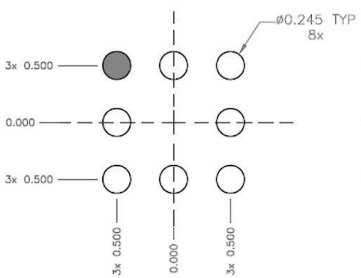
PCB Design Requirements

PCB Surface Finish

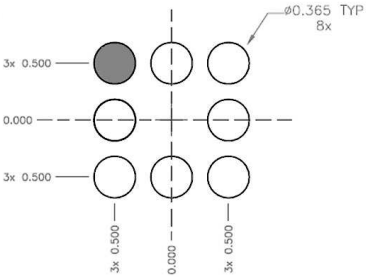
(The PCB surface finish used for RFMD's qualification process is electroless nickel, immersion gold. Typical thickness is 3 inch to 8 inch gold over 180 inch nickel.

PCB Land Pattern Recommendation

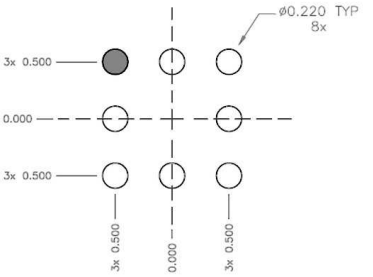
PCB land patterns for RFMD components are based on IPC-7351 standards and RFMD empirical data. The pad pattern shown has been developed and tested for optimized assembly at RFMD. The PCB land pattern has been developed to accommodate lead and package tolerances. Since surface mount processes vary from company to company, careful process development is recommended.



PCB Metal Land Pattern



PCB Solder Mask Pattern



PCB Stencil Pattern

Notes:
1. Shaded area represents Pin 1 location.

Tape and Reel

Carrier tape basic dimensions are based on EIA 481. The pocket is designed to hold the part for shipping and loading onto SMT manufacturing equipment, while protecting the body and the solder terminals from damaging stresses. The individual pocket design can vary from vendor to vendor, but width and pitch will be consistent.

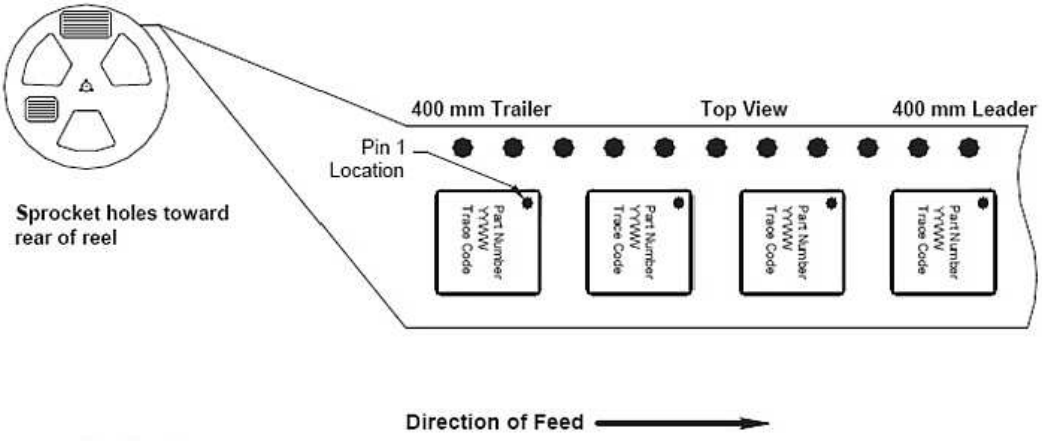
Carrier tape is wound or placed onto a shipping reel either 330mm (13 inches) in diameter or 178mm (7 inches) in diameter. The center hub design is large enough to ensure the radius formed by the carrier tape around it does not put unnecessary stress on the parts.

Prior to shipping, moisture sensitive parts (MSL level 2a-5a) are baked and placed into the pockets of the carrier tape. A cover tape is sealed over the top of the entire length of the carrier tape. The reel is sealed in a moisture barrier ESD bag with the appropriate units of desiccant and a humidity indicator card, which is placed in a cardboard shipping box. It is important to note that unused moisture sensitive parts need to be resealed in the moisture barrier bag. If the reels exceed the exposure limit and need to be rebaked, most carrier tape and shipping reels are not rated as bakeable at 125°C. If baking is required, devices may be baked according to section 4, table 4-1, of Joint Industry Standard IPC/JEDEC J-STD-033.

The table below provides information for carrier tape and reels used for shipping the devices described in this document.

Tape and Reel

RFMD Part Number	Reel Diameter Inch (mm)	Hub Diameter Inch (mm)	Width (mm)	Pocket Pitch (mm)	Feed	Units per Reel
RF6650TR7	7 (178)	2.4 (61)	8	4	Single	2500



Notes:
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Material Declaration

RFMD Part Number	Unit Mass in Grams (Average)	Breakdown of Component (e.g. Filter, Resistor, Connector	Material Name (e.g. Copper, Matte Tin, Alloy)	Substance Name (e.g. Cu, Au, Sn, SiO2)	CAS No.	PPM	Substance Mass (mg)
RF6650	0.003	Die	Silicon	Si	7440-21-3	608173	2.022929
Pb-free Compliant?	Yes	Polyimide	Polyimide	Polyimide	60842-76-4	8355	0.027792
RoHS Compliant?	Yes	Under Bump Metalizitaion	Titanium	Ti	7440-32-6	41	0.000136
D/C Compliance:	N/A		Copper	Cu	7440-50-8	112	0.000373
Pb Category:	e4		Nickel	Ni	7440-02-0	1615	0.005373
			Gold	Au	7440-57-5	875	0.002911
		Back-side Coating	Filled Silicone Coating	Polyethylene Terephthalate, Silicone	25038-59-9	24763	0.082369
				Silica	7631-86-9	4866	0.016187
				Epoxy Resin	Proprietary	649	0.002158
				Acrylic Resin	Proprietary	649	0.002158
				Carbon Black	7440-44-0	324	0.001079
		Lead-free Solder Sphere	Tin	Sn	7440-31-5	333846	1.110452
			Silver	Ag	7440-22-4	13633	0.045348
			Copper	Cu	7440-50-8	2098	0.006977
					Total Mass (mg)		3.326

This Material Declaration is based solely on information, including analytical data, provided to RFMD by its vendors.

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