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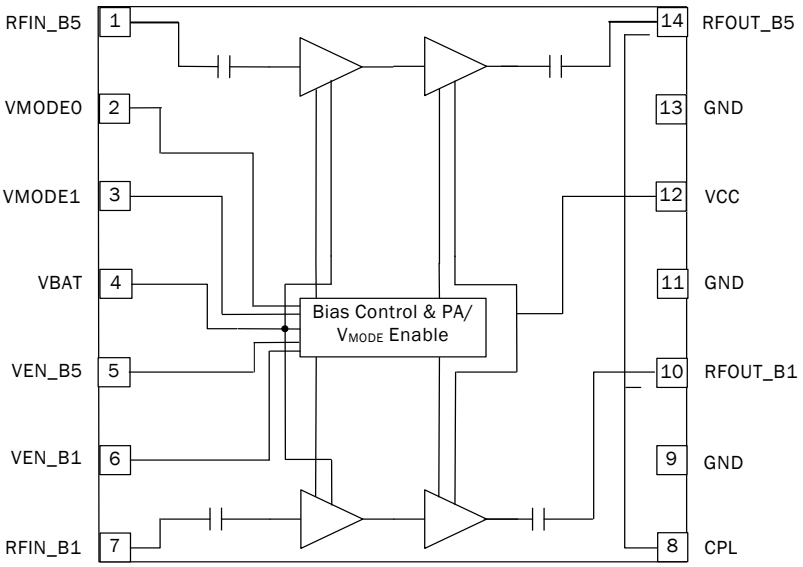
RF7205

3V W-CDMA BAND 1/5 DUAL BAND PA MODULE

Package Style: Module, 14-Pin, 4mmx5mmx1.0mm



Functional Block Diagram

Features

- Dual-Band 1/5 UMTS PA
- HSDPA and HSPA+ Compliant
- Low Voltage Positive Bias Supply (3.0V to 4.2V)
- High Efficiency Operation:
  41% at P_{OUT}=+28.0dBm (Band 1)
  41% at P_{OUT}=+28.0dBm (Band 5)
  19% at P_{OUT}=+19.0dBm (without DC/DC converter)
- Low Quiescent Current in Low Power Mode: 16mA
- Internal Voltage Regulator Eliminates the Need for External Reference Voltage (V_{REF})
- Common V_{MODE} Control Lines Between Bands
- 3-Mode Power States for Each Band with Digital Control Interface
- Supports DC/DC Converter Operation (V_{CC} Pin)
- Integrated Power Coupler
- Integrated Blocking and Collector Decoupling Caps

Applications

- Dual-Band 1/5 UMTS Handsets and Data Cards
- WCDMA/HSDPA/HSUPA/HSPA+ Wireless Handsets and Data Cards

Product Description

The RF7205 is a high-power, high-efficiency, dual-band, linear power amplifier designed for use as final amplification stages in 3V, 50Ω W-CDMA mobile cellular equipment and spread-spectrum systems. This PA is developed for UMTS Bands 1 and 5 which operates in the transmit frequency bands from 1920MHz to 1980MHz and 824MHz to 849MHz, respectively. The RF7205 uses two digital control pins to select one of three power modes to optimize performance and current drain at lower power levels. The part also has one integrated directional coupler output which eliminates the need for an external discrete coupler for each band. The RF7205 is fully HSDPA and HSPA+ compliant and is assembled on a 14-pin, 4mmx5mm laminate module.

Ordering Information

RF7205	3V W-CDMA Band 1/5 Dual Band PA Module
RF7205PCBA-410	Fully Assembled Evaluation Board

Optimum Technology Matching® Applied

☐ GaAs HBT	☐ SiGe BiCMOS	☐ GaAs pHEMT	☐ GaN HEMT
☐ GaAs MESFET	☐ Si BiCMOS	☐ Si CMOS	☐ RF MEMS
☑ InGaP HBT	☐ SiGe HBT	☐ Si BJT	☐ LDMOS

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Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage in Standby Mode	6.0	V
Supply Voltage in Idle Mode	6.0	V
Supply Voltage in Operating Mode, 50Ω Load	6.0	V
Supply Voltage, V_{BAT}	6.0	V
Control Voltage, VMODE0, VMODE1	3.5	V
Control Voltage, $V_{EN.B1}$, $V_{EN.B5}$	3.5	V
RF - Input Power	+6	dBm
RF - Output Power	+30	dBm
Output Load VSWR (Ruggedness)	10:1	
Operating Ambient Temperature	-30 to +110	°C
Storage Temperature	-55 to +150	°C

Caution! ESD sensitive device.

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability. Specified typical performance or functional operation of the device under Absolute Maximum Rating conditions is not implied.

RoHS status based on EUDirective2002/95/EC (at time of this document revision).

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Recommended Operating Conditions					
Operating Frequency Range	824		849	MHz	Band 5
	1920		1980	MHz	Band 1
V_{BAT}	+3.0	+3.4	+4.2	V	
V_{CC}	+3.0[1]	+3.4	+4.2	V	
V_{EN_B1}, V_{EN_B5}	0		0.5	V	Band disabled.
	1.4	1.8	3.0	V	Band enabled.
V_{MODE0}, V_{MODE1}	0		0.5	V	Logic “low”.
	1.5	1.8	3.0	V	Logic “high”.
Band 5 P_{OUT}					
Maximum Linear Output (HPM)	28.0[2, 3]			dBm	High Power Mode (HPM)
Maximum Linear Output (MPM)	19.0[2, 3]			dBm	Medium Power Mode (MPM)
Maximum Linear Output (LPM)	8.0[2, 3]			dBm	Low Power Mode (LPM)
Band 1 P_{OUT}					
Maximum Linear Output (HPM)	28.0[2, 3]			dBm	High Power Mode (HPM)
Maximum Linear Output (MPM)	19.0[2, 3]			dBm	Medium Power Mode (MPM)
Maximum Linear Output (LPM)	8.0[2, 3]			dBm	Low Power Mode (LPM)
Ambient Temperature	-30	+25	+85	°C	

Notes:

[1]Minimum V_{CC} for max P_{OUT} is indicated. V_{CC} down to 0.5V may be used for backed-off power when using DC/DC converter to conserve battery current.

[2]For operation at V_{CC}=+3.0V, derate P_{OUT} by 1.3dB. For V_{CC}=+3.2V, derate P_{OUT} by 0.6dB.

[3]P_{OUT} is specified for 3GPP (Rel 99) modulation. For HSDPA and HSPA+ operation, derate P_{OUT} by 1.5dB:
HSDPA Configuration: β_C=12, β_d=15, β_{hS}=24, HSPA+ Configuration: 3GPP Release 7 Subtest 1

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Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Band 1 Electrical Specifications					T=+25°C, V_{CC}=V_{BAT}=+3.4V, V_{EN}=+1.8V, Rel 99 Modulation, and 50Ω system, unless otherwise specified.
Gain	25	27	30	dB	HPM, P_{OUT}=28.0dBm
	16	19	22	dB	MPM, P_{OUT}≤19.0dBm
	13	16	19	dB	LPM, P_{OUT}≤8.0dBm
Gain Linearity		±1.0		dB	HPM, 19.0dBm≤P_{OUT}≤28.0dBm
ACLR - 5MHz Offset		-40	-36	dBc	HPM, P_{OUT}=28.0dBm
		-42	-36	dBc	MPM, P_{OUT}=19.0dBm
		-42	-36	dBc	LPM, P_{OUT}=8.0dBm
ACLR - 10MHz Offset		-53	-48	dBc	HPM, P_{OUT}=28.0dBm
		-53	-48	dBc	MPM, P_{OUT}=19.0dBm
		-53	-48	dBc	LPM, P_{OUT}=8.0dBm
PAE Without DC/DC Converter	36	41	48	%	HPM, P_{OUT}=28.0dBm
	15	19	25	%	MPM, P_{OUT}=19.0dBm
	3.5	4.7	7	%	LPM, P_{OUT}=8.0dBm
Current Drain	386	450	515	mA	HPM, P_{OUT}=28.0dBm
	93	120	155	mA	MPM, P_{OUT}=19.0dBm
	26	39	53	mA	LPM, P_{OUT}=8.0dBm
Quiescent Current	45	75	95	mA	HPM, DC only
	13	20	32	mA	MPM, DC only
	10	16	27	mA	LPM, DC only
Enable Current (I_{EN_B1})		0.3	1.0	mA	Source or sink current. V_{EN}=1.8V.
Mode Current (I_{MODE0}, I_{MODE1})		0.3	1.0	mA	Source or sink current. V_{MODE0}, V_{MODE1}=1.8V.
Leakage Current		5	15	µA	DC only. V_{CC}=V_{BAT}=4.2V, V_{EN_B1}=V_{EN_B5}=V_{MODE0}=V_{MODE1}=0.5V.
Noise Power in Receive Band		-140		dBm/Hz	All power modes, measured at duplex offset frequency (FTX+190MHz). Rx: 2110MHz to 2170MHz, P_{OUT}≤28.0dBm
Input Impedance		1.7:1		VSWR	No ext. matching, P_{OUT}≤28dBm, all modes.
Harmonic, 2FO		-25	-15	dBm	P_{OUT}≤28.0dBm, all power modes.
Harmonic, 3FO		-30		dBm	P_{OUT}≤28.0dBm, all power modes
Spurious Output Level			-70	dBc	All spurious, P_{OUT}≤28dBm, all conditions, load VSWR≤6:1.
Insertion Phase Shift	-25	±10	+25	°	Phase change at 19dBm when switching from HPM to MPM and MPM to LPM at 8dBm.
DC Enable Time			10	µS	DC only. Time from V_{EN}=high to stable idle current (90% of steady state value).
RF Rise/Fall Time			6	µS	P_{OUT}≤28.0dBm, all modes. 90% of target, DC settled prior to RF.
Coupling Factor		20		dB	P_{OUT}≤28.0dBm, all modes.
Coupling Accuracy - Temp/Voltage	-0.5		+0.5	dB	P_{OUT}≤28dBm, all modes. -30°C≤T≤85°C, 3.0V≤V_{CC} & V_{BAT}≤4.2V, referenced to 25°C, 3.4V conditions.
Coupling Accuracy - VSWR		±0.3		dB	P_{OUT}≤28dBm, all modes, load VSWR=2:1, ±0.3dB accuracy corresponds to 19dB directivity.

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Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Band 5 Electrical Specifications					T=+25°C, V_{CC}=V_{BAT}=+3.4V, V_{EN}=+1.8V, Rel 99 Modulation, and 50Ω system, unless otherwise specified.
Gain	26	28	31	dB	HPM, P_{OUT}=28.0dBm
	17	20	24	dB	MPM, P_{OUT}≤19.0dBm
	14	17	20	dB	LPM, P_{OUT}≤8.0dBm
Gain Linearity		±1.0		dB	HPM, 19.0dBm≤P_{OUT}≤28.0dBm
ACLR - 5MHz Offset		-40	-36	dBc	HPM, P_{OUT}=28.0dBm
		-42	-36	dBc	MPM, P_{OUT}=19.0dBm
		-42	-36	dBc	LPM, P_{OUT}=8.0dBm
ACLR - 10MHz Offset		-53	-48	dBc	HPM, P_{OUT}=28.0dBm
		-53	-48	dBc	MPM, P_{OUT}=19.0dBm
		-53	-48	dBc	LPM, P_{OUT}=8.0dBm
PAE Without DC/DC Converter	36	41	48	%	HPM, P_{OUT}=28.0dBm
	15	19	25	%	MPM, P_{OUT}=19.0dBm
	3.5	4.7	7	%	LPM, P_{OUT}=8.0dBm
Current Drain	386	450	515	mA	HPM, P_{OUT}=28.0dBm
	93	120	155	mA	MPM, P_{OUT}=19.0dBm
	26	39	53	mA	LPM, P_{OUT}=8.0dBm
Quiescent Current	40	75	95	mA	HPM, DC only
	15	20	40	mA	MPM, DC only
	10	16	37	mA	LPM, DC only
Enable Current (I_{EN_B5})		0.3	1.0	mA	Source or sink current. V_{EN}=1.8V.
Mode Current (I_{MODE0}, I_{MODE1})		0.3	1.0	mA	Source or sink current. V_{MODE0}, V_{MODE1}=1.8V.
Leakage Current		5	15	µA	DC only. V_{CC}=V_{BAT}=4.2V, V_{EN_B1}=V_{EN_B5}=V_{MODE0}=V_{MODE1}=0.5V.
Noise Power in Receive Band		-135		dBm/Hz	All modes, measured at duplex offset frequency (FTX+45MHz). Rx: 869MHz to 894MHz, P_{OUT}≤28.0dBm
Input Impedance		1.7:1		VSWR	No ext. matching, P_{OUT}≤28.0dBm, all modes.
Harmonic, 2FO		-15	-10	dBm	P_{OUT}≤28.0dBm, all power modes.
Harmonic, 3FO		-20		dBm	P_{OUT}≤28.0dBm, all power modes
Spurious Output Level			-70	dBc	All spurious, P_{OUT}≤28.0dBm, all conditions, load VSWR≤6:1.
Insertion Phase Shift	-25	±20	+25	°	Phase change at 19dBm when switching from HPM to MPM and MPM to LPM at 8dBm.
DC Enable Time			10	µS	DC only. Time from V_{EN}=high to stable idle current (90% of steady state value).
RF Rise/Fall Time			6	µS	P_{OUT}≤28.0dBm, all modes. 90% of target, DC settled prior to RF.
Coupling Factor		-22		dB	P_{OUT}≤28.0dBm, all modes.
Coupling Accuracy - Temp/Voltage	-0.5		+0.5	dB	P_{OUT}≤28.0dBm, all modes. -30°C≤T≤85°C, 3.0V≤V_{CC} & V_{BAT}≤4.2V, referenced to 25°C, 3.4V conditions.
Coupling Accuracy - VSWR		±0.3		dB	P_{OUT}≤28.0dBm, all modes, load VSWR=2:1, ±0.3dB accuracy corresponds to 19dB directivity.

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Pin	Function	Description
1	RFIN_B5	Band 5 RF input internally matched to 50Ω and DC blocked.
2	VMODE0	Digital control input for power mode selection (see operating modes truth table).
3	VMODE1	Digital control input for power mode selection (see operating modes truth table).
4	VBAT	Supply voltage for the first stage amplifier and bias circuitry.
5	VEN_B5	Band 5 digital control for PA enable and disable (see operating modes truth table).
6	VEN_B1	Band 1 digital control for PA enable and disable (see operating modes truth table).
7	RFIN_B1	Band 1 RF input internally matched to 50Ω and DC blocked.
8	CPL	Coupler output for both bands 1 and 5.
9	GND	This pin must be grounded.
10	RFOUT_B1	Band 1 RF output internally matched to 50Ω and DC blocked.
11	GND	This pin must be grounded.
12	VCC	Supply voltage for the second stage amplifier.
13	GND	This pin must be grounded.
14	RFOUT_B5	Band 5 RF output internally matched to 50Ω and DC blocked.
Pkg Base	GND	Ground connection. The package backside should be soldered to a topside ground pad connecting to the PCB ground plane with multiple ground vias. The pad should have a low thermal resistance and low electrical impedance to the ground plane.

Conditions/Comments	V_{EN_B1}	V_{EN_B5}	V_{MODE0}	V_{MODE1}	V_{BAT}	V_{CC}
Power down mode	Low	Low	Low	Low	3.0V to 4.2V	3.0V to 4.2V
Standby mode	Low	Low	X	X	3.0V to 4.2V	3.0V to 4.2V
B1 high power mode	High	Low	Low	Low	3.0V to 4.2V	3.0V to 4.2V
B1 medium power mode	High	Low	High	Low	3.0V to 4.2V	3.0V to 4.2V
B1 low power mode	High	Low	High	High	3.0V to 4.2V	3.0V to 4.2V
B1 optional lower V_{CC} in low power mode	High	Low	High	High	3.0V to 4.2V	≥0.5V
B5 high power mode	Low	High	Low	Low	3.0V to 4.2V	3.0V to 4.2V
B5 medium power mode	Low	High	High	Low	3.0V to 4.2V	3.0V to 4.2V
B5 low power mode	Low	High	High	High	3.0V to 4.2V	3.0V to 4.2V
B5 optional lower V_{CC} in low power mode	Low	High	High	High	3.0V to 4.2V	≥0.5V

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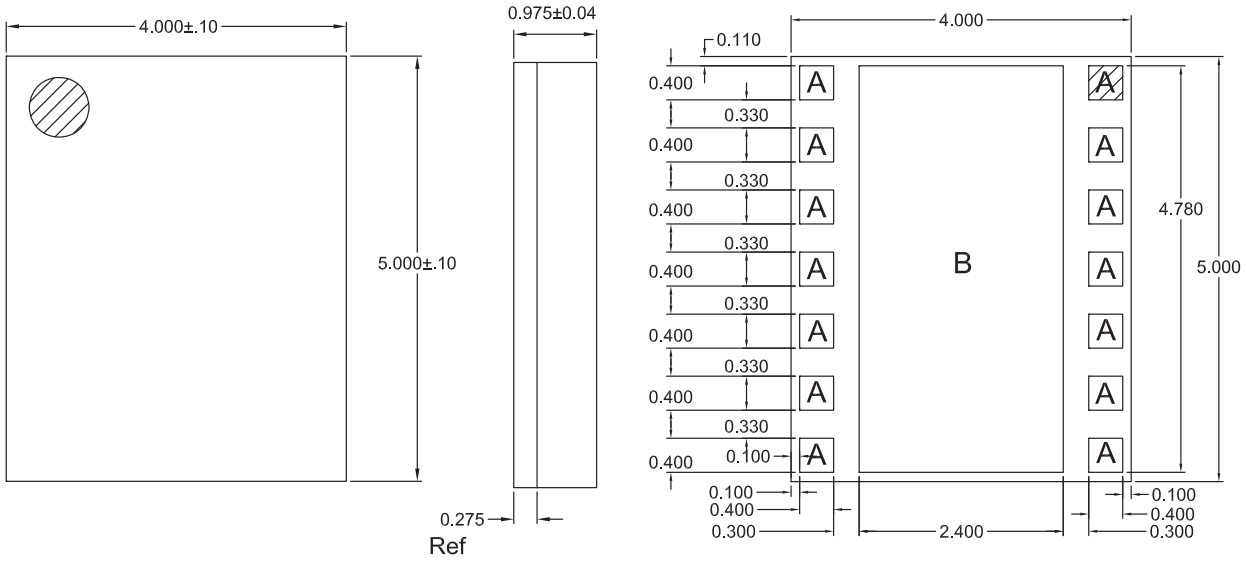
Package Drawing



Notes:
1. Shaded area represents Pin 1 location

A = 0.400 mm Sq Typ
B = 2.400 x 4.780 mm

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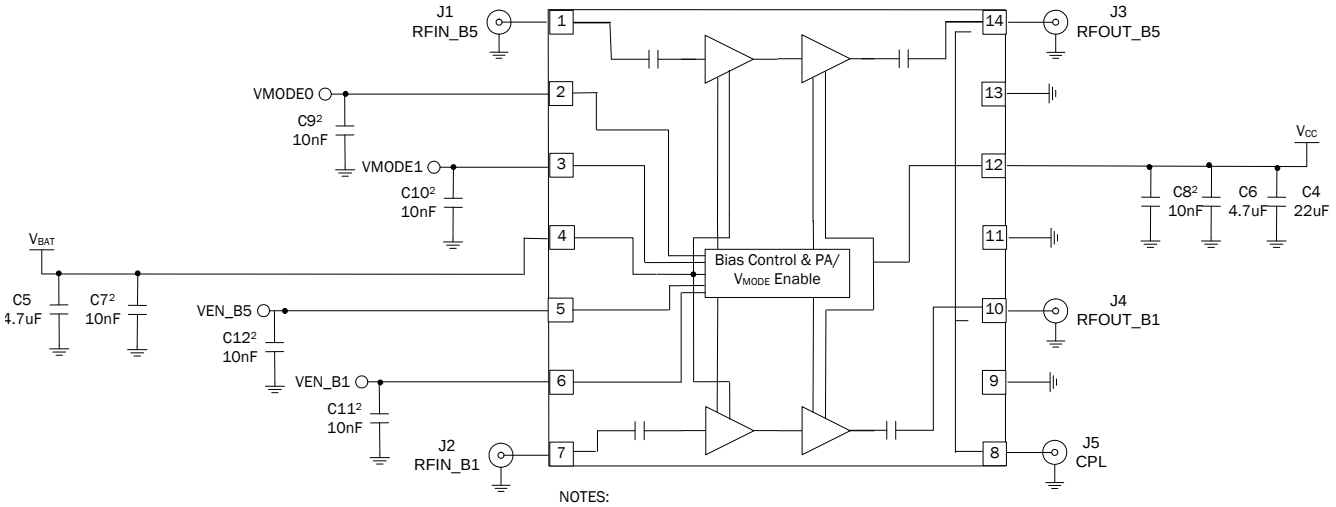
Preliminary Application Schematic



NOTES:
1. VCC and VBAT are connected is DC-DC converter is not used.
2. Place these capacitors as close to PA as possible.

PCB Design Requirements

PCB Surface Finish

The PCB surface finish used for RFMD's qualification process is electroless nickel, immersion gold. Typical thickness is 3μinch to 8μinch gold over 180μinch nickel.

PCB Land Pattern Recommendation

PCB land patterns for RFMD components are based on IPC-7351 standards and RFMD empirical data. The pad pattern shown has been developed and tested for optimized assembly at RFMD. The PCB land pattern has been developed to accommodate lead and package tolerances. Since surface mount processes vary from company to company, careful process development is recommended.

PCB Metal Land Pattern

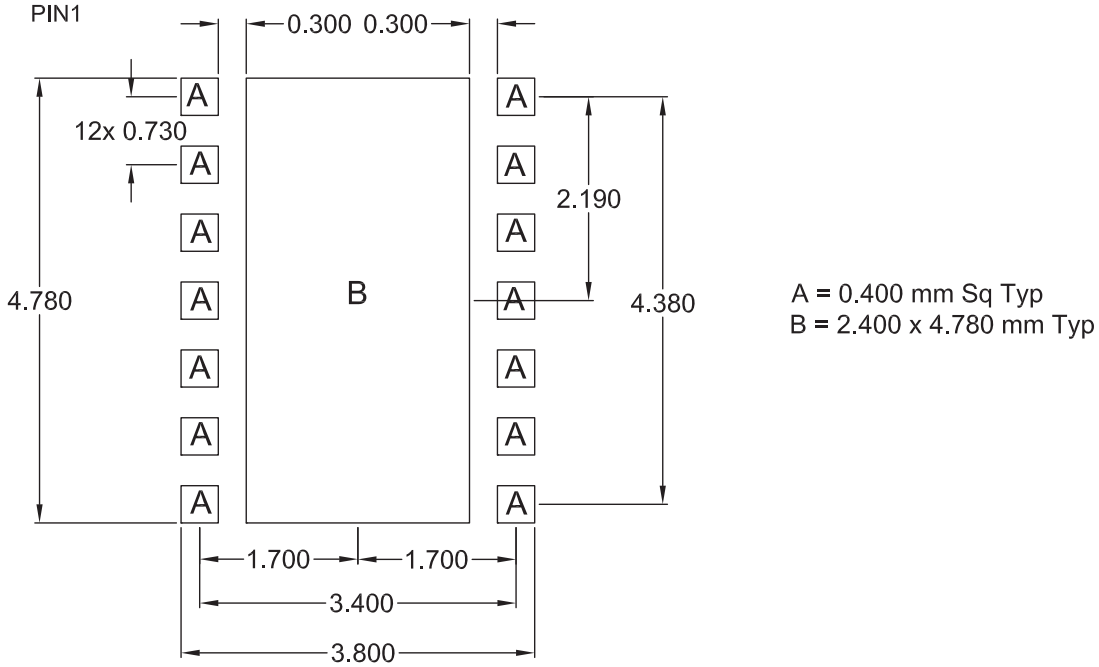


Figure 1. PCB Metal Land Pattern (Top View)

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PCB Solder Mask Pattern

Liquid Photo-Imageable (LPI) solder mask is recommended. The solder mask footprint will match what is shown for the PCB metal land pattern with a 2mil to 3mil expansion to accommodate solder mask registration clearance around all pads. The center-grounding pad shall also have a solder mask clearance. Expansion of the pads to create solder mask clearance can be provided in the master data or requested from the PCB fabrication supplier.

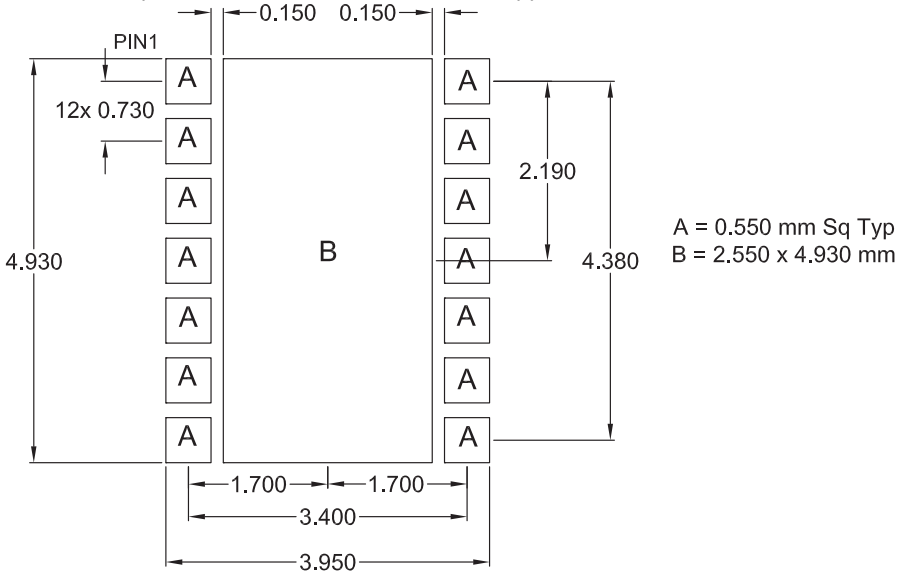

Figure 2. PCB Solder Mask Pattern (Top View)

Thermal Pad and Via Design

The PCB land pattern has been designed with a thermal pad that matches the die paddle size on the bottom of the device.

Thermal vias are required in the PCB layout to effectively conduct heat away from the package. The via pattern has been designed to address thermal, power dissipation and electrical requirements of the device as well as accommodating routing strategies.

The via pattern used for the RFMD qualification is based on thru-hole vias with 0.203mm to 0.330mm finished hole size on a 0.5mm to 1.2mm grid pattern with 0.025mm plating on via walls. If micro vias are used in a design, it is suggested that the quantity of vias be increased by a 4:1 ratio to achieve similar results.

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