

RF Power Field Effect Transistor

N-Channel Enhancement-Mode Lateral MOSFET

Designed for GSM and EDGE base station applications with frequencies from 1800 to 2000 MHz. Suitable for FM, TDMA, CDMA and multicarrier amplifier applications.

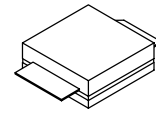
- Typical GSM Performance:
Power Gain - 14 dB (Typ) @ 30 Watts
Efficiency - 50% (Typ) @ 30 Watts
- Capable of Handling 5:1 VSWR, @ 26 Vdc, 30 Watts CW Output Power

Features

- Internally Matched for Ease of Use
- High Gain, High Efficiency and High Linearity
- Integrated ESD Protection
- Designed for Maximum Gain and Insertion Phase Flatness
- Low Gold Plating Thickness on Leads, 40μm Nominal.
- RoHS Compliant
- In Tape and Reel. R3 Suffix = 250 Units per 32 mm, 13 inch Reel.

MRF18030ALSR3

**1805-1880 MHz, 30 W, 26 V
GSM/GSM EDGE
LATERAL N-CHANNEL
RF POWER MOSFET**



**CASE 465F-04, STYLE 1
NI-400S**

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain-Source Voltage	V _{DSS}	-0.5, +65	Vdc
Gate-Source Voltage	V _{GS}	-0.5, +15	Vdc
Total Device Dissipation @ T _C = 25°C Derate above 25°C	P _D	83.3 0.48	W W/°C
Storage Temperature Range	T _{stg}	- 65 to +150	°C
Case Operating Temperature	T _C	150	°C
Operating Junction Temperature	T _J	200	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case	R _{θJC}	2.1	°C/W

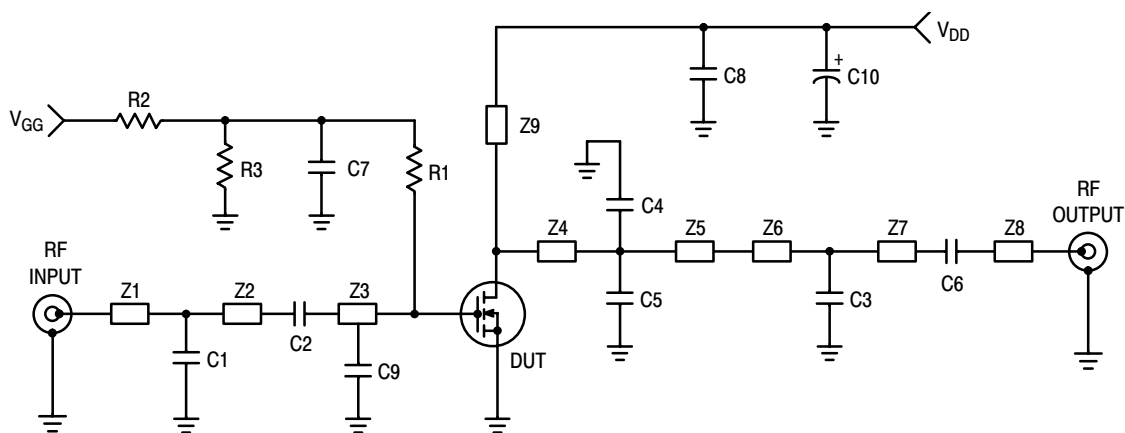
Table 3. ESD Protection Characteristics

Test Conditions	Class
Human Body Model	2 (Minimum)
Machine Model	M3 (Minimum)

Table 4. Electrical Characteristics ($T_C = 25^\circ\text{C}$, 50 ohm system unless otherwise noted)

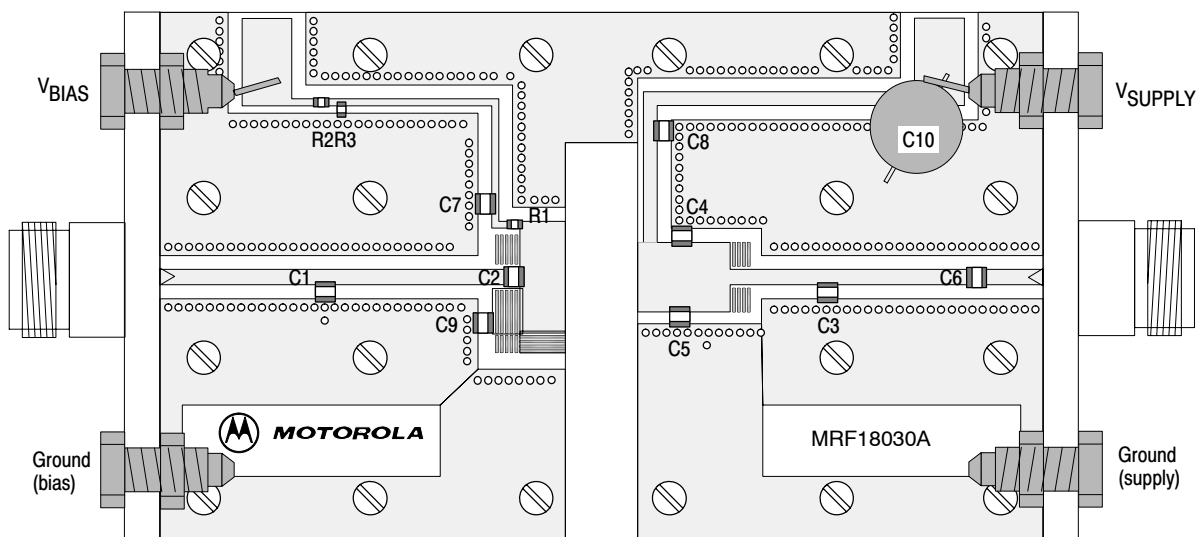
Characteristic	Symbol	Min	Typ	Max	Unit
Off Characteristics					
Drain-Source Breakdown Voltage ($V_{GS} = 0\text{ Vdc}$, $I_D = 20\text{ }\mu\text{Adc}$)	$V_{(BR)DSS}$	65	—	—	Vdc
Zero Gate Voltage Drain Current ($V_{DS} = 26\text{ Vdc}$, $V_{GS} = 0\text{ Vdc}$)	I_{DSS}	—	—	1	μAdc
Gate-Source Leakage Current ($V_{GS} = 5\text{ Vdc}$, $V_{DS} = 0\text{ Vdc}$)	I_{GSS}	—	—	1	μAdc
On Characteristics					
Gate Threshold Voltage ($V_{DS} = 10\text{ Vdc}$, $I_D = 100\text{ }\mu\text{Adc}$)	$V_{GS(th)}$	2	3	4	Vdc
Gate Quiescent Voltage ($V_{DS} = 26\text{ Vdc}$, $I_D = 250\text{ mAdc}$)	$V_{GS(Q)}$	2	3.9	4.5	Vdc
Drain-Source On-Voltage ($V_{GS} = 10\text{ Vdc}$, $I_D = 1\text{ Adc}$)	$V_{DS(on)}$	—	0.29	0.4	Vdc
Forward Transconductance ($V_{DS} = 10\text{ Vdc}$, $I_D = 1\text{ Adc}$)	g_{fs}	—	2	—	S
Dynamic Characteristics					
Reverse Transfer Capacitance ⁽¹⁾ ($V_{DS} = 26\text{ Vdc} \pm 30\text{ mV(rms)ac}$ @ 1 MHz, $V_{GS} = 0\text{ Vdc}$)	C_{rss}	—	1.3	—	pF
Functional Tests (In Freescale Test Fixture) ⁽²⁾					
Output Power, 1 dB Compression Point ($V_{DD} = 26\text{ Vdc}$, $I_{DQ} = 250\text{ mA}$, $f = 1805\text{ MHz}$)	P1dB	27	30	—	W
Common-Source Amplifier Power Gain @ 30 W ($V_{DD} = 26\text{ Vdc}$, $I_{DQ} = 250\text{ mA}$, $f = 1805\text{ MHz}$)	G_{ps}	13	14	—	dB
Drain Efficiency @ 30 W ($V_{DD} = 26\text{ Vdc}$, $I_{DQ} = 250\text{ mA}$, $f = 1805\text{ MHz}$)	η	46.5	50	—	%
Input Return Loss @ 30 W ($V_{DD} = 26\text{ Vdc}$, $I_{DQ} = 250\text{ mA}$, $f = 1805\text{ MHz}$)	IRL	—	-12	-9	dB

1. Part internally matched both on input and output.
2. Device specifications obtained on a Production Test Fixture.



C1	1.8 pF, 100B Chip Capacitor	Z1	0.874" x 0.087" Microstrip
C2	0.8 pF, 100B Chip Capacitor	Z2	1.094" x 0.087" Microstrip
C3	1.0 pF, 100B Chip Capacitor	Z3	0.257" x 0.633" Microstrip
C4, C5	1.2 pF, 100B Chip Capacitors	Z4	0.189" x 0.394" Microstrip
C6, C7, C8	8.2 pF, 100B Chip Capacitors	Z5	0.335" x 0.394" Microstrip
C9	0.3 pF, 100B Chip Capacitor	Z6	0.484" x 0.087" Microstrip
C10	220 μ F, 63 V Electrolytic Capacitor	Z7	0.877" x 0.087" Microstrip
R1	1.0 k Ω , 1/8 W Chip Resistor (0805)	Z8	0.366" x 0.087" Microstrip
R2, R3	10 k Ω , 1/8 W Chip Resistors (0805)	Z9	$\approx$ 0.600" x 0.087" Microstrip

Figure 1. 1805 - 1880 MHz Test Fixture Schematic



Freescall has begun the transition of marking Printed Circuit Boards (PCBs) with the Freescall Semiconductor signature/logo. PCBs may have either Motorola or Freescall markings during the transition period. These changes will have no impact on form, fit or function of the current product.

Figure 2. 1805 - 1880 MHz Test Fixture Component Layout

TYPICAL CHARACTERISTICS

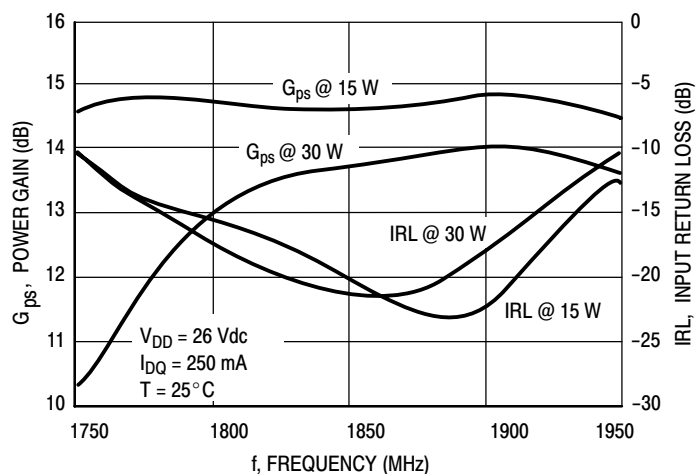


Figure 3. Wideband Gain and IRL at 30 W and 15 W Output Power

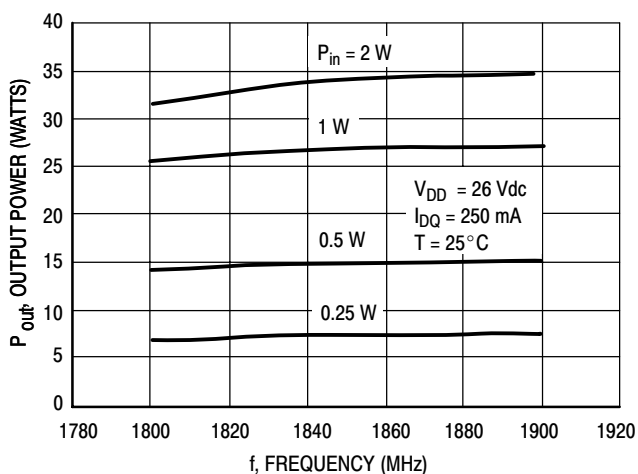


Figure 4. Output Power versus Frequency

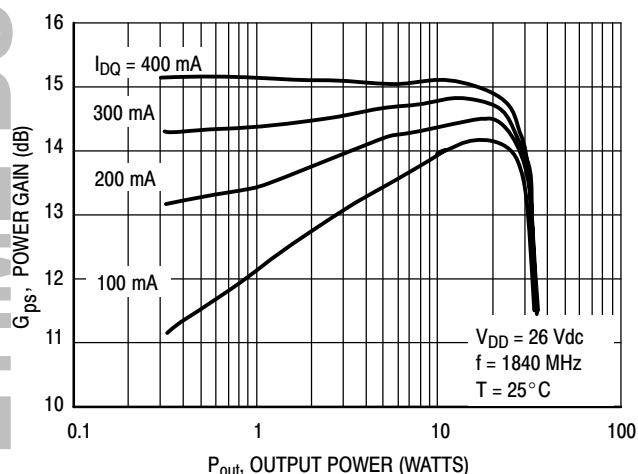


Figure 5. Power Gain versus Output Power

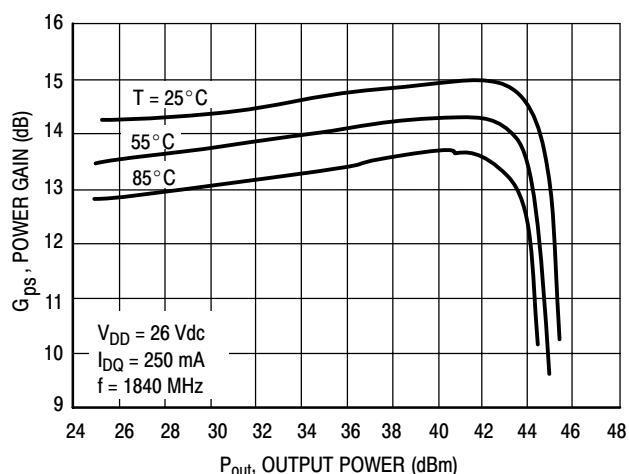


Figure 6. Power Gain versus Output Power

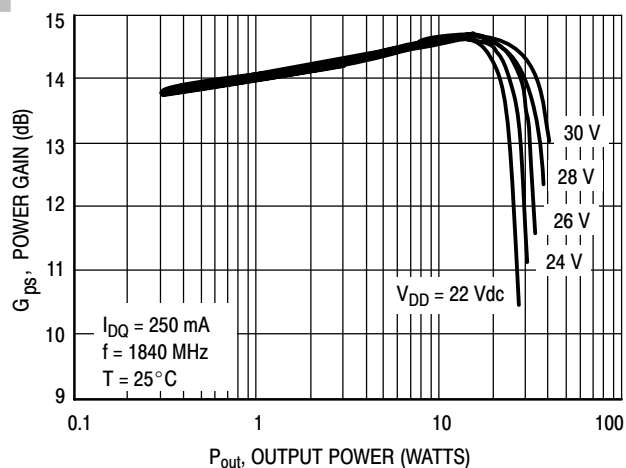


Figure 7. Power Gain versus Output Power

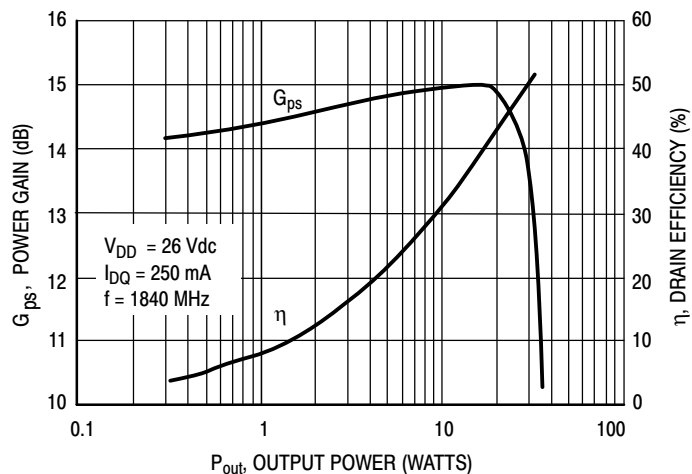
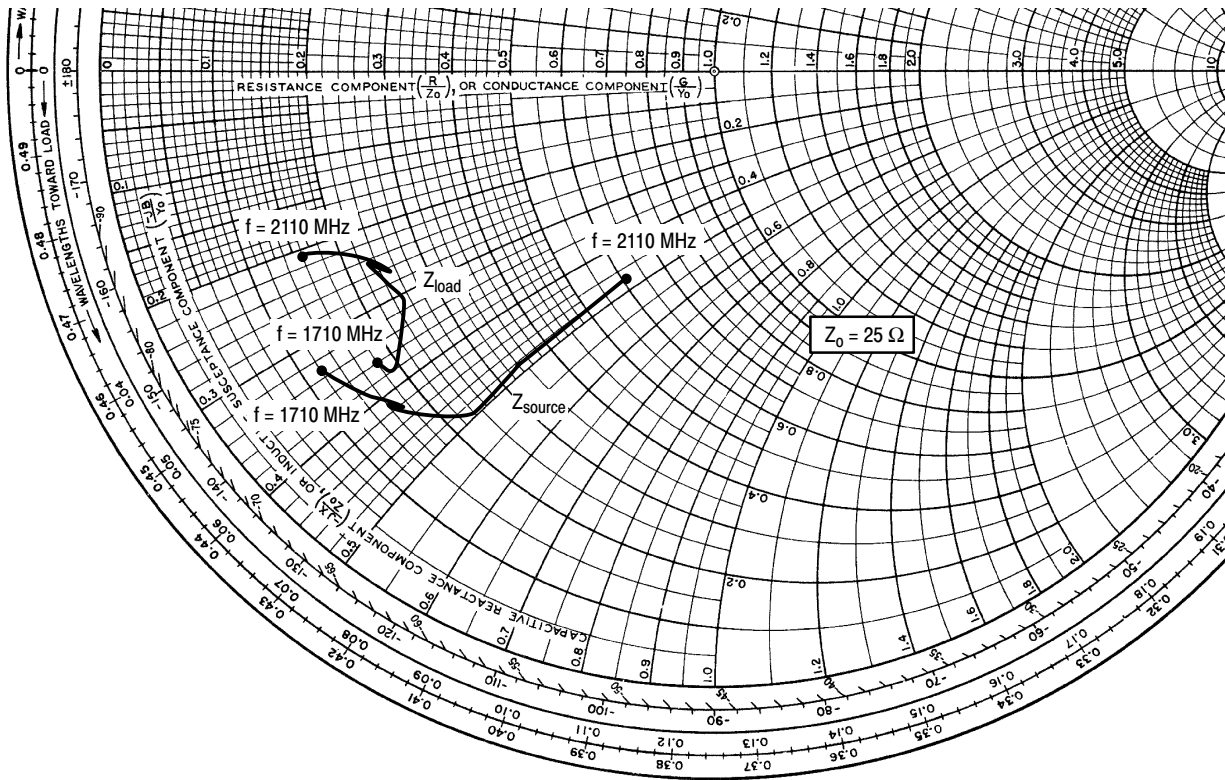


Figure 8. Power Gain and Efficiency versus Output Power



$V_{DD} = 26 \text{ V}$, $I_{DQ} = 250 \text{ mA}$, $P_{out} = 30 \text{ W (CW)}$

f MHz	Z_{source} Ω	Z_{load} Ω
1710	$2.92 - j8.24$	$4.18 - j9.06$
1785	$3.84 - j9.75$	$4.59 - j9.46$
1805	$4.15 - j10.38$	$4.98 - j9.06$
1840	$4.04 - j10.22$	$6.10 - j7.63$
1880	$6.12 - j12.29$	$5.83 - j6.89$
1960	$6.20 - j12.29$	$5.55 - j6.33$
1990	$8.61 - j12.10$	$5.93 - j6.66$
2110	$15.19 - j11.85$	$3.82 - j5.33$

Z_{source} = Test circuit impedance as measured from gate to ground.

Z_{load} = Test circuit impedance as measured from drain to ground.

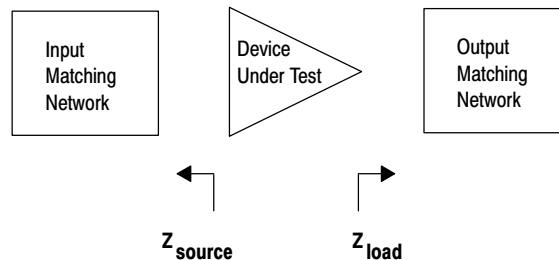
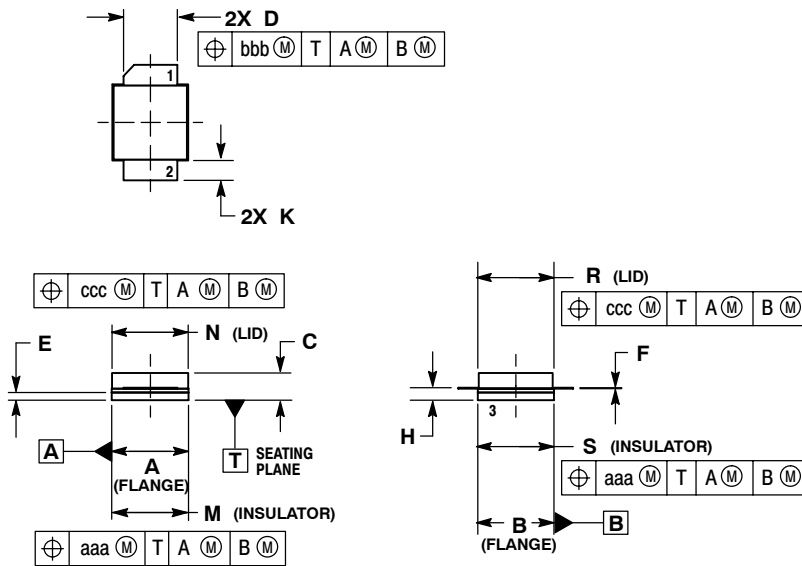


Figure 9. Series Equivalent Source and Load Impedance

PACKAGE DIMENSIONS



- NOTES:
1. CONTROLLING DIMENSION: INCH.
 2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.
 3. DIMENSION H IS MEASURED 0.030 (0.762) AWAY FROM PACKAGE BODY.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.395	.405	10.03	10.29
B	.395	.405	10.03	10.29
C	.125	.163	3.18	4.14
D	.275	.285	6.98	7.24
E	.035	.045	0.89	1.14
F	.004	.006	0.10	0.15
H	.057	.067	1.45	1.70
K	.092	.122	2.34	3.10
M	.395	.405	10.03	10.29
N	.395	.405	10.03	10.29
R	.395	.405	10.03	10.29
S	.395	.405	10.03	10.29
aaa	.005 REF		0.127 REF	
bbb	.010 REF		0.254 REF	
ccc	.015 REF		0.38 REF	

STYLE 1:
PIN 1: DRAIN
2: GATE
3: SOURCE

**CASE 465F-04
ISSUE E
NI-400S
MRF18030ALSR3**

PRODUCT DOCUMENTATION

Refer to the following documents to aid your design process.

Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
10	Oct. 2008	• Data sheet revised to reflect part status change, p. 1, including use of applicable overlay. • Modified data sheet to reflect RF Test Reduction described in Product and Process Change Notification number, PCN12779, p. 1, 2 • Added Product Documentation and Revision History, p. 7

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