Freescale Semiconductor
Technical Data

Document Number: MMG5004N
Rev. 0, 8/2006

RoHS

Heterojunction Bipolar Transistor Technology (InGaP HBT)

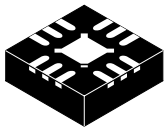
WLAN Power Amplifier

Designed for 802.11a applications with frequencies from 4900 to 5900 MHz.

- 23 dBm P1dB CW @ 5.25 GHz
- Power Gain— 24 dB Typical @ f = 5.25 GHz, Class AB
- EVM — ≤3% @ P_{out} = 18 dBM @ PAE = 10% under OFDM, 64 QAM, 54 Mbps
- High Gain, High Efficiency and High Linearity
- RoHS Compliant
- In Tape and Reel. R2 Suffix = 1,500 Units per 12 mm, 7 inch Reel.

MMG5004NR2

4.9–5.9 GHz, 24 dB, 23 dBm
802.11a WLAN POWER AMPLIFIER
InGaP HBT



CASE 1483-01
QFN 3x3

ARCHIVE INFORMATION

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Collector Supply	V_{CC}	5	V
Base Supply First Stage	V_{B1}	5	V
Base Supply Second Stage	V_{B2}	5	V
Base Supply Third Stage	V_{B3}	5	V
Detector Bias Supply	V_{BIAS}	5	V
Quiescent Current	I_{DC}	130	mA

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	64 (1)	°C/W
Case Operating Temperature Range	T_C	–40 to +85	°C
Storage Temperature Range	T_{stg}	–55 to +150	°C

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22–A114)	1A (Minimum)
Machine Model (per EIA/JESD22–A115)	A (Minimum)
Charge Device Model (per JESD22–C101)	III (Minimum)

1. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers.* Go to http://www.freescale.com/rf. Select Documentation/Application Notes – AN1955.

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Table 4. Moisture Sensitivity Level

Test Methodology	Rating	Package Peak Temperature	Unit
Per JESD 22-A113, IPC/JEDEC J-STD-020	1	260	°C

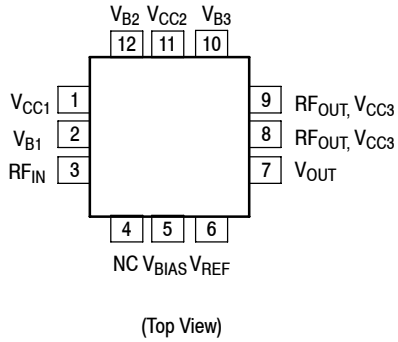
Table 5. Electrical Characteristics (T_A = 25°C unless otherwise noted.) V_{CC} = 3.3 Vdc, V_{B1}, V_{B2}, V_{B3} = 2.8 Vdc, V_{BIAS} = 3 Vdc, I_{CQ} = 105 mA, f = 5250 MHz

Characteristic	Symbol	Min	Typ	Max	Unit
Output Power at 1dB Compression, CW	P1dB	—	23	—	dBm
Power Gain (P_{out} = 18 dBm, OFDM, 64 QAM, 54 Mbps)	G_p	—	24	—	dB
Error Vector Magnitude (P_{out} = 18 dBm, OFDM, 64 QAM, 54 Mbps)	EVM	—	3	—	%
Total Current (P_{out} = 18 dBm, OFDM, 64 QAM, 54 Mbps)	I_{Ctotal}	—	200	—	mA
Quiescent Current	I_{CQ}	—	105	—	mA
Bias Control Reference Current (I_{CQ} = 105 mA)	I_{ref}	—	7	—	mA
Gain Flatness (Over 100 MHz)	G_F	—	±0.2	—	dB
Gain Variation over Temperature (-40 to 85°C)	—	—	±1	—	dB
Input Return Loss	IRL	—	-15	—	dB
Reverse Isolation	—	—	-40	—	dB
Second Harmonic (P_{out} = 18 dBm, OFDM, 64 QAM, 54 Mbps)	—	—	-50	—	dBc
Third Harmonic (P_{out} = 18 dBm, OFDM, 64 QAM, 54 Mbps)	—	—	-50	—	dBc
Ramp-On Time (10-90%)	t_{ON}	—	100	—	ns

ARCHIVE INFORMATION

Table 6. Functional Pin Description

Name	Pin Number	Description
V_{CC1}	1	Power supply for first stage amplifier.
V_{B1}	2	Bias current control voltage for the first stage. The V_{B1} pin can be combined with V_{B2} and V_{B3} into a single current control voltage (V_{BC}).
RF_{IN}	3	RF input for the power amplifier. This pin is DC−shorted to GND and AC−coupled to the transistor base of the first stage.
V_{BIAS}	5	Detector bias voltage supply.
V_{REF}	6	Detector output voltage reference. V_{out} − V_{REF} is useful for tracking detector performance over temperature.
V_{OUT}	7	Detector output voltage.
RF_{OUT}	8, 9	RF output for the power amplifier. This pin is DC−coupled and requires a DC−blocking capacitor.
V_{CC3}	8, 9	Power supply for third stage amplifier.
V_{B2}	10	Bias current control voltage for the second stage. The V_{B2} pin can be combined with V_{B1} and V_{B3} into a single current control voltage (V_{BC}).
V_{CC2}	11	Power supply for second stage amplifier.
V_{B3}	12	Bias current control voltage for third stage. The V_{B3} pin can be combined with V_{B1} and V_{B2} into a single current control voltage (V_{BC}).
GND	Center Metal	The center metal base of the QFN 3x3 package provides both DC/RF ground as well as heat sink for the power amplifier.



(Top View)

Figure 1. Pin Connections

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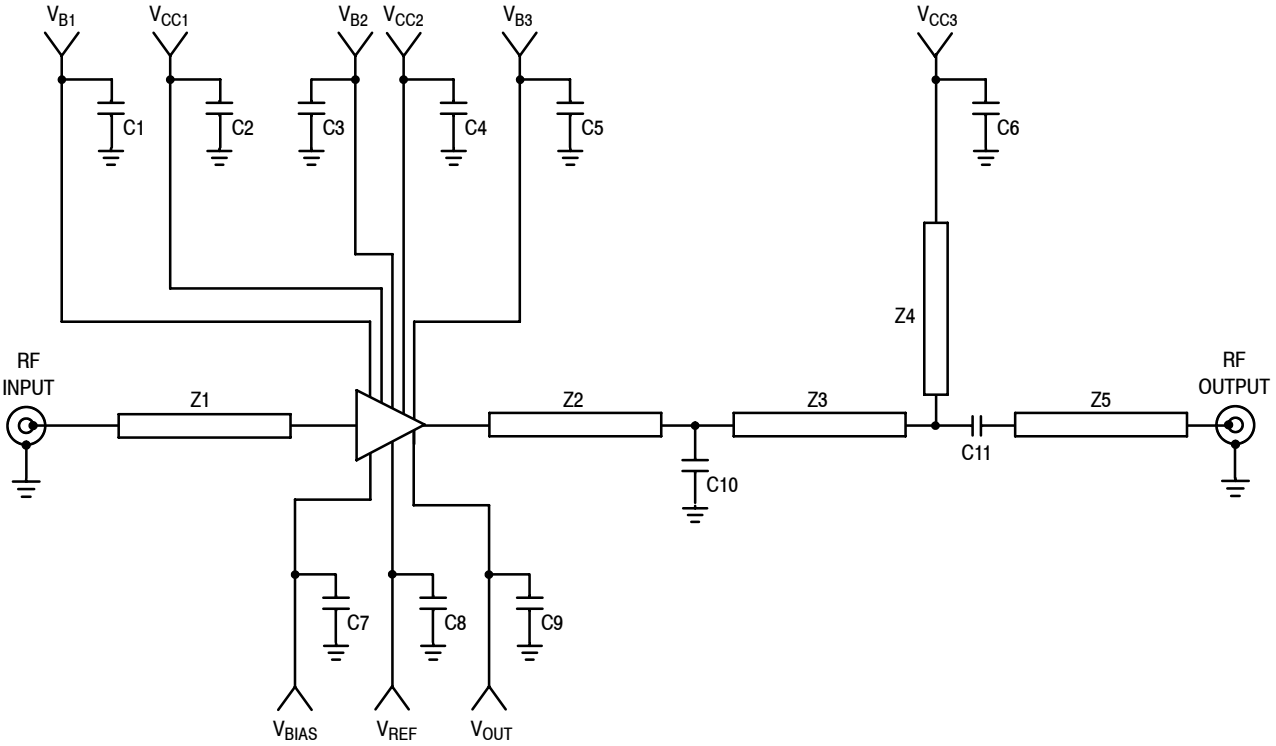

Z1	0.010″ x 0.556″ Microstrip
Z2	0.010″ x 0.405″ Microstrip
Z3	0.010″ x 0.106″ Microstrip
Z4	0.004″ x 0.330″ Microstrip
PCB	Getek ML200M, 0.005″, ε_r = 3.8

Figure 2. MMG5004NR2 Test Circuit Schematic

Table 7. MM5004NR2 Test Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
C1, C3, C5	100 pF Chip Capacitors	08055A101FAT2A	AVX
C2, C4, C6	1 μF Chip Capacitors	12065A105JAT2A	AVX
C7, C8, C9	27 pF Chip Capacitors	06035A270FAT2A	AVX
C10	0.7 pF Chip Capacitor	04025J0R788W	AVX
C11	22 pF Chip Capacitor	06035A220FAT2A	AVX

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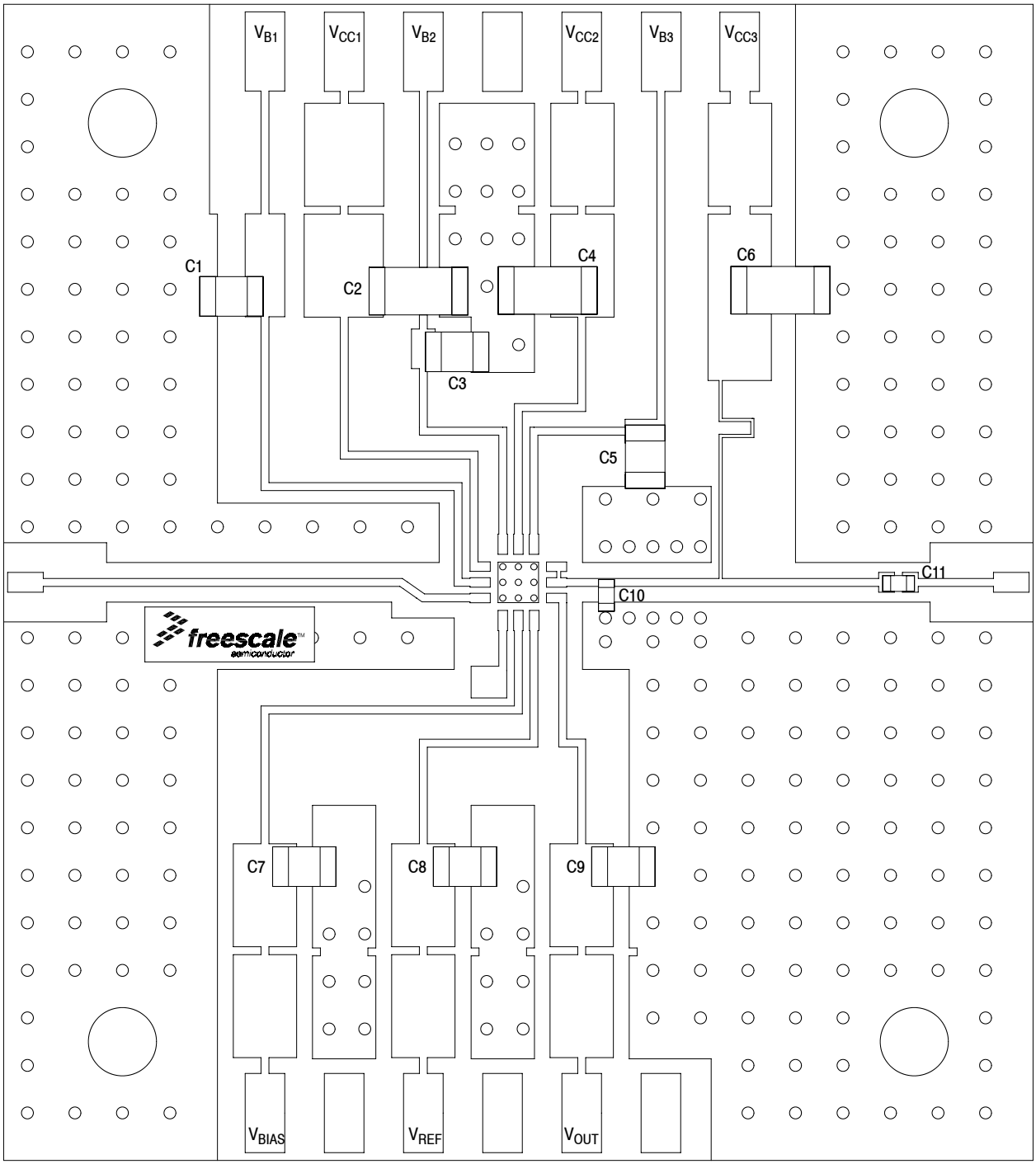


Freescale has begun the transition of marking Printed Circuit Boards (PCBs) with the Freescale Semiconductor signature/logo. PCBs may have either Motorola or Freescale markings during the transition period. These changes will have no impact on form, fit or function of the current product.

Figure 3. MMG5004NR2 Test Circuit Component Layout

TYPICAL CHARACTERISTICS

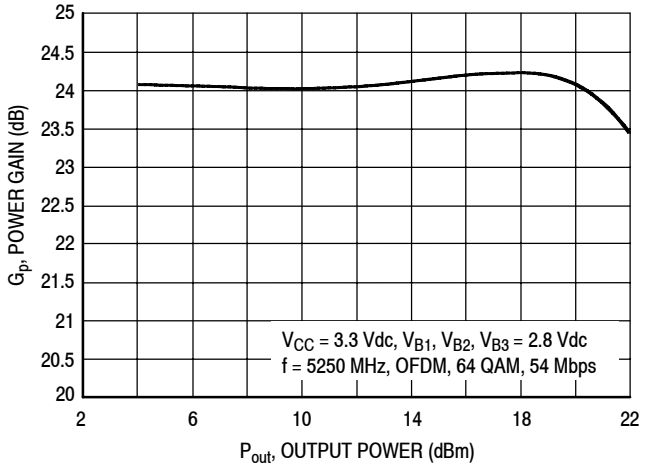


Figure 4. Power Gain versus Output Power

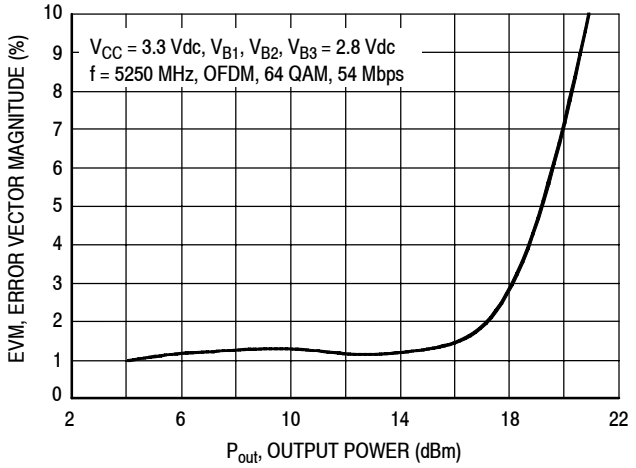


Figure 5. Error Vector Magnitude versus Output Power

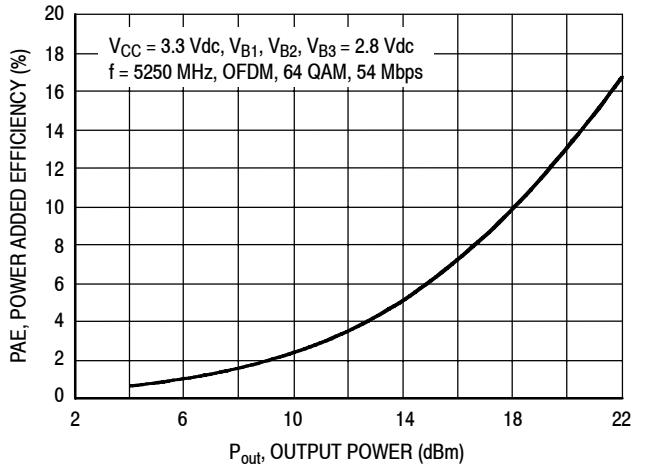


Figure 6. Power Added Efficiency versus Output Power

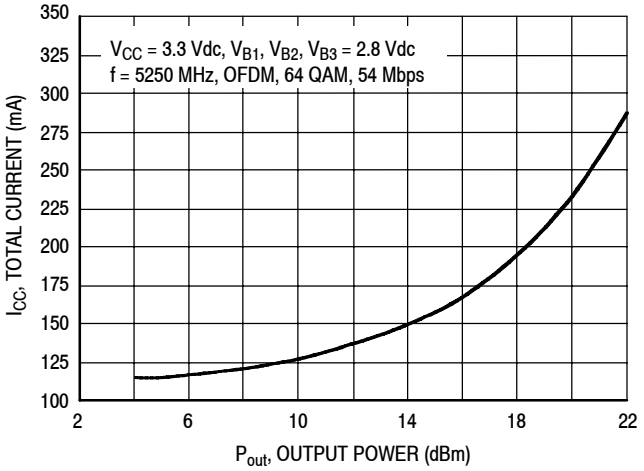


Figure 7. Total Current versus Output Power

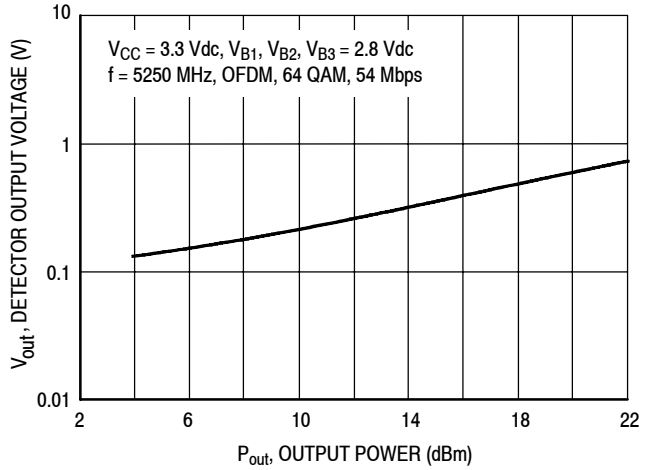


Figure 8. Detector Output Voltage versus Output Power

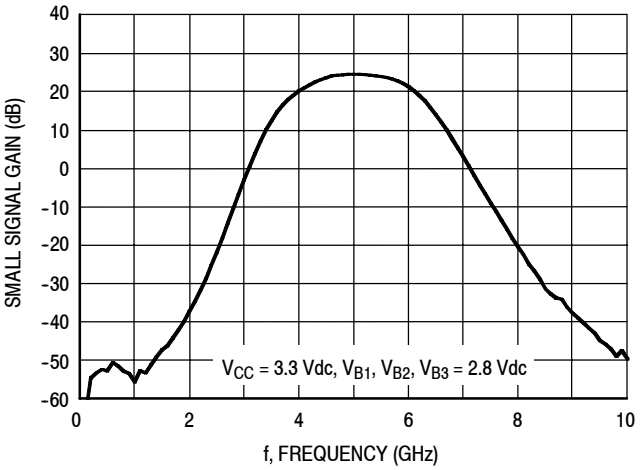


Figure 9. Small Signal Gain (S21) versus Frequency

TYPICAL CHARACTERISTICS

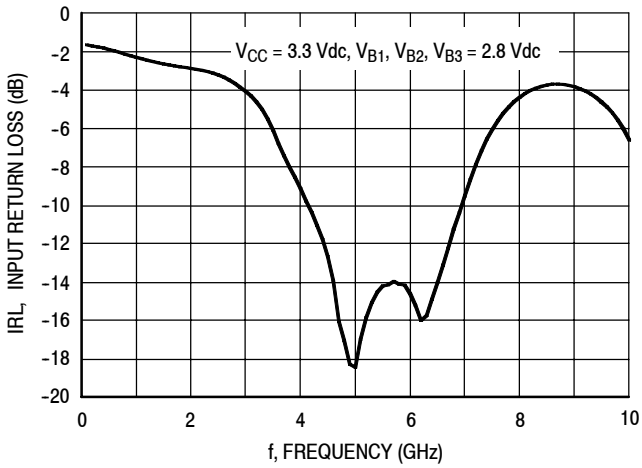


Figure 10. Input Return Loss (S11) versus Frequency

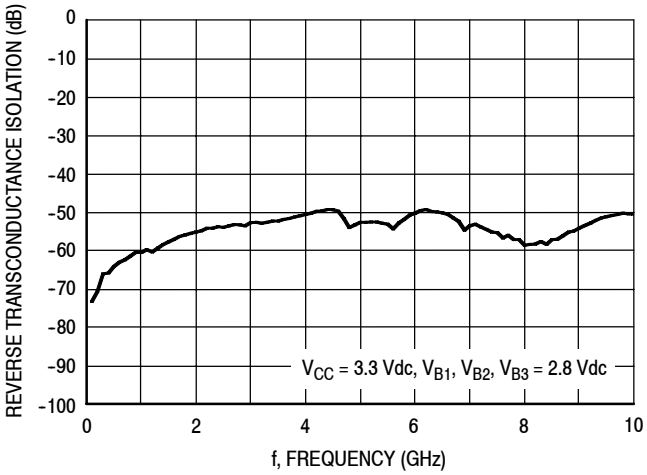


Figure 11. Reverse Transconductance Isolation (S12) versus Frequency

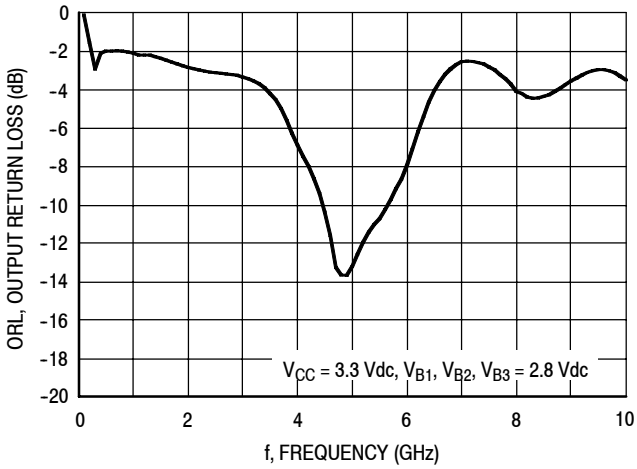
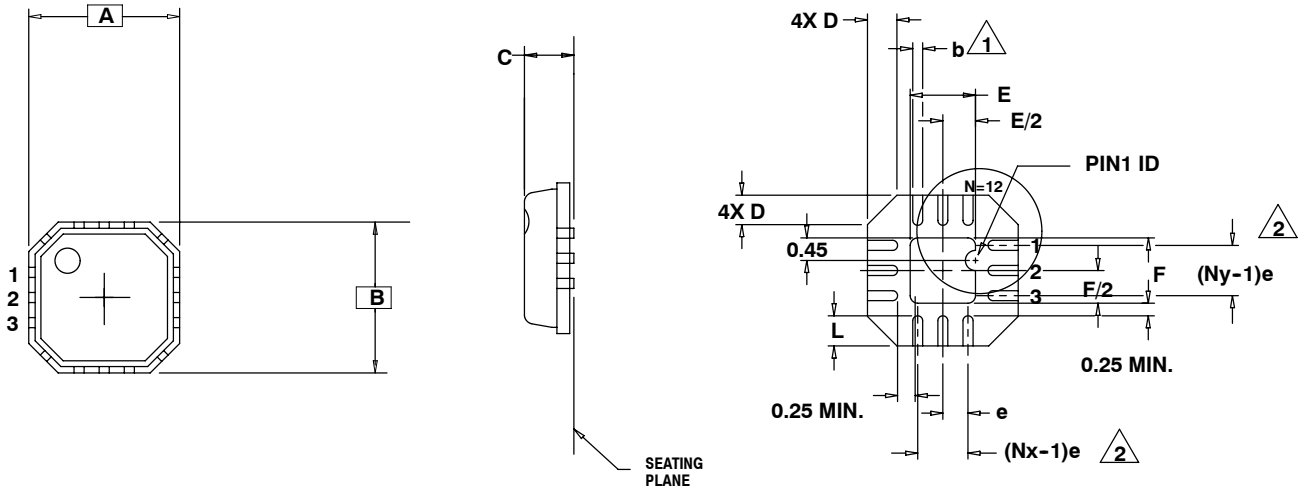


Figure 12. Output Return Loss (S22) versus Frequency



TOP VIEW

SIDE VIEW

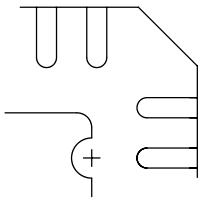
BOTTOM VIEW

NOTES:

1. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.20 AND 0.25 MM FROM TERMINAL TIP.
2. N IS THE NUMBER OF TERMINALS (12).
   Nx IS THE NUMBER OF TERMINALS IN X-DIRECTION AND
   Ny IS THE NUMBER OF TERMINALS IN Y-DIRECTION.
3. ALL DIMENSIONS ARE IN MILLIMETERS.

DIM	MIN	NOM	MAX
A		3.00 BSC	
B		3.00 BSC	
C	-	0.85	1.00
D	0.24	0.42	0.60
E		SEE EXPOSED PAD	
F		SEE EXPOSED PAD	
b	0.18	0.23	0.30
e		0.50 BSC	
Nx		3	
Ny		3	

SYMBOLS	E			F		
	MIN	NOM	MAX	MIN	NOM	MAX
EXPOSED PAD	1.15	1.30	1.45	1.15	1.30	1.45



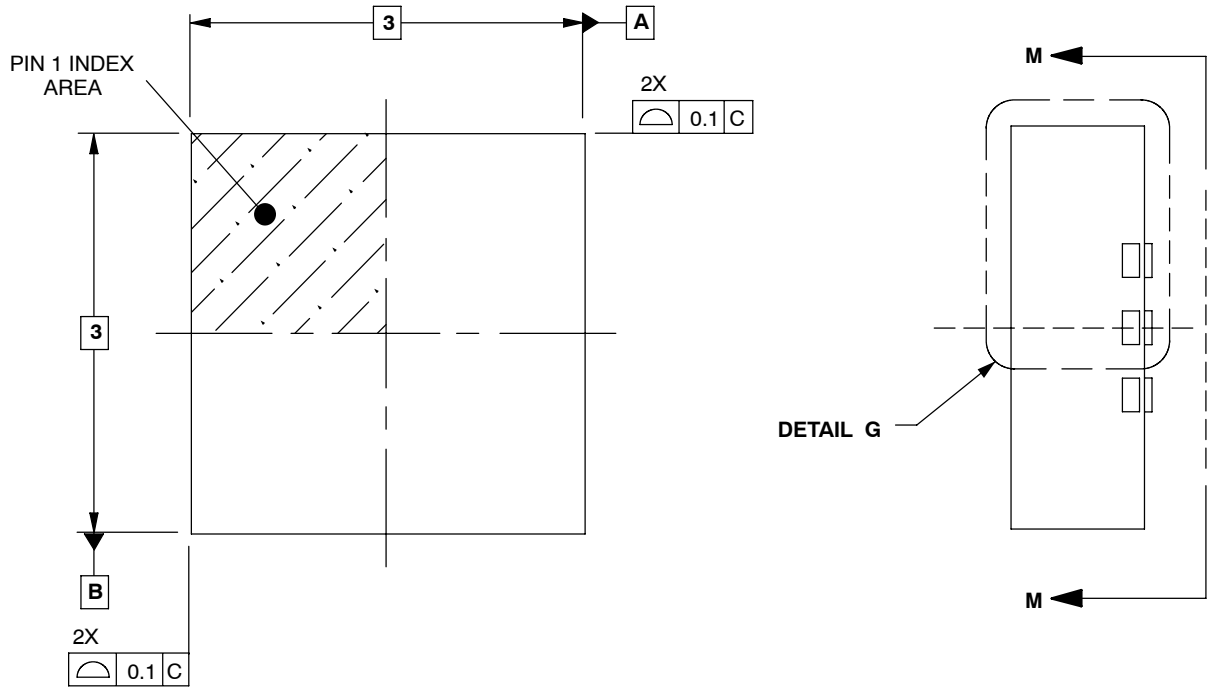
STANDARD

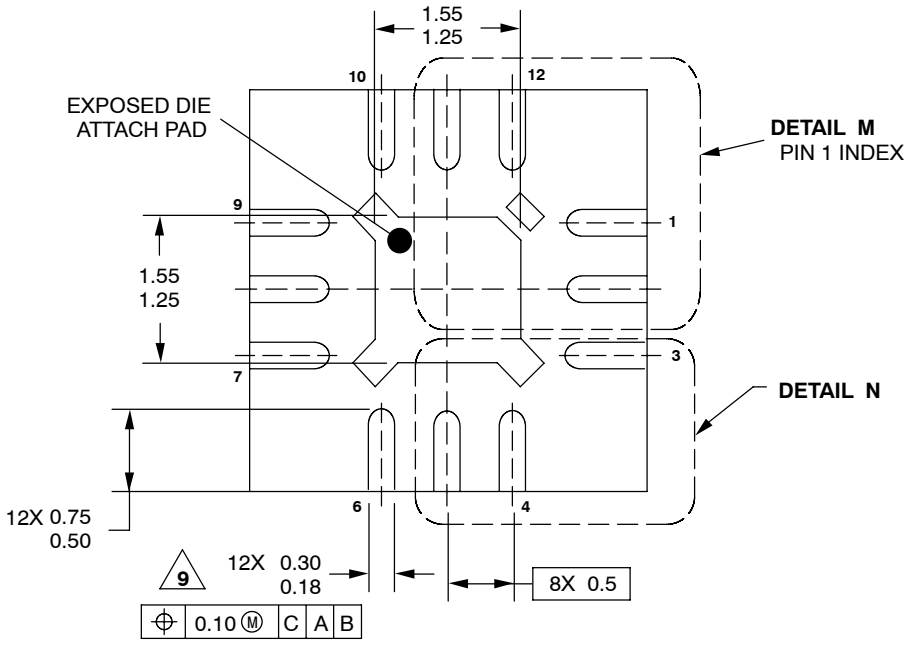
DETAIL "A" – PIN #1 ID AND TIE BAR MARK OPTION

Figure 13. MMG5004NR2 Specific Mechanical Outline Information

ARCHIVE INFORMATION

PACKAGE DIMENSIONS



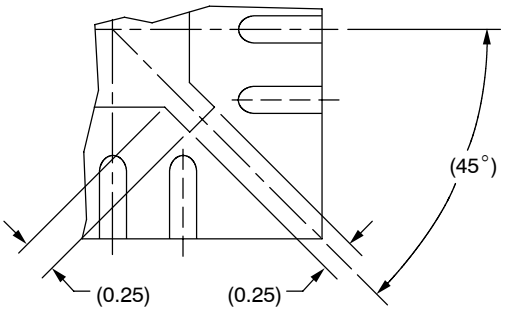


VIEW M - M

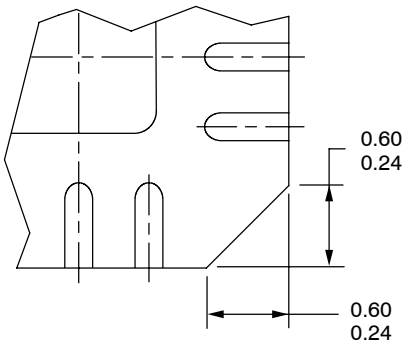
NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. THE COMPLETE JEDEC DESIGNATOR FOR THIS PACKAGE IS: HF-PQFP-N.
4. FOR ANVIL SINGULATED QFN PACKAGES, MAXIMUM DRAFT ANGLED IS 12°.
5. PACKAGE WARPAGE MAX 0.05 MM.
6. CORNER CHAMFER MAY NOT BE PRESENT. DIMENSIONS OF OPTIONAL FEATURES ARE FOR REFERENCE ONLY.
7. CORNER LEADS CAN BE USED FOR THERMAL OR GROUND AND ARE TIED TO THE DIE ATTACH PAD. THESE LEADS ARE NOT INCLUDED IN THE LEAD COUNT.
8. COPLANARITY APPLIES TO LEAD, CORNER LEADS, AND DIE ATTACH PAD.
9. THIS DIMENSION APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.20 MM AND 0.25 MM FROM TERMINAL TIP.

CASE 1483-01
ISSUE A
QFN 3x3

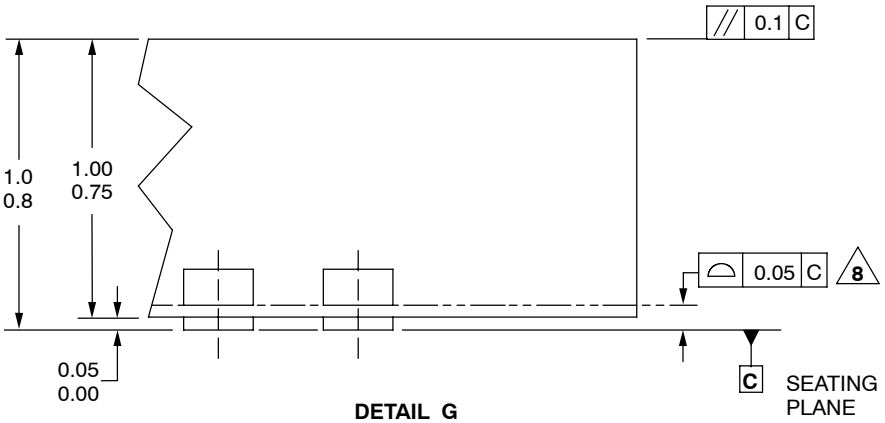
(continued)



DETAIL N
PREFERRED CORNER CONFIGURATION
6



DETAIL N
CORNER CONFIGURATION
6

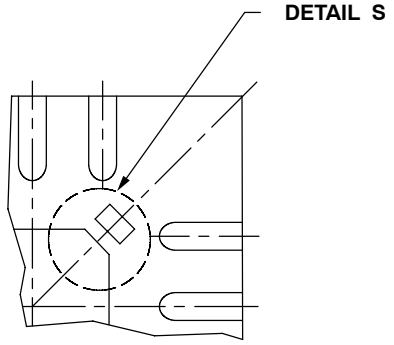


DETAIL G
VIEW ROTATED 90° CW

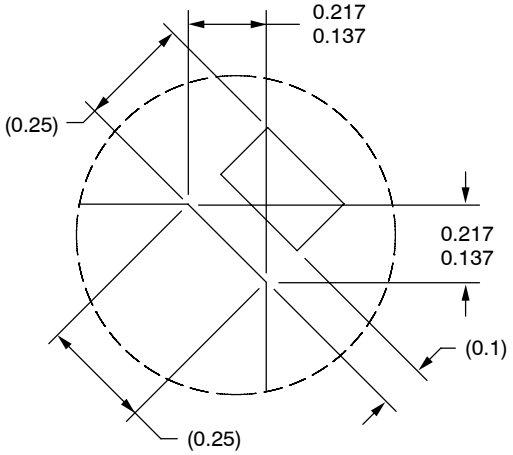
CASE 1483-01
ISSUE A
QFN 3x3

(continued)

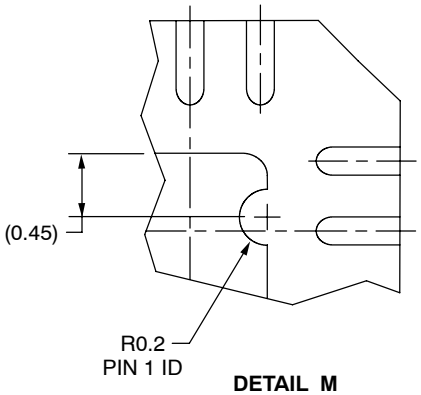
ARCHIVE INFORMATION



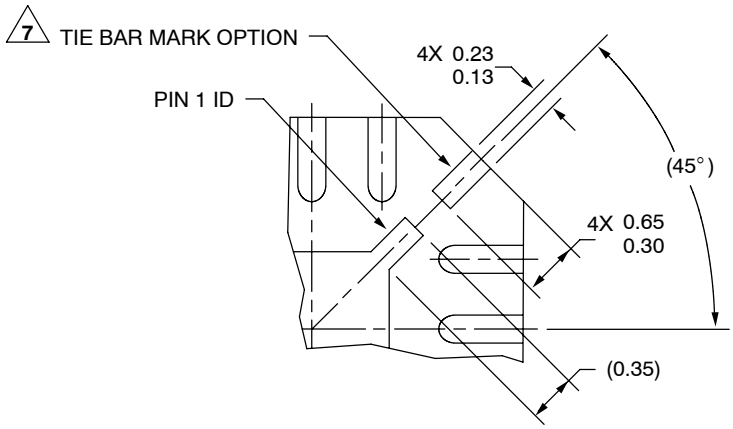
DETAIL M
PREFERRED BACKSIDE PIN 1 INDEX



DETAIL S
BACKSIDE PIN 1 INDEX



DETAIL M
BACKSIDE PIN 1 INDEX OPTION



DETAIL M
BACKSIDE PIN 1 INDEX OPTION

CASE 1483-01
ISSUE A
QFN 3x3

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