

Replaced by MMG1001NT1. N suffix indicates 260°C reflow capable. The PFP-16 package has had lead-free terminations from its initial release.

Gallium Arsenide CATV Integrated Amplifier Module

Features

- Specified for 79-, 112- and 132-Channel Loading
- Excellent Distortion Performance
- Built-in Input Diode Protection
- GaAs FET Transistor Technology
- Unconditionally Stable Under All Load Conditions
- In Tape and Reel. R2 Suffix = 1,500 Units per 16 mm, 13 inch Reel.
 T1 Suffix = 1,000 Units per 16 mm, 13 inch Reel.

Applications

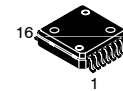
- CATV Systems Operating in the 40 to 870 MHz Frequency Range
- Input Stage Amplifier in Optical Nodes, Line Extenders and Trunk Distribution Amplifiers for CATV Systems
- Output Stage Amplifier on Applications Requiring Low Power Dissipation and High Output Performance
- Driver Amplifier in Linear General Purpose Applications

Description

- 24 Vdc Supply or 12 Vdc Supply with Bias Change, 40 to 870 MHz, CATV Integrated Forward Amplifier Module

MMG1001R2
MMG1001T1

870 MHz
19 dB GAIN
132-CHANNEL
CATV INTEGRATED AMPLIFIER
MODULE



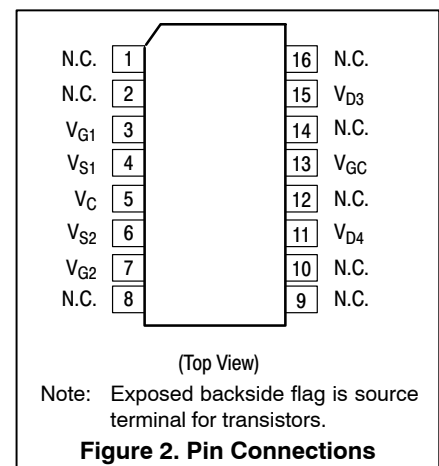
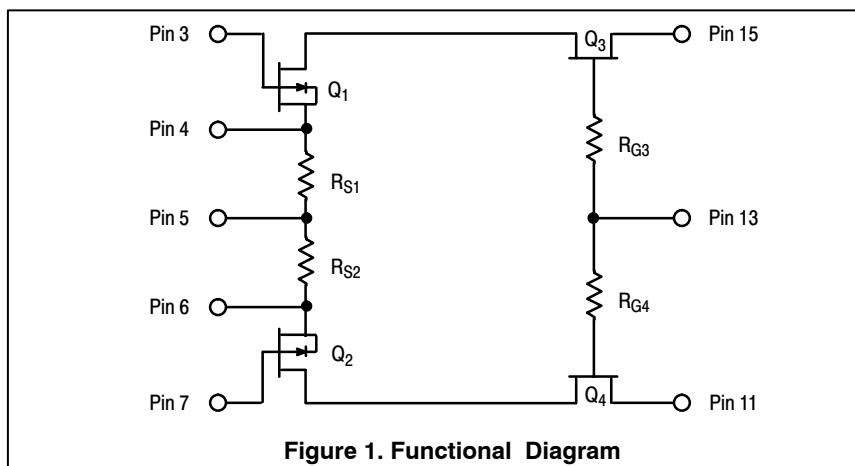
CASE 978-03
PFP-16

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
RF Voltage Input (Single Tone)	V_{in}	+65	dBmV
DC Supply Voltage 24 V Application 12 V Application	V_{CC}	+26 +14	Vdc
Operating Case Temperature Range	T_C	-20 to +100	°C
Storage Temperature Range	T_{stg}	-40 to +100	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	6.6	°C/W



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Table 3. ESD Protection Characteristics

Test Conditions	Class
Human Body Model	1 (minimum)
Machine Model	M1 (minimum)
Charge Device Model	C5 (minimum)

Table 4. Moisture Sensitivity Level

Test Methodology	Rating	Package Peak Temperature	Unit
Per JESD 22-A113, IPC/JEDEC J-STD-020	3	260	°C

Table 5. Electrical Characteristics for 24 V Application ($V_{CC} = 24$ Vdc, $T_C = +30^\circ\text{C}$, $75\ \Omega$ system unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit		
Frequency Range	BW	40	—	870	MHz		
Power Gain	G_p	50 MHz	18	—	dB		
		870 MHz	19	—			
Slope	S	—	0.6	—	dB		
Gain Flatness (40 - 870 MHz, Peak to Valley)	G_F	—	0.5	—	dB		
Input Return Loss ($Z_o = 75$ Ohms)	IRL	f = 40 - 160 MHz	21	—	dB		
		f = 161 - 450 MHz	19	—			
		f = 451 - 870 MHz	22	—			
Output Return Loss ($Z_o = 75$ Ohms)	ORL	f = 40 - 400 MHz	22	—	dB		
		f = 401 - 870 MHz	17	—			
Composite Second Order		($V_{out} = +44$ dBmV/ch., Worst Case) 132-Channel FLAT	CSO ₁₃₂	—	-65	-58	dBc
		($V_{out} = +46$ dBmV/ch., Worst Case) 112-Channel FLAT	CSO ₁₁₂	—	-65	-59	
		($V_{out} = +48$ dBmV/ch., Worst Case) 79-Channel FLAT	CSO ₇₉	—	-71	-62	
Cross Modulation Distortion @ Ch 2		($V_{out} = +44$ dBmV/ch., FM = 55 MHz) 132-Channel FLAT	XMD ₁₃₂	—	-64	-52	dBc
		($V_{out} = +46$ dBmV/ch., FM = 55 MHz) 112-Channel FLAT	XMD ₁₁₂	—	-63	-52	
		($V_{out} = +48$ dBmV/ch., FM = 55 MHz) 79-Channel FLAT	XMD ₇₉	—	-62	-52	
Composite Triple Beat		($V_{out} = +44$ dBmV/ch., Worst Case) 132-Channel FLAT	CTB ₁₃₂	—	-63	-56	dBc
		($V_{out} = +46$ dBmV/ch., Worst Case) 112-Channel FLAT	CTB ₁₁₂	—	-64	-56	
		($V_{out} = +48$ dBmV/ch., Worst Case) 79-Channel FLAT	CTB ₇₉	—	-65	-58	
Noise Figure	NF	50 MHz	—	4	5.0	dB	
		870 MHz	—	4	5.0		
DC Current ($V_{DC} = 24$ V, $T_C = -20^\circ$ to $+100^\circ\text{C}$)	I_{DC}	230	250	265	mA		

(continued)

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Table 4. Electrical Characteristics for 12 V Application ($V_{CC} = 12 \text{ Vdc}$, $T_C = +30^\circ\text{C}$, 75Ω system unless otherwise noted)
(continued)

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency Range	BW	40	—	870	MHz
Power Gain	G_p	—	18	—	dB
50 MHz 870 MHz		—	19	—	
Slope	S	—	0.6	—	dB
Gain Flatness (40 - 870 MHz, Peak to Valley)	G_F	—	0.5	—	dB
Input Return Loss ($Z_o = 75 \text{ Ohms}$)	IRL	—	21	—	dB
f = 40-160 MHz		—	19	—	
f = 161-450 MHz		—	19	—	
f = 451-870 MHz		—	19	—	
Output Return Loss ($Z_o = 75 \text{ Ohms}$)	ORL	—	19	—	dB
f = 40-400 MHz		—	17	—	
f = 401-750 MHz		—	15	—	
f = 751-870 MHz		—	15	—	
Composite Second Order ($V_{out} = +42 \text{ dBmV/ch.}$, Worst Case)	CSO_{112} CSO_{79}	—	-65	—	dBc
($V_{out} = +42 \text{ dBmV/ch.}$, Worst Case)		112-Channel FLAT 79-Channel FLAT	—	-71	
Cross Modulation Distortion @ Ch 2 ($V_{out} = +42 \text{ dBmV/ch.}$, FM = 55 MHz)	XMD_{112} XMD_{79}	—	-63	—	dBc
($V_{out} = +42 \text{ dBmV/ch.}$, FM = 55 MHz)		112-Channel FLAT 79-Channel FLAT	—	-62	
Composite Triple Beat ($V_{out} = +42 \text{ dBmV/ch.}$, Worst Case)	CTB_{112} CTB_{79}	—	-64	—	dBc
($V_{out} = +42 \text{ dBmV/ch.}$, Worst Case)		112-Channel FLAT 79-Channel FLAT	—	-65	
Noise Figure	NF	—	4	5.0	dB
50 MHz 870 MHz		—	4	5.0	
DC Current ($V_{DC} = 12 \text{ V}$, $T_C = -20^\circ$ to $+100^\circ\text{C}$)	I_{DC}	190	210	225	mA

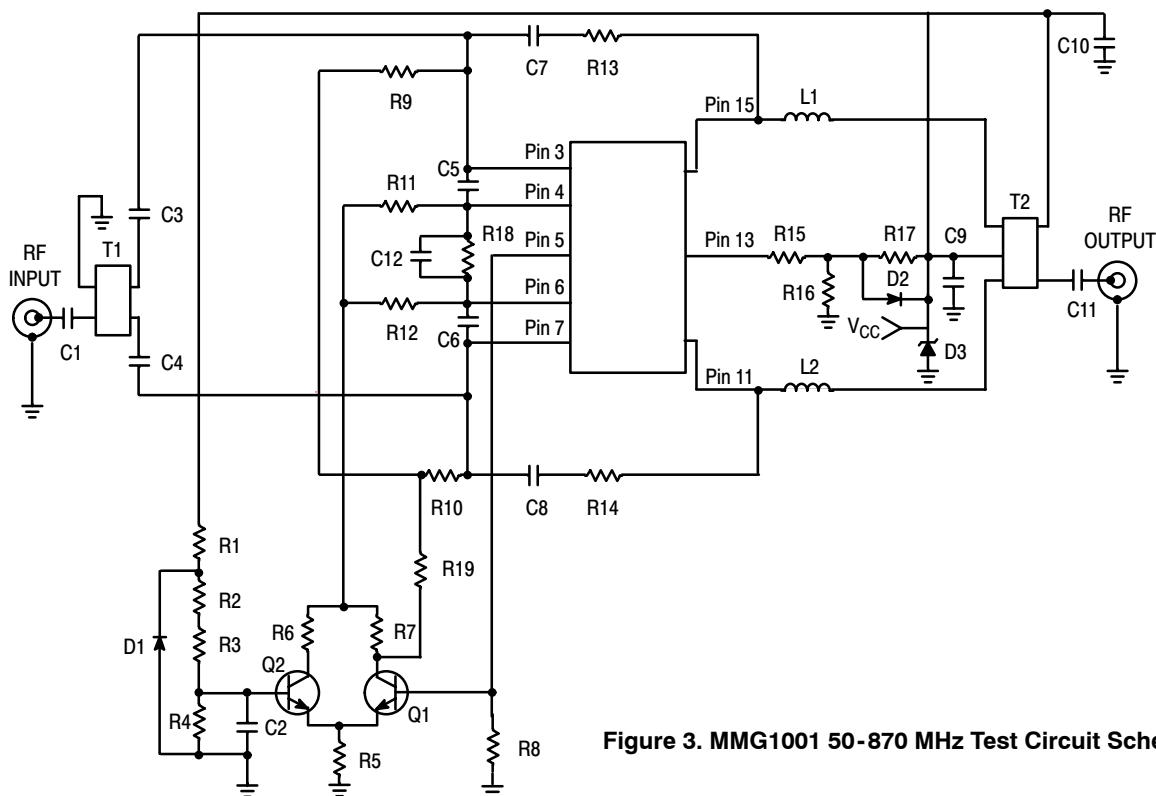
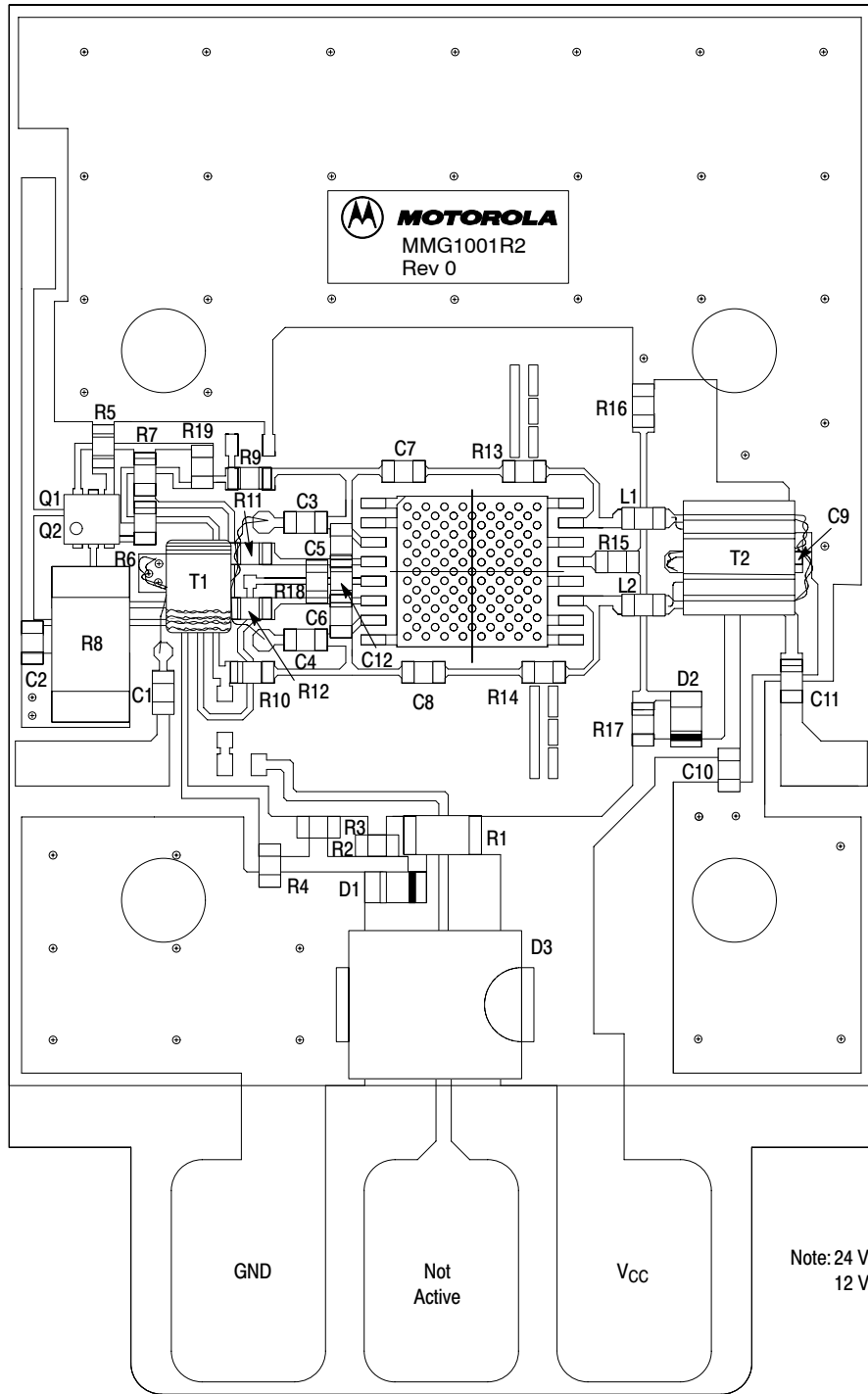


Figure 3. MMG1001 50-870 MHz Test Circuit Schematic

Table 6. MMG1001 50-870 MHz Test Circuit Component Designations and Values

Designation	Description (24 V Application)	Description (12 V Application)
C1, C7, C8, C11	220 pF Chip Capacitors (0603)	220 pF Chip Capacitors (0603)
C2, C3, C4, C9, C10	0.01 μ F Chip Capacitors (0603)	0.01 μ F Chip Capacitors (0603)
C5, C6	1.8 pF Chip Capacitors (0603)	1.8 pF Chip Capacitors (0603)
C12	5.6 pF Chip Capacitor (0603)	5.6 pF Chip Capacitor (0603)
D1	5.1 V Zener Diode, On/MM3Z5V1T1	5.1 V Zener Diode, On/MM3Z5V1T1
D2	27 V Zener Diode, On/MM3Z27VT1	27 V Zener Diode, On/MM3Z27VT1
D3	Transient Voltage Suppressor, On/1.5k27A/1.5SMC27AT3	Transient Voltage Suppressor, On/1.5k27A/1.5SMC27AT3
L1, L2	22 nH Chip Inductors (0603)	22 nH Chip Inductors (0603)
Q1, Q2	Dual Transistors Package, On/MBT3904DW1T1	Dual Transistors Package, On/MBT3904DW1T1
R1	2.2 k Ω , 1/4 W Chip Resistor (1206)	820 Ω , 1/4 W Chip Resistor (1206)
R2	560 Ω Chip Resistor (0603)	560 Ω Chip Resistor (0603)
R3	82 Ω Chip Resistor (0603)	40 Ω Chip Resistor (0603)
R4	820 Ω Chip Resistors (0603)	150 Ω Chip Resistors (0603)
R5	820 Ω Chip Resistors (0603)	100 Ω Chip Resistors (0603)
R6	120 Ω Chip Resistor (0603)	120 Ω Chip Resistor (0603)
R7	1.5 k Ω Chip Resistor (0603)	1.5 k Ω Chip Resistor (0603)
R8	12 Ω , 1 W Chip Resistor (2512)	4.8 Ω , 1 W Chip Resistor (2512)
R9, R10, R15	470 Ω Chip Resistors (0603)	470 Ω Chip Resistors (0603)
R11, R12	18 Ω Chip Resistors (0603)	18 Ω Chip Resistors (0603)
R13, R14	910 Ω Chip Resistors (0603)	910 Ω Chip Resistors (0603)
R16	2 k Ω Chip Resistor (0603)	2.7 k Ω Chip Resistor (0603)
R17	6.2 k Ω Chip Resistor (0603)	6.2 k Ω Chip Resistor (0603)
R18	15 Ω Chip Resistor (0603)	15 Ω Chip Resistor (0603)
R19	0 Ω Chip Resistor (0603)	0 Ω Chip Resistor (0603)
T1	Input Transformer, Mot/77PC016E068	Input Transformer, 77PC016E068
T2	Output Transformer, Mot/77PC016E061	Output Transformer, 77PC016E061
PCB	FR4, 62 mil, $\epsilon_r = 4.81$	FR4, 62 mil, $\epsilon_r = 4.81$



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Figure 4. MMG1001 50-870 MHz Test Circuit Component Layout

TYPICAL CHARACTERISTICS FOR 24 V APPLICATION

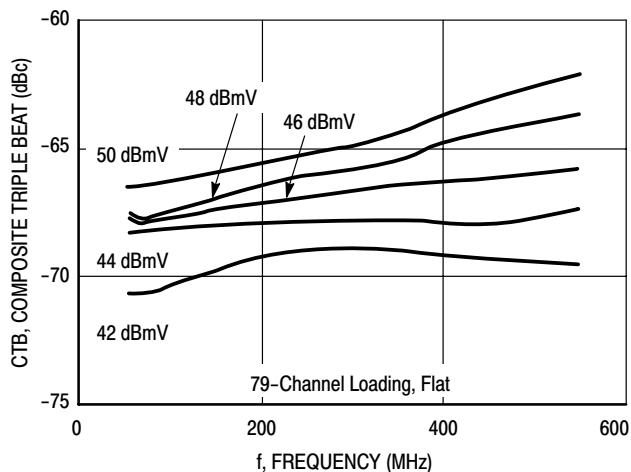


Figure 5. Composite Triple Beat versus Frequency

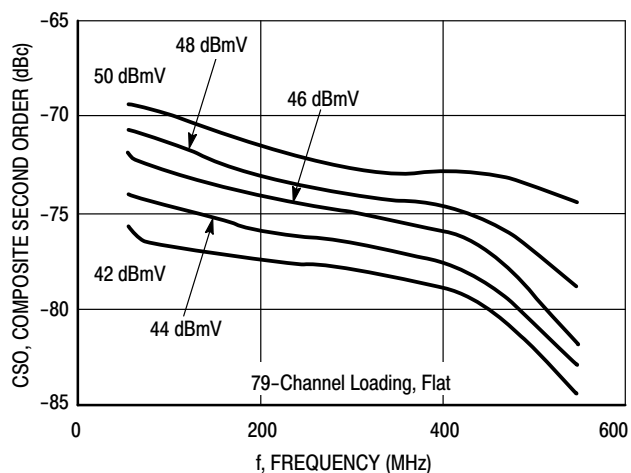


Figure 6. Composite Second Order versus Frequency

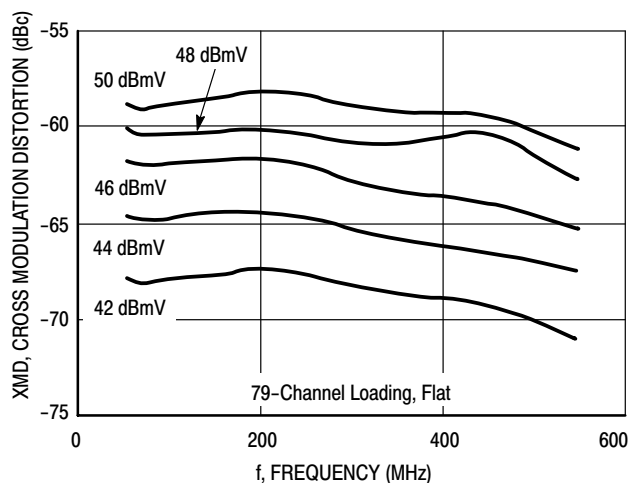
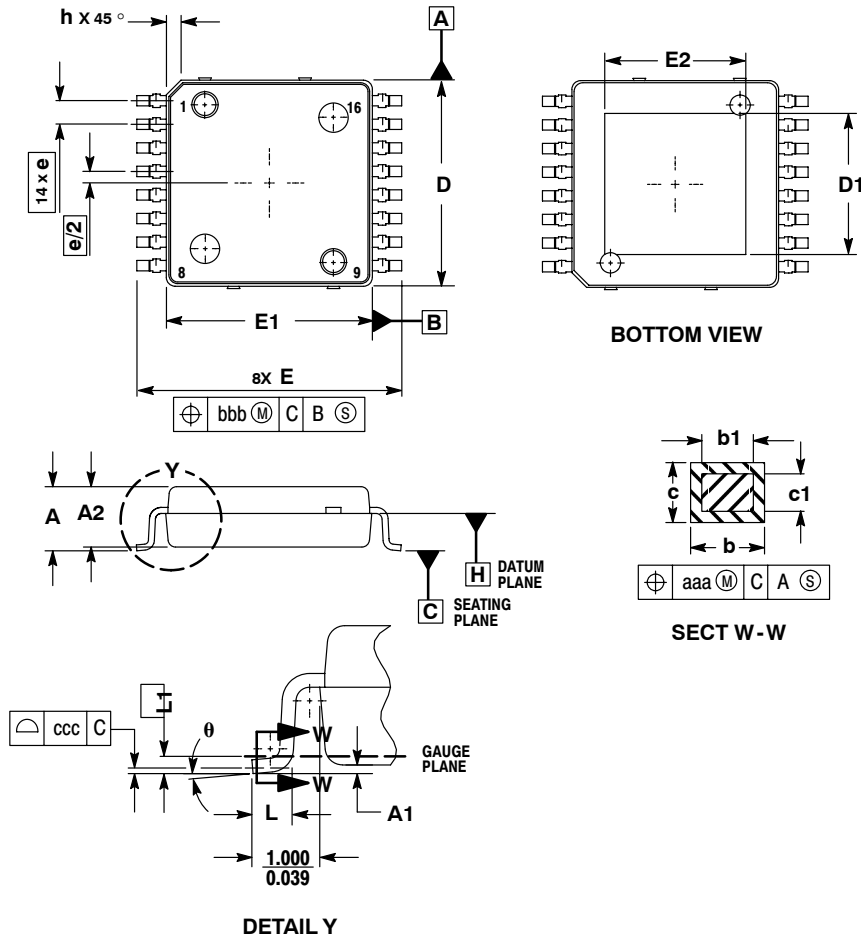


Figure 7. Cross Modulation Distortion versus Frequency

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PACKAGE DIMENSIONS



NOTES:

1. CONTROLLING DIMENSION: MILLIMETER.
2. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DATUM PLANE -H- IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.250 PER SIDE. DIMENSIONS D AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION IS 0.127 TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-.

DIM	MILLIMETERS	
	MIN	MAX
A	2.000	2.300
A1	0.025	0.100
A2	1.950	2.100
D	6.950	7.100
D1	4.372	5.180
E	8.850	9.150
E1	6.950	7.100
E2	4.372	5.180
L	0.466	0.720
L1	0.250 BSC	
b	0.300	0.432
b1	0.300	0.375
c	0.180	0.279
c1	0.180	0.230
e	0.800 BSC	
h	---	0.600
θ	0°	7°
aaa	0.200	
bbb	0.200	
ccc	0.100	

**CASE 978-03
ISSUE C
PFP-16**

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