Freescale Semiconductor
Data Sheet: Technical Data
An Energy Efficient Solution by Freescale

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✓RoHS

3-Axis Orientation/Motion Detection Sensor

The MMA7660FC is a ±1.5 g 3-Axis Accelerometer with Digital Output (I^2C). It is a very low power, low profile capacitive MEMS sensor featuring a low pass filter, compensation for 0g offset and gain errors, and conversion to 6-bit digital values at a user configurable samples per second. The device can be used for sensor data changes, product orientation, and gesture detection through an interrupt pin (INT). The device is housed in a small 3mm x 3mm x 0.9mm DFN package.

Features

- Digital Output (I^2C)
- 3mm x 3mm x 0.9mm DFN Package
- Low Power Current Consumption: Off Mode: 0.4 µA, Standby Mode: 2 µA, Active Mode: 47 µA at 1 ODR
- Configurable Samples per Second from 1 to 120 samples a second.
- Low Voltage Operation:
  – Analog Voltage: 2.4 V - 3.6 V
  – Digital Voltage: 1.71 V - 3.6 V
- Auto-Wake/Sleep Feature for Low Power Consumption
- Tilt Orientation Detection for Portrait/Landscape Capability
- Gesture Detection Including Shake Detection and Tap Detection
- Robust Design, High Shocks Survivability (10,000 g)
- RoHS Compliant
- Halogen Free
- Environmentally Preferred Product
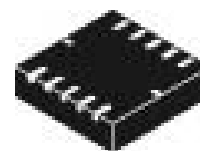- Low Cost

Typical Applications

- Mobile Phone/ PMP/PDA: Orientation Detection (Portrait/Landscape), Image Stability, Text Scroll, Motion Dialing, Tap to Mute
- Laptop PC: Anti-Theft
- Gaming: Motion Detection, Auto-Wake/Sleep For Low Power Consumption
- Digital Still Camera: Image Stability

MMA7660FC

MMA7660FC: XYZ-AXIS ACCELEROMETER
±1.5 g

Bottom View

10 LEAD
DFN
CASE 2002-03

Top View

RESERVED — 1	10 — RESERVED
N/C — 2	9 — DVDD
AVDD — 3	8 — DVSS
AVSS — 4	7 — SDA
INT — 5	6 — SCL

Figure 1. Pin Connections

ORDERING INFORMATION			
Part Number	**Temperature Range**	**Package**	**Shipping**
MMA7660FCT	−40 to +85℃	DFN-10	Tray
MMA7660FCR1	−40 to +85℃	DFN-10	7" Tape & Reel

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Definitions

Auto-Wake: Sleep Mode (uses AMSR sample rate in SR [0x08] register)
Auto-Sleep: Run Mode (uses AWSR sample rate in SR [0x08] register)
PMP: Portable Media Player
PDA: Personal Digital Assistant
DFN: Dual Flat No Lead
ESD: Electro Static Discharge
ODR: Output Data Rate
MEMS: Microelectromechanical Systems

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Top View
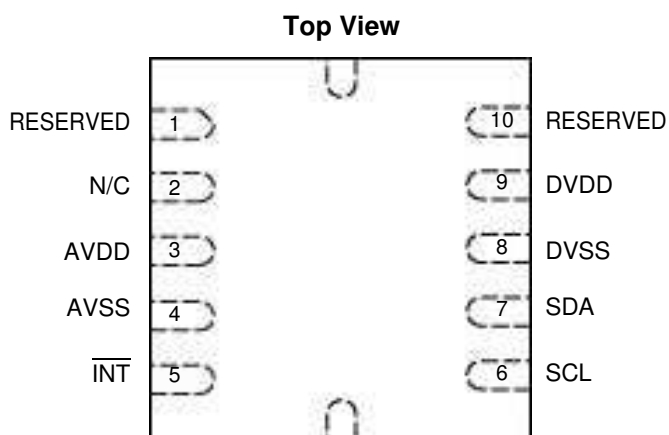
Figure 1. Pinout

Table 1. Pin Description

Pin #	Pin Name	Description	Pin Status
1	RESERVED	Connect to AVSS	Input
2	N/C	No Internal Connection, leave unconnected or connect to Ground	Input
3	AVDD	Device Power	Input
4	AVSS	Device Ground	Input
5	$\overline{INT}$	Interrupt/Data Ready	Output
6	SCL	I^{2}C Serial Clock	Input
7	SDA	I^{2}C Serial Data	Open Drain
8	DVSS	Digital I/O Ground	Input
9	DVDD	Digital I/O Power	Input
10	RESERVED	Connect to AVSS	Input
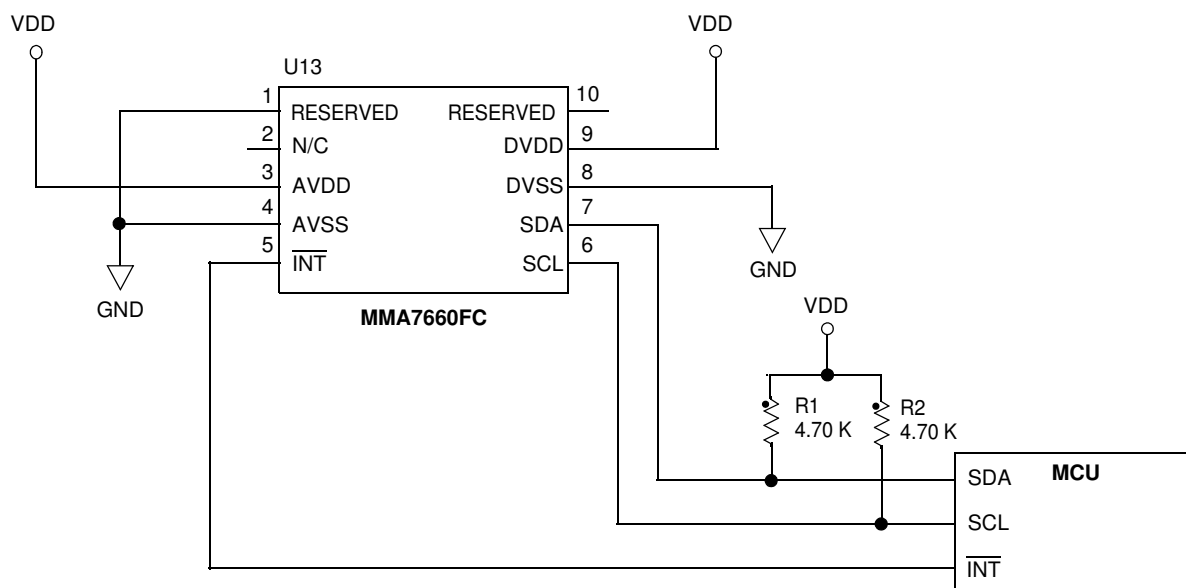
NOTE: A 0.1 μF ceramic capacitor can be placed connecting pin 3 (AVDD) to pin 4 (AVSS). In addition, another 0.1 μF ceramic capacitor can be place connecting pin 9 (DVDD) to pin 8 (DVSS). The capacitors should be placed close to the pins of the MMA7660FC and is recommended for testing and to adequately decouple the accelerometer from noise on the power supply.

Figure 2. I^{2}C Connection to MCU
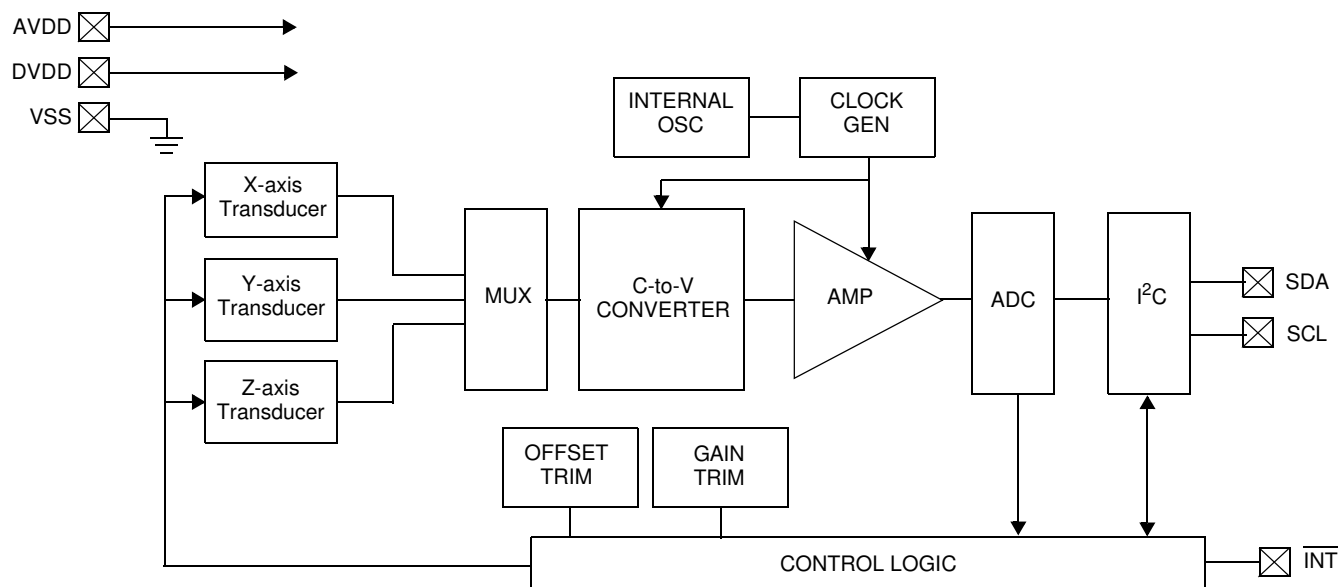
Figure 3. Simplified Accelerometer Functional Block Diagram

Table 2. Maximum Ratings

(Maximum ratings are the limits to which the device can be exposed without causing permanent damage.)

Rating	Symbol	Value	Unit
Maximum Acceleration (all axes, 100 µs)	g_{max}	10,000	g
Analog Supply Voltage	AV_{DD}	-0.3 to +3.6	V
Digital I/O pins Supply Voltage	DV_{DD_IO}	-0.3 to +3.6	V
Drop Test	D_{drop}	1.8	m
Storage Temperature Range	T_{stg}	-40 to +125	℃

ELECTRO STATIC DISCHARGE (ESD)

WARNING: This device is sensitive to electrostatic discharge.

   Although the Freescale accelerometer contains internal 2000 V ESD protection circuitry, extra precaution must be taken by the user to protect the chip from ESD. A charge of over 2000 V can accumulate on the human body or associated test equipment. A charge of this magnitude can alter the performance or cause failure of the chip. When handling the accelerometer, proper ESD precautions should be followed to avoid exposing the device to discharges which may be detrimental to its performance.

Table 3. ESD And Latch-up Protection Characteristics

Rating	Symbol	Value	Unit
Human Body Model	HBM	±2000	V
Machine Model	MM	±200	V
Charge Device Model	CDM	±500	V
Latch-up current at $T_A = 85℃$		±100	mA

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Table 4. Operating Characteristics

Unless otherwise noted: $-40\,°C \le T_A \le 85\,°C$, $2.4\ V \le AV_{DD} \le 3.6\ V$, $1.71\ V < DV_{DD} < 3.6\ V$, Acceleration = 0g

Typical values are at AV_{DD} = 2.8 V, DV_{DD} = 2.8 V, T_A = +25°C

Characteristics	Symbol	Min	Typ	Max	Unit
Analog Supply Voltage					
Standby/Operation Mode	AV_{DD}	2.4	2.8	3.6	V
Enable Bus Modeon Mode	AV_{DD}		0		V
Digital I/O Pins Supply Voltage					
Standby/Operation Mode	DV_{DD_IO}	1.71	2.8	AV_{DD}	V
Enable Bus Modeon Mode	DV_{DD_IO}	1.71	1.8	3.6	V
Supply Current Drain					
Off Mode	I_{DD}		0.4		µA
Power Down Mode	I_{DD}		2		µA
Standby Mode[1]	I_{DD}	0	2	10	µA
Active Mode, ODR = 1	I_{DD}		47		µA
Active Mode, ODR = 2	I_{DD}		49		µA
Active Mode, ODR = 4	I_{DD}		54		µA
Active Mode, ODR = 8	I_{DD}		66		µA
Active Mode, ODR = 16	I_{DD}		89		µA
Active Mode, ODR = 32	I_{DD}		133		µA
Active Mode, ODR = 64	I_{DD}		221		µA
Active Mode[1], ODR = 120	I_{DD}		294		µA
Acceleration Range			±1.5		g
Operating Temperature Range	T_A	-40	25	85	°C
0g Output Signal (T_A = 25°C, AV_{DD} = 2.8 V)					
0g Offset ±1.5g range[1]	V_{OFF}	-3	0	3	counts
0g Offset Temperature Variation					
X			-1.3		mg/°C
Y			+1.5		mg/°C
Z			-1.0		mg/°C
Sensitivity[1] (T_A = 25°C, AV_{DD} = 2.8 V)					
±1.5g range 6-bit			21.33		count/g
Acceleration Sensitivity at T_{AMB}		19.62	21.33	23.04	count/g
Acceleration Sensitivity Temperature Variation			±0.01		%/°C
Input High Voltage	V_{IH}	0.7 x D_{VDD}			
Input Low Voltage	V_{IL}			0.35 x D_{VDD}	
Output Low Voltage (IOL = 6 mA + SDA, INT)	V_{OL}			0.5	V
Input Leakage Current	I_{IH}, I_{IL}		0.025		µA
Internal Clock Frequency[1] (T_A = 25°C, AV_{DD} = 2.8 V)	t_{CLK}	135	150	165	kHz
I²C Interface Speed				400	kHz
Control Timing					
Turn on time from AV_{DD} = 0 V to AV_{DD} = 2.5 V[2]				1.3	ms
Turn off time from Active to Standby Mode				1	ms
Turn on time Standby to Active Mode				12 ms + 1/ODR	ms
Timing Clock Source Accuracy (T_A = 25°C, DV_{DD} = 1.8 V)		-10		10	%
Timing Clock Source Temperature Variation		-15		15	%
Cross Axis Sensitivity[3]			±1		%
Noise[4]			±1		count

Notes

1. These parameters are tested in production at final test.
2. Assuming VDD power on slope is < 1 ms.
3. A measure of the devices ability to reject an acceleration applied 90° from the true axis of sensitivity.
4. Noise is defined as quantiles given to a sample size. These are the occurrences of noise: 94% = ±1 count, 5% = ±2 counts, and 1% = ±3 counts.

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PRINCIPLE OF OPERATION

The Freescale Accelerometer consists of a MEMS capacitive sensing g-cell and a signal conditioning ASIC contained in a single package. The sensing element is sealed hermetically at the wafer level using a bulk micro machined cap wafer. The g-cell is a mechanical structure formed from semiconductor materials (polysilicon) using masking and etching processes.

The sensor can be modeled as a movable beam that moves between two mechanically fixed beams (Figure 4). Two gaps are formed; one being between the movable beam and the first stationary beam and the second between the movable beam and the second stationary beam.

The ASIC uses switched capacitor techniques to measure the g-cell capacitors and extract the acceleration data from the difference between the two capacitors. The ASIC also signal conditions and filters (switched capacitor) the signal, providing a digital output that is proportional to acceleration.
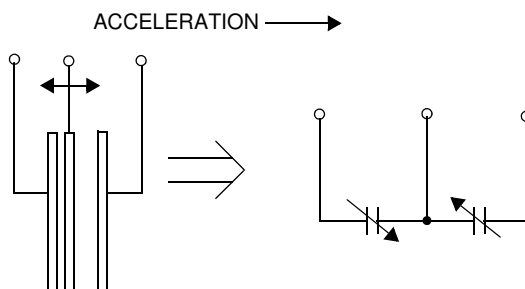
ACCELERATION ⟶

Figure 4. Simplified Transducer Physical Model

MODES OF OPERATION

The sensor has three power modes: Off Mode, Standby Mode, and Active Mode to offer the customer different power consumption options. The sensor is only capable of running in one of these modes at a time.

The Off Mode offers the lowest power consumption, approximately 0.4 µA and can only be reached by powering down the analog supply. See Figure 5. In this mode, there is no analog supply and all I²C activity is ignored.

The Standby Mode is ideal for battery operated products. When Standby Mode is active the device outputs are turned off providing a significant reduction in operating current. When the device is in Standby Mode the current will be reduced to approximately 3 µA. Standby Mode is entered as soon as both analog and digital power supplies are up. In this mode, the device can read and write to the registers with I²C, but no new measurements can be taken. The mode of the device is controlled through the MODE (0x07) control register by accessing the mode bit in the Mode register.

During the Active Mode, continuous measurement on all three axes is enabled. In addition, the user can choose to enable: Shake Detection, Tap Detection, Orientation Detection, and/or Auto-Wake/Sleep Feature and in this mode the digital analysis for any of these functions is done. The user can configure the samples per second to any of the following: 1 sample/second, 2 samples/second, 4 samples/second, 8 samples/second, 16 samples/second, 32 samples/second, 64 samples/second, and 120 samples/second, for the Auto-Sleep state. If the user is configuring the Auto-Wake feature, the selectable ranges are: 1 sample/second, 8 samples/second, 16 samples/seconds and 32 samples/second. Depending on the samples per second selected the power consumption will vary.

Table 5. Modes Of Operation

| Measurement and Power Mode	I²C Bus	DVDD	AVDD	Function
Power Down Mode	DVDD is down, so I²C bus *cannot* be used for other devices (MMA7660FC clamps I²C bus to DVVD pin)	Off	Off	MMA7660FC is powered down in both supplies. I²C activity is unavailable on bus.
		Off	On	MMA7660FC is powered down in digital supply but not analog supply. I²C activity is unavailable on bus. AVDD power cycling requires 50 msec.
Off Mode	MMA7660FC will not respond, but I²C bus can be used for other devices (MMA7660FC does not load I²C bus)	On	Off	MMA7660FC is powered down in analog supply but not digital supply. I²C activity is ignored.
Standby Mode	MMA7660FC will respond to I²C bus	On	On	MMA7660FC is powered up in both supplies, so registers can be accessed normally to set MMA7660FC to Active Mode when desired. MMA7660FC's sensor measurement system is idle.
Active Mode Auto-Sleep Auto-Wake	MMA7660FC will respond to I²C bus	On	On	MMA7660FC is able to operate sensor measurement system at user programmable samples per second and run all of the digital analysis functions. Tap detection operates in Active Mode and Auto-Sleep, but not Auto-Wake.
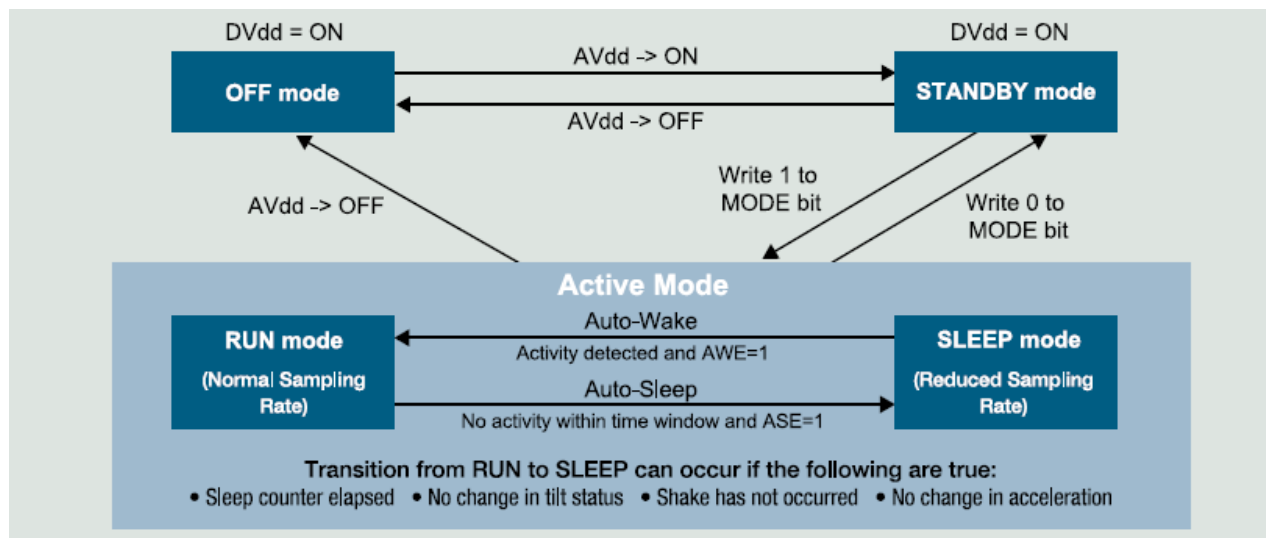
Figure 5. State Machine of Modes

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CONFIGURABLE SAMPLES PER SECONDS AND INTERRUPT SETTINGS

The device can be configured into 8 different samples per seconds including: 1 sample/second, 2 samples/second, 4 samples/second, 8 samples/second, 16 samples/second, 32 samples/second, 64 samples/second, and 120 samples/second, The user can specify the samples per second for their particular application, deciding on the trade off between power consumption and number of samples, this can be configured in the SR (0x08) register. Once the user configurable samples per second is chosen, the device will update the data for all 3 axes in the register at a resolution of 6-bits/axis.

The user can choose to enable/disable any of the following interrupts in the INTSU (0x06) register: Front/Back Interrupt, Up/Down/Left/Right Interrupt, Tap Detection Interrupt, GINT (real-time motion tracking), Shake on X-axis, Shake on Y-axis, and Shake on Z-axis. If the GINT is enabled, real-time motion tracking can be configured to trigger an interrupt after every sensor data update: 1s (1 sample/second), 500 ms (2 samples/second), 250 ms (4 samples/second), 125 ms (8 samples/second), 62.5 ms (16 samples/second), 31.25 ms (32 samples/second), 15.625 ms (64 samples/second), or 8.36 ms (120 samples/second). If any of the shake axis interrupts are enabled; excessive agitation, greater than 1.3 g, will trigger an interrupt. If either the Up/Down/Left/Right Interrupt or the Front/Back Interrupt is enabled, any change in orientation will generate an interrupt. When the Auto-Wake feature is enabled, and the Auto-Sleep counter elapses an interrupt will occur. When the device is in Auto-Sleep state, if a shake interrupt, tap interrupt, Delta G, or orientation detection interrupt occur, the device will go out of sleep state and into wake state.

POWER SAVING FEATURES

The MMA7660FC includes a range of user configurable power saving features. The device's samples per second can be set over a wide range from 1 to 120 samples a second; the operating current is directly proportional to samples per second. The analog supply A_{VDD} can be powered down to put the MMA7660FC into Off Mode, which typically draws 0.4 µA. The Auto-Wake/Sleep feature can toggle the sampling rate from a higher user selected samples per second to a lower user selected samples per second, changing based on if motion is detected or not. The user can choose to use any of the above options to configure the part and make it have the optimal power consumption level for the desired application.

TESTING THE LOGIC CHAIN

MMA7660FC can be put into Test Mode, which disables accelerometer measurements and instead allows the user to write 6-bit values directly to the three axis data registers, thus simulating real time accelerometer measurements. The state machine will respond to these values according to the enabled features and functions, allowing them to be validated.

NOTE: MMA7660FC does *not* include an accelerometer self test function, which is typically an electrostatic force applied to each axis to cause it to deflect.

FEATURES

The Sensor employs both analog and digital filtering to ensure low noise and accurate output when using the part for Shake, Tap, or Orientation Detection. During Active Mode, the data is filtered and stored for each of the 3 axes at the specified following measurement intervals: 1s (1 sample/second), 500 ms (2 samples/second), 250 ms (4 samples/second), 125 ms (8 samples/second), 62.5 ms (16 samples/second), 31.25 ms (32 samples/second), 15.625 ms (64 samples/second), or 8.36 ms (120 samples/second) or indicated in AMSR [2:0].

The 6-bit measurement data is stored in the XOUT (0x00), YOUT (0x01), and ZOUT (0x02) registers and is used to update the Shake, Alert, Tap, PoLa[2:0] (updates Up, Down, Left, and Right position), and BaFro[1:0] (updates Back and Front position) in the TILT (0x03) register used for orientation detection. The customer can configure the part by enabling a number of user-desired interrupts in the INTSU (0x06) register. Once the interrupts are enabled a change in filtered readings will cause an interrupt to occur depending on the output.

The filters that are being used by this sensor is the analog filtering, digital noise filtering of measurements used for orientation detection and updated in the XOUT (0x00), YOUT (0x01), and ZOUT (0x02) registers. The filtering method used is to oversample each axis by taking 32 readings, and then calculate the average for the output measurement data as a finite impulse response filter.

Table 6. Feature Summary Table

Feature	Will Generate Interrupt
Orientation Change	When FBINT, PLINT = 1
Shake	When SHINTX, SHINTY, SHINTZ = 1
Tap or Tilt	When PDINT = 1
Auto-Wake/Sleep	When ASINT = 1
X, Y, Z Data Update	When GINT = 1

NOTE: Sensor Measurements are NOT taken in Standby Mode or in Test Mode.

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Orientation Detection

Orientation Detection Logic

   MMA7660FC gives the customer the capability to do orientation detection for such applications as Portrait/Landscape in Mobile Phone/PDA/ PMP. The tilt orientation of the device is in 3 dimensions and is identified in its last known static position. This enables a product to set its display orientation appropriately to either portrait/landscape mode, or to turn off the display if the product is placed upside down. The sensor provides six different positions including: Left, Right, Up, Down, Back, and Front, shown in Table 7. In Active Mode the data is processed and updates the orientation positions in the TILT (0x03) register. At each measurement interval, it computes new values for Left, Right, Up, Down, Back, and Front but it does not automatically update these bits in the TILT (0x03) register. These values are updated depending on the debounce filter settings (SR Register 0x08) configured by the customer.

   In order to give the customer the ability to configure the debounce filter, specific to there application, they can change the following bits in the SR (0x08) register, FILT [2:0]. Please see below for a more detailed explanation of how the FILT [2:0] works in conjunction with updating the TILT (0x03) register:

   •   If FILT [2:0] = 000, then the new values for Left, Right, Up, Down, Back, and Front are updated in the TILT (0x03) register (PoLa [2:0] and BaFro [1:0]) after every reading without any further analysis.
   •   If FILT [2:0] = 001 – 111, then the sensor requires the computed values for Left, Right, Up, Down, Back, and Front to be the same from 1-7 consecutive readings (depending on the value in FILT [2:0], before updating the values stored in TILT (0x03) register (PoLa [2:0] and BaFro [1:0]). The debounce counter is reset after a mismatched reading or the TILT (0x03) register is updated (if the orientation condition is met).

Table 7. Orientation Detection Logic of when Interrupt will Occur

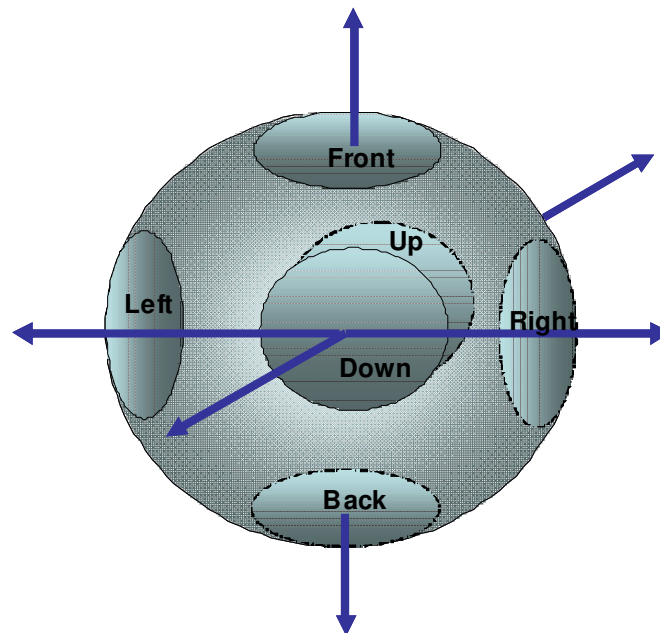| Orientation	Xg		Yg		Zg
Shake	$|X| > +1.3g$	or	$|Y| > +1.3g$	or	$|Z| > +1.3g$
Up	$|Z| < 0.8g$ and $|X| > |Y|$ and $X < 0$				
Down	$|Z| < 0.8g$ and $|X| > |Y|$ and $X > 0$				
Right			$|Z| < 0.8g$ and $|Y| > |X|$ and $Y < 0$		
Left			$|Z| < 0.8g$ and $|Y| > |X|$ and $Y > 0$		
Back					$Z < -0.25g$
Front					$Z > 0.25g$

Figure 6. Orientation Detection Logic in 3-Dimensional Space

Tap Detection

The MMA7660FC also includes a Tap Detection feature that can be used for a number of different customer applications such as button replacement. For example, a single tap can stop a song from playing and a double tap can play a song. This function detects a fast transition that exceeds a user-defined threshold (PDET (0x09) register) for a set duration (PD (0x0A) register).

Tap Detection Setup

In order to enable Tap detection in the device the user must enable the Tap Interrupt in the INTSU (0x06) register and AMSR [2:0] = 000 in the SR (0x08) register. In this mode, TILT (0x03) register, XOUT (0x00), YOUT (0x01), and ZOUT (0x02) registers will update at the 120 samples/second.

The user can configure Tap Detection to be detected on X and/or Y and/or Z axes. The customer can configure this by changing the XDA, YDA, and/or ZDA bit in the PDET (0x09) register. Detection for enabled axes is decided on an OR basis: If the PDINT bit is set in the INTSU (0x06) register, the device reports the first axis for which it detects a tap by the Tap bit in the TILT (0x03) register. When the Tap bit in the TILT (0x03) register is set, tap detection ceases, but the device will continue to process orientation detection data. Tap detection will resume when the TILT (0x03) register is read.

NOTE: Delta G is available with any AMSR setting, when XDA = YDA = ZDA = 1 (PDET = 1). When the sampling rate is less than 120 samples/second, the device can not detect tapping, but can detect small tilt angles (30 º angle change) which can not be detected by orientation detection.

Shake Detection

The shake feature can be used as a button replacement to perform functions such as scrolling through images or web pages on a Mobile Phone/PMP/PDA. The customer can enable the shake interrupt on any of the 3 axes, by enabling the SHINTX, SHINTY, and/or SHINTZ in the INTSU (0x06) register.

MMA7660FC detects shake by examining the current 6-bit measurement for each axis in XOUT, YOUT, and ZOUT. The axes that are tested for shake detection are the ones enabled by SHINTX, SHINTY, and/or SHINTZ. If a selected axis measures greater that 1.3 or less than -1.3 g, then a shake is detected for that axis and an interrupt occurs. All three axes are checked independently, but a common Shake bit in the TILT register is set when shake is detected in any one of the selected axes. Therefore when all three (SHINTX, SHINTY, and/or SHINTZ) are selected the sensor will not know what axis the shake occurred. When the TILT register is read the Shake bit is cleared during the acknowledge bit of the read access to that register and shake detection monitoring starts again.

Auto-Wake/Sleep

The MMA7660FC has the Auto-Wake/Sleep feature that can be enabled for power saving. In the Auto-Wake function, the device is put into a user specified low samples per second (1 sample/second, 8 samples/second, 16 samples/second, or 32 samples/second) in order to minimize power consumption. When the Auto-Wake is enabled and activity is detected such as a change in orientation, pulse event, Delta G acceleration or a shake event, then the device wakes up. Auto-Wake will automatically enable Auto-Sleep when the device is in wake mode and can therefore be configured to cause an interrupt on wake-up, by configuring the part to either wake-up with a change in orientation, shake, or if using the part at 120 samples/second tap detection. When the device is in Auto-Wake mode, the MODE (0x07) register, bit AWE is high. When the device has detected a change in orientation, a tap shake, or Delta G (change in acceleration), the device will enter Auto-Sleep mode. In the Auto-Sleep function, the device is put into any of the following user specified samples per seconds (1 sample/second, 2 samples/second, 4 samples/second, 8 samples/second, 16 samples/second, 32 samples/second, 64 samples/second, and 120 samples/second). In the Auto-Sleep mode, if no change in the orientation, shake or tap has occurred and the sleep counter has elapsed, the device will go into the Auto-Wake mode. When the device is in the Auto-Sleep mode, the MODE (0x07) register, bit ASE is high. The device can be programmed to continually cycle between Auto-Wake/Sleep.

NOTE: The device can either be powered on in Wake/Sleep state depending on ASE/AWE settings. If the AWE bit is set, the device is powered on in, in sleep state. If the ASW bit is set, the device is powered on in, in wake state.

Table 8. Auto-Wake/Sleep Truth Table

	Trigger Wake-up	Reset Sleep Counter	Trigger Sleep Mode
Orientation Detection Change	Yes	Yes	No
Shake	Yes	Yes	No
Delta G (set with PD (0x0A) and PDET (0x09))	Yes (XDA = YDA = ZDA = 0)	Yes	No
Pulse Detect (120 samples/second)	Yes	Yes	No
Sleep Counter Elapsed	No	No	Yes

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REGISTER DEFINITIONS

Table 9. User Register Summary

Address	Name	Definition	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$00	XOUT	6-bit output value X	-	Alert	XOUT[5]	XOUT[4]	XOUT[3]	XOUT[2]	XOUT[1]	XOUT[0]
$01	YOUT	6-bit output value Y	-	Alert	YOUT[5]	YOUT[4]	YOUT[3]	YOUT[2]	YOUT[1]	YOUT[0]
$02	ZOUT	6-bit output value Z	-	Alert	ZOUT[5]	ZOUT[4]	ZOUT[3]	ZOUT[2]	ZOUT[1]	ZOUT[0]
$03	TILT	Tilt Status	Shake	Alert	Tap	PoLa[2]	PoLa[1]	PoLa[0]	BaFro[1]	BaFro[0]
$04	SRST	Sampling Rate Status	0	0	0	0	0	0	AWSRS	AMSRS
$05	SPCNT	Sleep Count	SC[7]	SC[6]	SC[5]	SC[4]	SC[3]	SC[2]	SC[1]	SC[0]
$06	INTSU	Interrupt Setup	SHINTX	SHINTY	SHINTZ	GINT	ASINT	PDINT	PLINT	FBINT
$07	MODE	Mode	IAH	IPP	SCPS	ASE	AWE	TON	-	MODE
$08	SR	Auto-Wake/Sleep and Portrait/Landscape samples per seconds and Debounce Filter	FILT[2]	FILT[1]	FILT[0]	AWSR[1]	AWSR[0]	AMSR[2]	AMSR[1]	AMSR[0]
$09	PDET	Tap Detection	ZDA	YDA	XDA	PDTH[4]	PDTH[3]	PDTH[2]	PDTH[1]	PDTH[0]
$0A	PD	Tap Debounce Count	PD[7]	PD[6]	PD[5]	PD[4]	PD[3]	PD[2]	PD[1]	PD[0]
$0B-$1F	Factory	Reserved	-	-	-	-	-	-	-	-

NOTE: To write to the registers the MODE bit in the MODE (0x07) register must be set to 0, placing the device in Standby Mode.

$00: 6-bits output value X (Read Only when not in Test Mode)
XOUT — X Output

D7	D6	D5	D4	D3	D2	D1	D0
-	Alert	XOUT[5]	XOUT[4]	XOUT[3]	XOUT[2]	XOUT[1]	XOUT[0]
0	0	0	0	0	0	0	0

Signed byte 6-bit 2's complement data with allowable range of +31 to -32.

XOUT[5] is 0 if the g direction is positive, 1 if the g direction is negative.

If the Alert bit is set, the register was read at the same time as the device was attempting to update the contents. The register must be read again.

$01: 6-bits output value Y (Read Only when not in Test Mode)
YOUT — Y Output

D7	D6	D5	D4	D3	D2	D1	D0
-	Alert	YOUT[5]	YOUT[4]	YOUT[3]	YOUT[2]	YOUT[1]	YOUT[0]
0	0	0	0	0	0	0	0

Signed byte 6-bit 2's complement data with allowable range of +31 to -32.

YOUT[5] is 0 if the g direction is positive, 1 if the g direction is negative.

If the Alert bit is set, the register was read at the same time as the device was attempting to update the contents. The register must be read again.

$02: 6-bits output value Z (Read Only when not in Test Mode)
ZOUT — Z Output

D7	D6	D5	D4	D3	D2	D1	D0
-	Alert	ZOUT[5]	ZXOUT[4]	ZOUT[3]	ZOUT[2]	ZOUT[1]	ZOUT[0]
0	0	0	0	0	0	0	0

Signed byte 6-bit 2's complement data with allowable range of +31 to -32.

ZOUT[5] is 0 if the g direction is positive, 1 if the g direction is negative.

If the Alert bit is set, the register was read at the same time as the device was attempting to update the contents. The register must be read again.

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$03: Tilt Status (Read only)
TILT

D7	D6	D5	D4	D3	D2	D1	D0
Shake	Alert	Tap	PoLa[2]	PoLa[1]	PoLa[0]	BaFro[1]	BaFro[0]
0	0	0	0	0	0	0	0

BaFro[1:0]

00:Unknown condition of front or back
01: Front: Equipment is lying on its front
10: Back: Equipment is lying on its back

PoLa[2:0]

000: Unknown condition of up or down or left or right
001: Left: Equipment is in landscape mode to the left
010: Right: Equipment is in landscape mode to the right
101: Down: Equipment standing vertically in inverted orientation
110: Up: Equipment standing vertically in normal orientation

Tap

1: Equipment has detected a tap
0: Equipment has not detected a tap

Alert

0: Register data is valid
1: The register was read at the same time as MMA7660FC was attempting to update the contents. Re-read the register

Shake

0: Equipment is not experiencing shake in one or more of the axes enabled by SHINTX, SHINTY, and SHINTZ
1: Equipment is experiencing shake in one or more of the axes enabled by SHINTX, SHINTY, and SHINTZ

Note: When entering active mode from standby mode, if the device is flat (±1g on Z-axis) the value for BaFro will be back (-1g) or front (+1g) but PoLa will be in unknown condition. if the device is being held in an Up/Down/Right/Left position, the PoLa value will be updated with current orientation, but BaFro will be in unknown condition.

$04: Sample Rate Status Register (Read only)
SRST

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	AWSRS	AMSRS
0	0	0	0	0	0	0	0

AMSRS

0: Samples per second specified in AMSR[2:0] is not active
1: Samples per second specified in AMSR[2:0] is active

AWSRS

0: Samples per second specified in AWSR[1:0] is not active
1: Samples per second specified in AWSR[1:0] is active

$05: Sleep Count Register (Read/Write)
SPCNT

D7	D6	D5	D4	D3	D2	D1	D0
SC[7]	SC[6]	SC[5]	SC[4]	SC[3]	SC[2]	SC[1]	SC[0]
0	0	0	0	0	0	0	0

Writing to the SPCNT (0x05) register resets the internal sleep counter.

SC[7:0]

Sets the 8-bit maximum count value for the 8-bit internal sleep counter in Auto-Sleep. When the 8-bit internal sleep counter reaches the value set by SC[7:0], MMA7660FC will exit Auto-Sleep and switch to the samples per second specified in AWSR[1:0] of the SR (0x08) register.

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$06: Interrupt Setup Register
INTSU

D7	D6	D5	D4	D3	D2	D1	D0
SHINTX	SHINTY	SHINTZ	GINT	ASINT	PDINT	PLINT	FBINT
0	0	0	0	0	0	0	0

FBINT

0: Front/Back position change does not cause an interrupt
1: Front/Back position change causes an interrupt

PLINT

0: Up/Down/Right/Left position change does not cause an interrupt
1: Up/Down/Right/Left position change causes an interrupt

PDINT

0: Successful tap detection does not cause an interrupt
1: Successful tap detection causes an interrupt

ASINT

0: Exiting Auto-Sleep does not cause an interrupt
1: Exiting Auto-Sleep causes an interrupt

GINT

0: There is not an automatic interrupt after every measurement
1: There is an automatic interrupt after every measurement, when g-cell readings are updated in XOUT, YOUT, ZOUT registers, regardless of whether the readings have changed or not. This interrupt does not affect the Auto-Sleep or Auto-Wake functions.

SHINTX

0: Shake on the X-axis does not cause an interrupt or set the Shake bit in the TILT register
1: Shake detected on the X-axis causes an interrupt, and sets the Shake bit in the TILT register

SHINTY

0: Shake on the Y-axis does not cause an interrupt or set the Shake bit in the TILT register
1: Shake detected on the Y-axis causes an interrupt, and sets the Shake bit in the TILT register

SHINTZ

0: Shake on the Z-axis does not cause an interrupt or set the Shake bit in the TILT register
1: Shake detected on the Z-axis causes an interrupt, and sets the Shake bit in the TILT register.

The active interrupt condition ($\overline{IRQ}$ = 0 if IAH = 0, $\overline{IRQ}$ = 1 if IAH = 1) is released during the acknowledge bit of the slave address transmission of the first subsequent I^{2}C to MMA7660FC after the interrupt was asserted.

MMA7660FC

$07: Mode Register (Read/Write)
MODE

D7	D6	D5	D4	D3	D2	D1	D0
IAH	IPP	SCPS	ASE	AWE	TON	-	MODE
0	0	0	0	0	0	0	0

NOTE: Writing to the Mode register resets sleep timing, and clears the XOUT, YOUT, ZOUT, TILT registers.Reading to the Mode register resets sleep timing.

NOTE: The device must be placed in Standby Mode to change the value of the registers.

Table 10. Modes

Mode of Operation	D0 - MODE	D2 - TON
Standby Mode	0	0
Test Mode	0	1
Active Mode	1	0

NOTE: The device can only enter into Test Mode, when the previous mode was Standby Mode. If the device was in Active mode, set MMA766FC to Standby Mode (MODE = TON = 0), then enter Test Mode (MODE = 0, TON = 1).

MODE

0: Standby mode or Test Mode depending on state of TON
1: Active mode
Existing state of TON bit must be 0, to write MODE = 1. Test Mode must not be enabled.
MMA7660FC always enters Active Mode using the samples per second specified in AMSR[2:0] of the SR (0x08) register.
When MMA7660FC enters Active Mode with [ASE:AWE] = 11, MMA7660FC operates Auto-Sleep functionality first.

TON

0: Standby Mode or Active Mode depending on state of MODE
1: Test Mode
Existing state of MODE bit must be 0, to write TON = 1. Device must be in Standby Mode.
In Test Mode (TON = 1), the data in the XOUT, YOUT and ZOUT registers is *not* updated by measurement, but is instead updated by the user through the I²C interface for test purposes. Changes to the XOUT, YOUT and ZOUT register data is processed by MMA7660FC to change orientation status and generate interrupts just like Active Mode. Debounce filtering and shake detection are disabled in Test Mode.

AWE

0: Auto-Wake is disabled
1: Auto-Wake is enabled.
When Auto-Wake functionality is operating, the AWSRS bit is the SRST register is set and the device uses the samples per second specified in AWSR[1:0] of the SR (0x08) register. When MMA7660FC automatically exits Auto-Wake by a selected interrupt, the device will then switch to the samples per second specified in AMSR[2:0] of the SR (0x08) register. If ASE = 1, then Auto-Sleep functionality is now enabled (Table 11).

ASE

0: Auto-Sleep is disabled
1: Auto-Sleep is enabled
When Auto-Sleep functionality is operating, the AMSRS bit is the SRST register is set and the device uses the samples per second specified in AMSR[2:0] of the SR (0x08) register. When MMA7660FC automatically exits Auto-Sleep because the Sleep Counter times out, the device will then switch to the samples per second specified in AWSR[1:0] of the SR register. If AWE = 1, then Auto-Wake functionality is now enabled (Table 11).

SCPS

0: The prescaler is divide-by-1. The 8-bit internal Sleep Counter input clock is the samples per second set by AMSR[2:0], so the clock range is 120 Hz to 1 Hz depending on AMSR[2:0] setting. Sleep Counter timeout range is 256 times the prescaled clock (see Table 12).
1: Prescaler is divide-by-16. The 8-bit Sleep Counter input clock is the samples per second set by AMSR[2:0] divided by 16, so the clock range is 4 Hz to 0.0625 Hz depending on AMSR[2:0] setting. Sleep Counter timeout range is 256 times the prescaled clock (see Table 12).

IPP

0: Interrupt output $\overline{INT}$ is open-drain.
1: Interrupt output $\overline{INT}$ is push-pull

NOTE: Do NOT connect pull-up resistor from $\overline{INT}$ to higher voltage than DVDD.

IAH

0: Interrupt output $\overline{INT}$ is active low
1: Interrupt output $\overline{INT}$ is active high

The active interrupt condition ($\overline{IRQ}$ = 0 if IAH = 0, $\overline{IRQ}$ = 1 if IAH = 1) is released during the acknowledge bit of the slave address transmission of the first subsequent I²C to the device after the interrupt was asserted.

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Table 11. ASE/AWE Conditions

Condition	Auto-Wake (Sleep Mode)	Auto-Sleep (Run Mode)
AWE = 0, ASE = 0		X
AWE = 1, ASE = 0	X	
AWE = 0, ASE = 1	X	X
AWE = 1, ASE = 1	X	X

NOTE: If interrupts are enabled, interrupts will behave normally in all conditions stated in Table 11.

Table 12. Sleep Counter Timeout Ranges

AMSR	SCPS = 0		SCPS = 1	
	Minimum Range (2^0)	Maximum Range (2^8)	Minimum Range (2^0)	Maximum Range (2^8)
1 SPS	1 s	256 s	16 s	4096 s
2 SPS	0.5 s	128 s	8 s	2048 s
4 SPS	0.25 s	34 s	4 s	1024 s
8 SPS	0.125 s	32 s	2 s	512 s
16 SPS	0.625 s	16 s	1 s	256 s
32 SPS	0.03125 s	8 s	0.5 s	128 s
64 SPS	0.0156 s	4 s	0.25 s	64 s
120 SPS	0.00836 s	2.14 s	0.133 s	34.24 s

$08: Auto-Wake and Active Mode Portrait/Landscape Samples per Seconds Register (Read/Write)
SR — Sample Rate Register

D7	D6	D5	D4	D3	D2	D1	D0
FILT[2]	FILT[1]	FILT[0]	AWSR[1]	AWSR[0]	AMSR[2]	AMSR[1]	AMSR[0]
0	0	0	0	0	0	0	0

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AMSR[2:0]	NAME	DESCRIPTION
000	AMPD	Tap Detection Mode and 120 Samples/Second Active and Auto-Sleep Mode **Tap Detection Sampling Rate**: The device takes readings continually at a rate of nominally 3846 g-cell measurements a second. It then filters these high speed measurements by maintaining continuous rolling averages of the current and last g-cell measurements. The averages are updated every 260 µs to track fast moving accelerations. Tap detection: itself compares the two filtered axis responses (fast and slow) described above for each axis. The absolute (unsigned) difference between the fast and slow axis responses is compared against the tap detection delta threshold value PDTH[4:0] in the PDET (0x09) register. **For portrait/landscape detection:** The device takes and averages 32 g-cell measurements every 8.36 ms in Active Mode and Auto-Sleep. The update rate is 120 samples per second. These measurements update the XOUT (0x00), YOUT (0x01), and ZOUT (0x02) registers also.
001	AM64	64 Samples/Second Active and Auto-Sleep Mode **For portrait/landscape detection**: The device takes and averages 32 g-cell measurements every 15.625 ms in Active Mode and Auto-Sleep. The update rate is 64 samples per second. These measurements update the XOUT (0x00), YOUT (0x01), and ZOUT (0x02) registers also.
010	AM32	32 Samples/Second Active and Auto-Sleep Mode **For portrait/landscape detection:** The device takes and averages 32 g-cell measurements every 31.25 ms in Active Mode and Auto-Sleep. The update rate is 32 samples per second. These measurements update XOUT (0x00), YOUT (0x01), and ZOUT (0x02) registers also.
011	AM16	16 Samples/Second Active and Auto-Sleep Mode **For portrait/landscape detection:** The device takes and averages 32 g-cell measurements every 62.5 ms in Active Mode and Auto-Sleep. The update rate is 16 samples per second. These measurements update the XOUT (0x00), YOUT (0x01), and ZOUT (0x02) registers also.
100	AM8	8 Samples/Second Active and Auto-Sleep Mode **For portrait/landscape detection:** The device takes and averages 32 g-cell measurements every 125 ms in Active Mode and Auto-Sleep. The update rate is 8 samples per second. These measurements update the XOUT (0x00), YOUT (0x01), and ZOUT (0x02) registers also.
101	AM4	4 Samples/Second Active and Auto-Sleep Mode **For portrait/landscape detection:** The device takes and averages 32 g-cell measurements every 250 ms in Active Mode and Auto-Sleep. The update rate is 4 samples per second. These measurements update the XOUT (0x00), YOUT (0x01), and ZOUT (0x02) registers also.
110	AM2	2 Samples/Second Active and Auto-Sleep Mode **For portrait/landscape detection:** The device takes and averages 32 g-cell measurements every 500 ms in Active Mode and Auto-Sleep. The update rate is 2 samples per second. These measurements update the XOUT (0x00), YOUT (0x01), and ZOUT (0x02) registers also.
111	AM1	1 Sample/Second Active and Auto-Sleep Mode **For portrait/landscape detection:** The device takes and averages 32 g-cell measurements every 1000 ms in Active Mode and Auto-Sleep. The update rate is 1 sample per second. These measurements update the XOUT (0x00), YOUT (0x01), and ZOUT (0x02) registers also.

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AWSR[1:0]	NAME	DESCRIPTION
00	AW32	32 Samples/Second Auto-Wake Mode **For portrait/landscape detection:** The device takes and averages 32 g-cell measurements every 31.25 ms in Auto-Wake. The update rate is 32 samples per second. These measurements update the XOUT (0x00), YOUT (0x01), and ZOUT (0x02) registers also.
01	AW16	16 Samples/Second Auto-Wake Mode **For portrait/landscape detection**: The device takes and averages 32 g-cell measurements every 62.5 ms in Auto-Wake. The update rate is 16 samples per second. These measurements update the XOUT (0x00), YOUT (0x01), and ZOUT (0x02) registers also.
10	AW8	8 Samples/Second Auto-Wake Mode **For portrait/landscape detection:** The device takes and averages 32 g-cell measurements every 125 ms in Auto-Wake. The update rate is 8 samples per second. These measurements update the XOUT (0x00), YOUT (0x01), and ZOUT (0x02) registers also.
11	AW1	1 Sample/Second Auto-Wake Mode **For portrait/landscape detection**: The device takes and averages 32 g-cell measurements every 1000 ms in Auto-Wake. The update rate is 1 sample per second. These measurements update the XOUT (0x00), YOUT (0x01), and ZOUT (0x02) registers also.

FILT[2:0]	DESCRIPTION
000	Tilt debounce filtering is disabled. The device updates portrait/landscape every reading at the rate set by AMSR[2:0] or AWSR[1:0]
001	2 measurement samples at the rate set by AMSR[2:0] or AWSR[1:0] have to match before the device updates portrait/landscape data in TILT (0x03) register.
010	3 measurement samples at the rate set by AMSR[2:0] or AWSR[1:0] have to match before the device updates portrait/landscape data in TILT (0x03) register.
011	4 measurement samples at the rate set by AMSR[2:0] or AWSR[1:0] have to match before the device updates portrait/landscape data in TILT (0x03) register.
100	5 measurement samples at the rate set by AMSR[2:0] or AWSR[1:0] have to match before the device updates portrait/landscape data in TILT (0x03) register.
101	6 measurement samples at the rate set by AMSR[2:0] or AWSR[1:0] have to match before the device updates portrait/landscape data in TILT (0x03) register.
110	7 measurement samples at the rate set by AMSR[2:0] or AWSR[1:0] have to match before the device updates portrait/landscape data in TILT (0x03) register.
111	8 measurement samples at the rate set by AMSR[2:0] or AWSR[1:0] have to match before the device updates portrait/landscape data in TILT (0x03) register.

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$09: Tap/Pulse Detection Register (Read/Write)
PDET

D7	D6	D5	D4	D3	D2	D1	D0
ZDA	YDA	XDA	PDTH[4]	PDTH[3]	PDTH[2]	PDTH[1]	PDTH[0]
0	0	0	0	0	0	0	0

NOTE: If XDA = YDA = ZDA = 0, samples per second is 120 samples/second, and Auto-Wake/Sleep feature is enabled, the tap interrupt will reset the sleep counter.

PDTH[4:0]	DESCRIPTION
00000	Tap detection threshold is ±1 count
00001	
00010	Tap detection threshold is ±2 counts
00011	Tap detection threshold is ±3 counts
...	... and so on up to...
11101	Tap detection threshold is ±29 counts
11110	Tap detection threshold is ±30 counts
11111	Tap detection threshold is ±31 counts

XDA

1: X-axis is disabled for tap detection
0: X-axis is enabled for tap detection

YDA

1: Y-axis is disabled for tap detection
0: Y-axis is enabled for tap detection

ZDA

1: Z-axis is disabled for tap detection
0: Z-axis is enabled for tap detection

$0A: *PD:* Tap/Pulse Debounce Count Register (Read/Write)

D7	D6	D5	D4	D3	D2	D1	D0
PD[7]	PD[6]	PD[5]	PD[4]	PD[3]	PD[2]	PD[1]	PD[0]
0	0	0	0	0	0	0	0

PD[4:0]	DESCRIPTION
00000000	The tap detection debounce filtering requires 2 adjacent tap detection tests to be the same to trigger a tap event and set the Tap bit in the TILT (0x03) register, and optionally set an interrupt if PDINT is set in the INTSU (0x06) register. Tap detection response time is nominally 0.52 ms.
00000001	
00000010	Tap detection debounce filtering requires 3 adjacent tap detection tests to be the same to trigger a tap event and set the Tap bit in the TILT (0x03) register, and optionally set an interrupt if PDINT is set in the INTSU (0x06) register. Tap detection response time is nominally 0.78 ms.
00000011	Tap detection debounce filtering requires 4 adjacent tap detection tests to be the same to trigger a tap event and set the Tap bit in the TILT (0x03) register, and optionally set an interrupt if PDINT is set in the INTSU (0x06) register. Tap detection response time is nominally 1.04 ms.
...	... and so on up to...
11111101	Tap detection debounce filtering requires 254 adjacent tap detection tests to be the same to trigger a tap event and set the Tap bit in the TILT (0x03) register, and optionally set an interrupt if PDINT is set in the INTSU (0x06) register. Tap detection response time is nominally 66.04 ms.
11111110	Tap detection debounce filtering requires 255 adjacent tap detection tests to be the same to trigger a tap event and set the Tap bit in the TILT (0x03) register, and optionally set an interrupt if PDINT is set in the INTSU (0x06) register. Tap detection response time is nominally 66.3 ms.
11111111	Tap detection debounce filtering requires 256 adjacent tap detection tests to be the same to trigger a tap event and set the Tap bit in the TILT (0x03) register, and optionally set an interrupt if PDINT is set in the INTSU (0x06) register. Tap detection response time is nominally 66.56 ms.

MMA7660FC

SERIAL INTERFACE

Serial-Addressing

MMA7660FC operates as a slave that sends and receives data through an I^{2}C 2-wire interface. The interface uses a Serial Data Line (SDA) and a Serial Clock Line (SCL) to achieve bi-directional communication between master(s) and slave(s). A master (typically a microcontroller) initiates all data transfers to and from the device, and generates the SCL clock that synchronizes the data transfer.
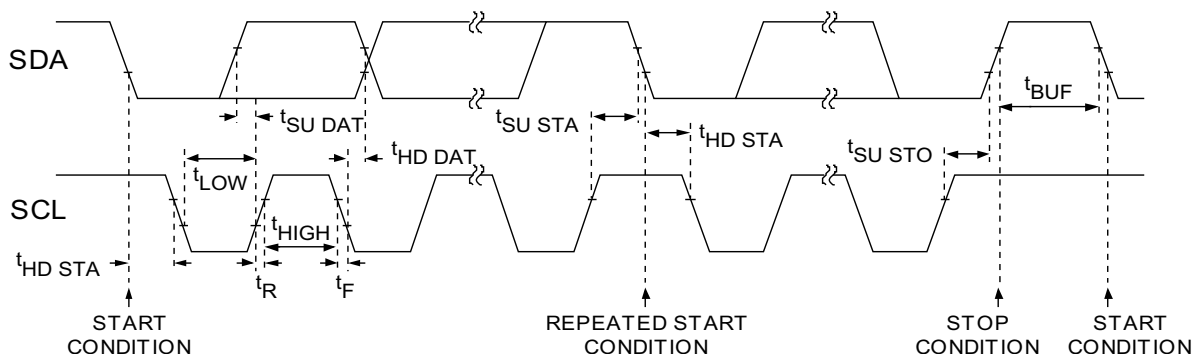
Figure 7. 2-Wire Serial Interface Timing Details

The device's SDA line operates as both an input and an open-drain output. A pull-up resistor, typically 4.7 kΩ, is required on SDA. The device's SCL line operates only as an input. A pull-up resistor, typically 4.7 kΩ, is required on SCL if there are multiple masters on the 2-wire interface, or if the master in a single-master system has an open-drain SCL output.

Each transmission consists of a START condition (Figure 7) sent by a master, followed by MMA7660FC's 7-bit slave address plus R/$\overline{W}$ bit, a register address byte, one or more data bytes, and finally a STOP condition.
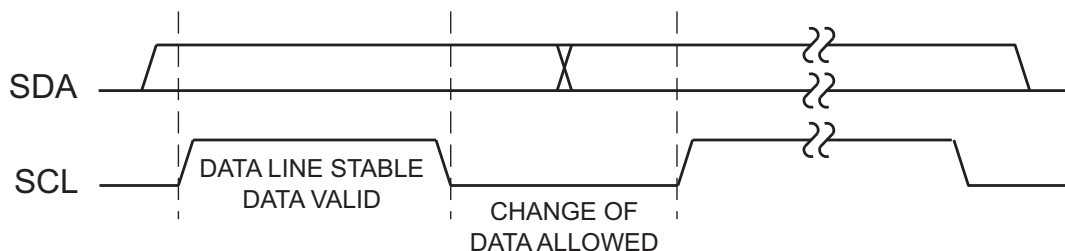
Figure 8. Start and Stop Conditions

Start and Stop Conditions

Both SCL and SDA remain high when the interface is not busy. A master signals the beginning of a transmission with a START (S) condition by transitioning SDA from high to low while SCL is high. When the master has finished communicating with the slave, it issues a STOP (P) condition by transitioning SDA from low to high while SCL is high. The bus is then free for another transmission.

Bit Transfer

One data bit is transferred during each clock tap. See Figure 9. The data on SDA must remain stable while SCL is high.
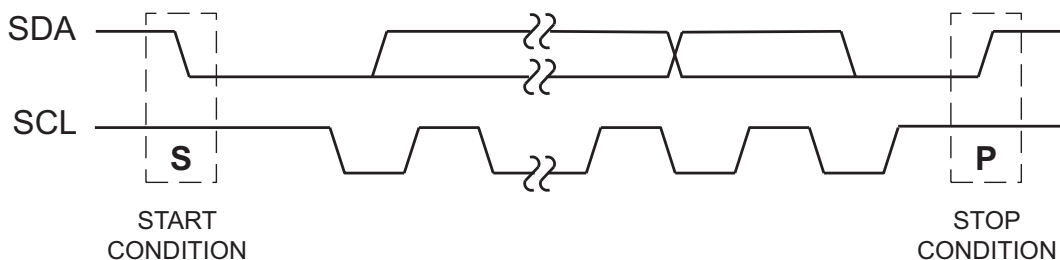
Figure 9. Bit Transfer

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Acknowledge

The acknowledge bit is a clocked 9th bit, shown in Figure 10, which the recipient uses to handshake a receipt of each byte of data. Thus each byte transferred effectively requires 9-bits. The master generates the 9th clock tap, and the recipient pulls down SDA during the acknowledge clock tap, such that the SDA line is stable low during the high period of the clock tap. When the master is transmitting to MMA7660FC, it generates the acknowledge bit because it is the recipient. When the device is transmitting to the master, the master generates the acknowledge bit because the master is the recipient.
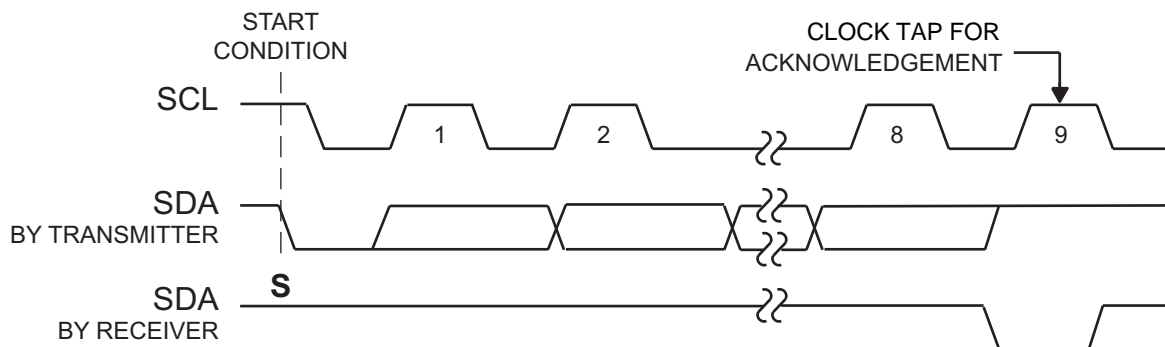
Figure 10. Acknowledge

The Slave Address

MMA7660FC has a 7-bit long slave address, shown in Figure 11. The bit following the 7-bit slave address (bit eight) is the R/$\overline{W}$ bit, which is low for a write command and high for a read command. The device has a factory set I^2C slave address which is normally 1001100 (0x4C). Contact the factory to request a different I^2C slave address, which is available in the range 0001000 to 1110111 (0x08 to 0xEF), by metal mask option.
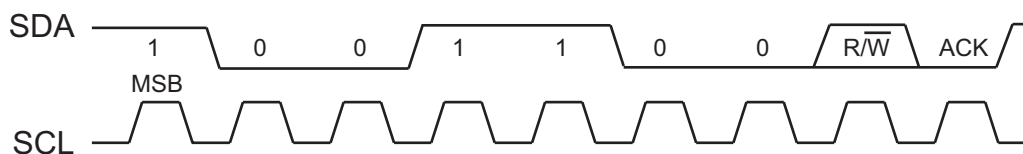

Figure 11. Slave Address

The device monitors the bus continuously, waiting for a START condition followed by its slave address. When the device recognizes its slave address, it acknowledges and is then ready for continued communication.

Message Format for Writing MMA7660FC

A write to MMA7660FC comprises the transmission of the device's keyscan slave address with the R/$\overline{W}$ bit set to 0, followed by at least one byte of information. The first byte of information is the register address of the first internal register that is to be updated. The Master Write address is 1001 1000 (0x98). If a STOP condition is detected after just the register address is received, then MMA7660FC takes no action. See Figure 12. MMA7660FC clears its internal register address pointer to register 0x00 when a STOP condition is detected, so a single byte write has no net effect because the register address given in this first and only byte is replaced by 0x00 at the STOP condition. The internal register address pointer is *not*, however, cleared on a repeated start condition. Use a single byte write followed by a repeated start to read back data from a register.

Any bytes received after the register address are data bytes. The first data byte goes into the internal register of the device selected by the register address. See Figure 12.
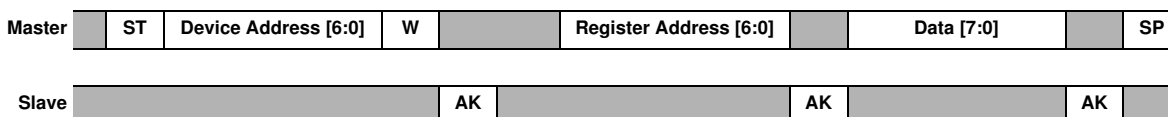
Master	ST	Device Address [6:0]	W		Register Address [6:0]		Data [7:0]		SP
Slave				AK		AK		AK	

Figure 12. Single Byte Write

MMA7660FC

If multiple data bytes are transmitted before a STOP condition is detected, these bytes are generally stored in subsequent MMA7660FC internal registers because the register address generally auto-increments.
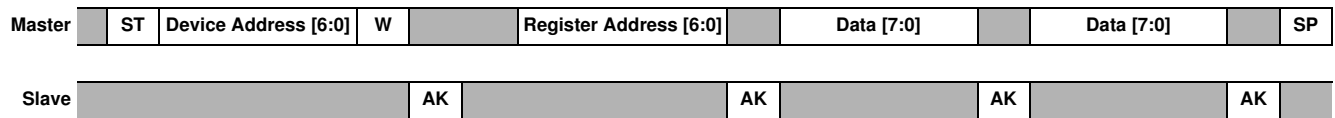
Master		ST	Device Address [6:0]	W		Register Address [6:0]		Data [7:0]		Data [7:0]		SP
Slave					AK		AK		AK		AK	

Figure 13. Multiple Bytes Write

Message Format for Reading MMA7660FC

MMA7660FC is read using it's internally stored register address as address pointer, the same way the stored register address is used as address pointer for a write. The pointer generally auto-increments after each data byte is read using the same rules as for a write. Thus, a read is initiated by first configuring the device's register address by performing a write (Figure 12) followed by a repeated start. The Master Write address is 1001 1001 (0x99). The master can now read 'n' consecutive bytes from it, with the first data byte being read from the register addressed by the initialized register address.
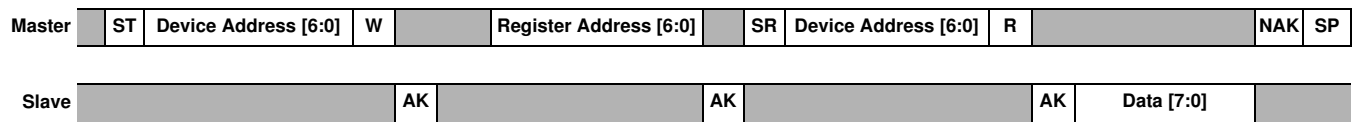
Master		ST	Device Address [6:0]	W		Register Address [6:0]		SR	Device Address [6:0]	R		NAK	SP
Slave					AK		AK			AK	Data [7:0]		

Figure 14. Single Byte Read

Master		ST	Device Address [6:0]	W		Register Address [6:0]		SR	Device Address [6:0]	R		AK
Slave					AK		AK			AK	Data [7:0]	

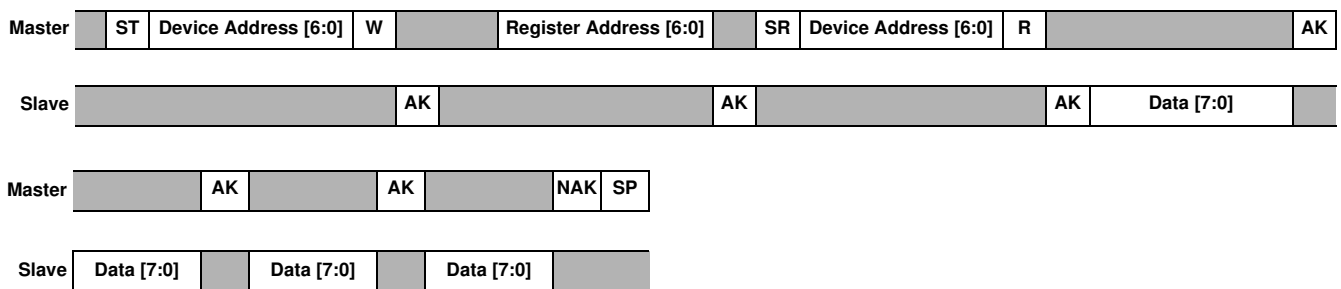| Master		AK		AK		NAK	SP
Slave	Data [7:0]		Data [7:0]		Data [7:0]		

Figure 15. Multiple Bytes Read

APPENDIX A – PACKAGE REQUIREMENTS FOR MMA7660FC

Minimum Recommended Footprint for Surface Mounted Applications

Surface mount board layout is a critical portion of the total design. The footprint for the surface mount packages must be the correct size to ensure proper solder connection interface between the board and the package. With the correct footprint, the packages will self-align when subjected to a solder reflow process. It is always recommended to design boards with a solder mask layer to avoid bridging and shorting between solder pads.

Soldering And Mounting Guidelines for the DFN Accelerometer Sensor to a PC Board

These guidelines are for soldering and mounting the Dual Flat No-Lead (DFN) package inertial sensors to printed circuit boards (PCBs). The purpose is to minimize the stress on the package after board mounting. The MMA7660 digital output accelerometer uses the DFN package platform. This section describes suggested methods of soldering these devices to the PC board for consumer applications. Pages 31, 32, and 33 show the package outline drawing for the package.

Overview of Soldering Considerations

Information provided here is based on experiments executed on DFN devices. They do not represent exact conditions present at a customer site. Hence, information herein should be used as guidance only and process and design optimizations are recommended to develop an application specific solution. It should be noted that with the proper PCB footprint and solder stencil designs the package will self-align during the solder reflow process. The following are the recommended guidelines to follow for mounting DFN sensors for consumer applications.

Halogen Content

This package is designed to be Halogen Free, exceeding most industry and customer standards. Halogen Free means that no homogeneous material within the assembly package shall contain chlorine (Cl) in excess of 700 ppm or 0.07% weight/weight or bromine (Br) in excess of 900 ppm or 0.09% weight/weight.

Note: Halogen Free is only compliant to the MMA7660FC, not to the packaging material.

PCB Mounting Recommendations

1. The PCB land should be designed with Non Solder Mask Defined (NSMD) as shown in Figure 16 and Figure 17.
2. No additional via pattern underneath package.
3. PCB land pad is 0.825 mm x 0.3 mm as shown in Figure 16 and Figure 17.
4. Do not solder down smaller side tabs on either end of the package.
5. The solder mask opening is equal to the size of the PCB land pad plus 0.15 mm.
6. The stencil aperture size is equal to the PCB land pad – minus 0.03 mm total.
7. Stencil thickness should be 75 μm.
8. Do not place any components or vias at a distance less than 2 mm from the package land area. This may cause additional package stress if it is too close to the package land area.
9. Signal traces connected to pads should be as symmetric as possible. Put dummy traces on NC pads in order to have same length of exposed trace for all pads. Signal traces with 0.15 mm width and minimum 0.5 mm length for all PCB land pads near the package are recommended as shown in Figure 16 and Figure 17. Wider trace can be continued after the 0.5 mm zone.
10. Use a standard pick and place process and equipment. Do not use a hand soldering process.
11. It is recommended to use a no clean solder paste.
12. Do not use a screw down or stacking to fix the PCB into an enclosure because this could bend the PCB putting stress on the package.
13. The PCB should be rated for the multiple lead-free reflow condition with max 260°C temperature.
14. No copper traces on top layer of PCB under the package. This will cause planarity issues with board mount.

Freescale DFN sensors are compliant with Restrictions on Hazardous Substances (RoHS), having halide free molding compound (green) and lead-free terminations. These terminations are compatible with tin-lead (Sn-Pb) as well as tin-silver-copper (Sn-Ag-Cu) solder paste soldering processes. Reflow profiles applicable to those processes can be used successfully for soldering the devices.
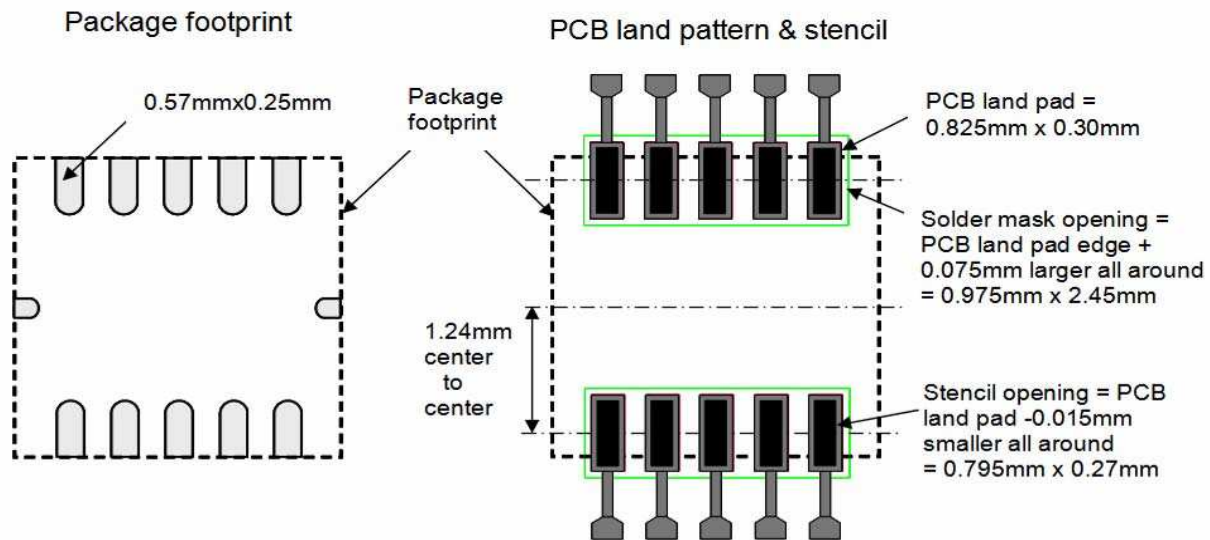
MMA7660FC

Package footprint

0.57mmx0.25mm

Package footprint

PCB land pattern & stencil

PCB land pad = 0.825mm x 0.30mm

Solder mask opening = PCB land pad edge + 0.075mm larger all around = 0.975mm x 2.45mm

1.24mm center to center

Stencil opening = PCB land pad -0.015mm smaller all around = 0.795mm x 0.27mm

Figure 16. Package Footprint, PCB Land Pattern, and Stencil Design

Wider trace

Signal trace near package: 0.15mm width and minimum 0.5mm length are recommended. Wider trace can be continued after this point.

Solder mask opening

0.5mm

0.15mm

Package footprint

0.10mm

0.5mm   0.5mm
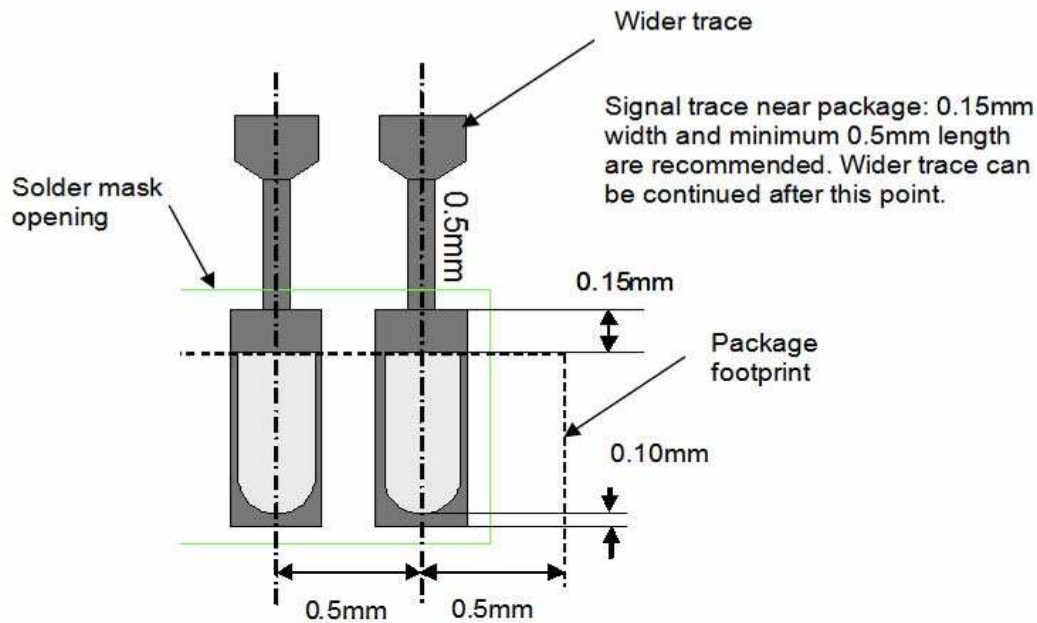
Figure 17. PCB Land Pattern Detail

Top View

Direction of Earth's Gravity

XOUT @ -1g
YOUT @ 0g
ZOUT @ 0g

XOUT @ 0g
YOUT @ +1g
ZOUT @ 0g

XOUT @ 0g
YOUT @ -1g
ZOUT @ 0g

XOUT @ +1g
YOUT @ 0g
ZOUT @ 0g

XOUT @ 0g
YOUT @ 0g
ZOUT @ +1g

Side View

XOUT @ 0g
YOUT @ 0g
ZOUT @ -1g
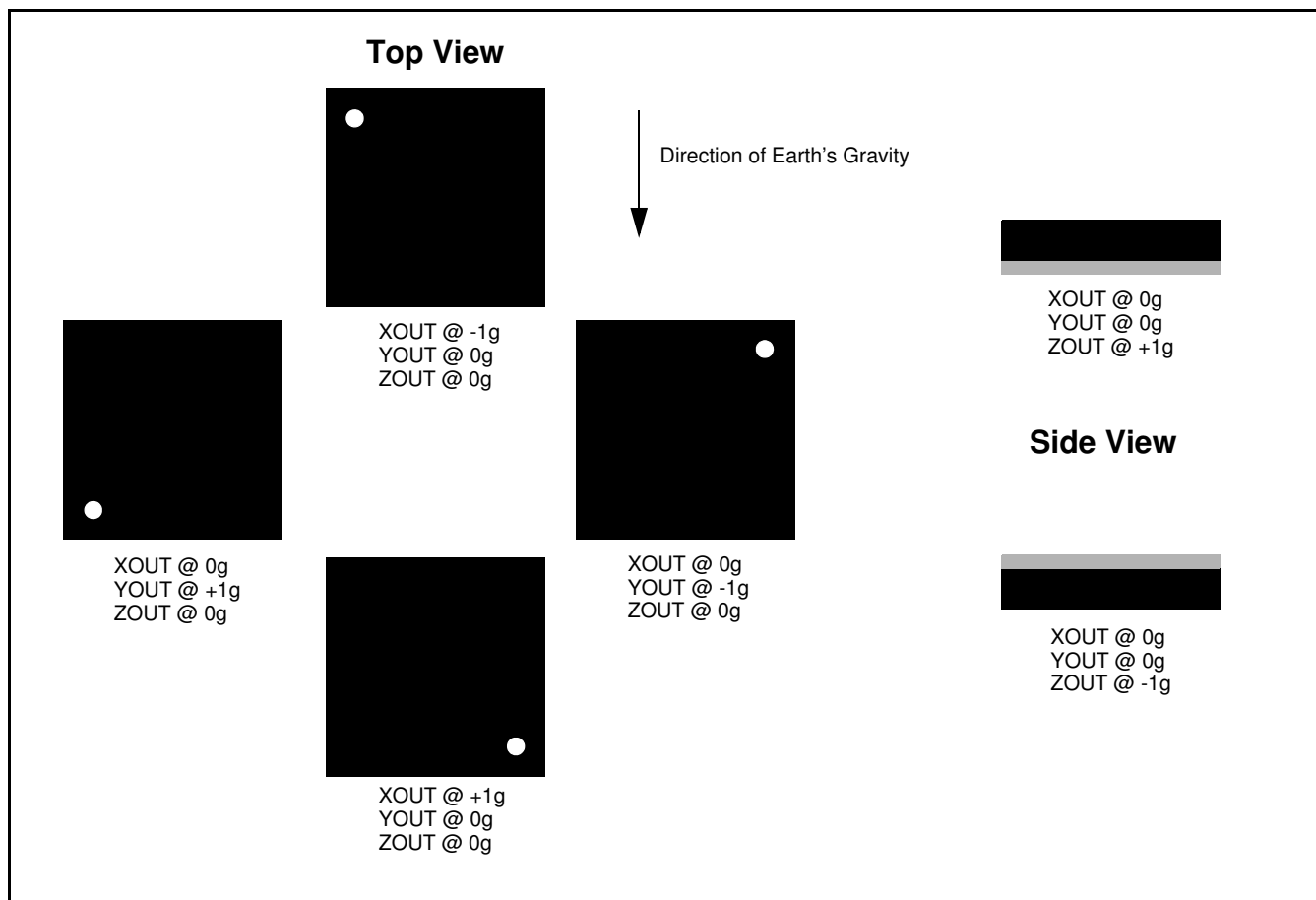
Figure 18. Product Orientation on Perpendicular Axis

+Z

-Y

-X

+X

+Y

-Z
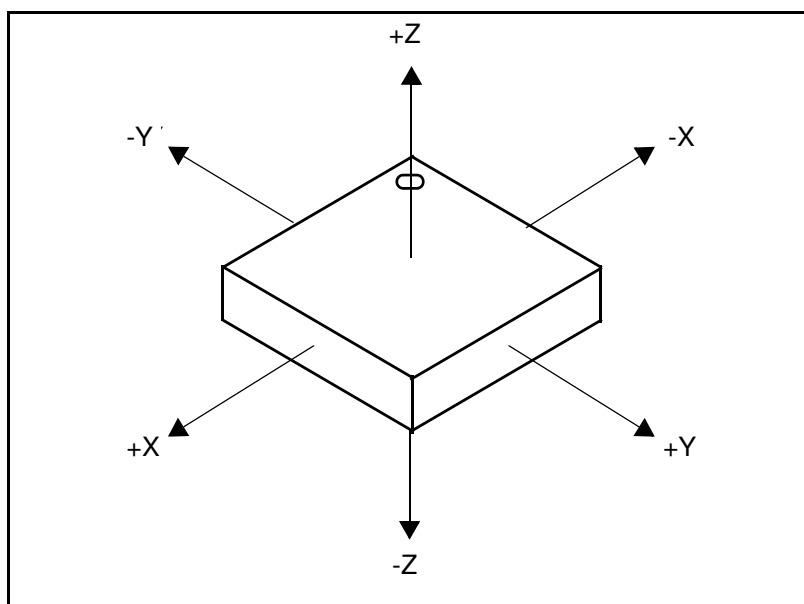
Figure 19. Product Orientations Showing Direction for Each Axis in Composite

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APPENDIX C - MMA7660FC ACQUISITION CODE TABLE

6-bit result	Binary	2's Comp	g value	Angle X or Y		Angle Z
0	0	0	0.000g	0.00°		90.00°
1	1	1	0.047g	2.69°		87.31°
2	10	2	0.094g	5.38°		84.62°
3	11	3	0.141g	8.08°		81.92°
4	100	4	0.188g	10.81°		79.19°
5	101	5	0.234g	13.55°		76.45°
6	110	6	0.281g	16.33°		73.67°
7	111	7	0.328g	19.16°		70.84°
8	1000	8	0.375g	22.02°		67.98°
9	1001	9	0.422g	24.95°		65.05°
10	1010	10	0.469g	27.95°		62.05°
11	1011	11	0.516g	31.04°		58.96°
12	1100	12	0.563g	34.23°	Z-axis must be in the range	55.77°
13	1101	13	0.609g	37.54°		52.46°
14	1110	14	0.656g	41.01°		48.99°
15	1111	15	0.703g	44.68°		45.32°
16	10000	16	0.750g	48.59°		41.41°
17	10001	17	0.797g	52.83°		37.17°
18	10010	18	0.844g	57.54°		32.46°
19	10011	19	0.891g	62.95°		27.05°
20	10100	20	0.938g	69.64°		20.36°
21	10101	21	0.984g	79.86°		10.14°
22	10110	22	1.031g			
23	10111	23	1.078g			
24	11000	24	1.125g			
25	11001	25	1.172g			
26	11010	26	1.219g			
27	11011	27	1.266g			
28	11100	28	1.313g	Shaken		
29	11101	29	1.359g	Shaken		
30	11110	30	1.406g	Shaken		
31	11111	31	1.453g	Shaken		
63	111111	-1	-0.047g	-2.69°		-87.31°
62	111110	-2	-0.094g	-5.38°		-84.62°
61	111101	-3	-0.141g	-8.08°		-81.92°
60	111100	-4	-0.188g	-10.81°		-79.19°
59	111011	-5	-0.234g	-13.55°		-76.45°
58	111010	-6	-0.281g	-16.33°		-73.67°
57	111001	-7	-0.328g	-19.16°		-70.84°
56	111000	-8	-0.375g	-22.02°		-67.98°
55	110111	-9	-0.422g	-24.95°		-65.05°
54	110110	-10	-0.469g	-27.95°		-62.05°
53	110101	-11	-0.516g	-31.04°		-58.96°
52	110100	-12	-0.563g	-34.23°		-55.77°
51	110011	-13	-0.609g	-37.54°		-52.46°
50	110010	-14	-0.656g	-41.01°		-48.99°

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49	110001	-15	-0.703g	-44.68°		-45.32°
48	110000	-16	-0.750g	-48.59°		-41.41°
47	101111	-17	-0.797g	-52.83°		-37.17°
46	101110	-18	-0.844g	-57.54°		-32.46°
45	101101	-19	-0.891g	-62.95°		-27.05°
44	101100	-20	-0.938g	-69.64°		-20.36°
43	101011	-21	-0.984g	-79.86°		-10.14°
42	101010	-22	-1.031g			
41	101001	-23	-1.078g			
40	101000	-24	-1.125g			
39	100111	-25	-1.172g			
38	100110	-26	-1.219g			
37	100101	-27	-1.266g			
36	100100	-28	-1.313g	Shaken		
35	100011	-29	-1.359g	Shaken		
34	100010	-30	-1.406g	Shaken		
33	100001	-31	-1.453g	Shaken		
32	100000	-32	-1.500g	Shaken		

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APPENDIX D - I^{2}C AC CHARACTERISTICS

This section includes information about I^{2}C AC Characteristics.

Table 1. I^{2}C AC Characteristics
(Typical Operating Circuit, V_{DD} = 1.71 V to 2.75 V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical current values are at V_{DD} = 1.8 V, T_A = +25°C.)

Parameter	Symbol	Min	Typ	Max	Units
Serial Clock Frequency[1]	f_{SCL}			400	kHz
Bus Free Time Between a STOP and a START Condition[2]	t_{BUF}	1.3			µs
Hold Time, (Repeated) START Condition[2]	$t_{HD, STA}$	0.6			µs
Repeated START Condition Setup Time[2]	$t_{SU, STA}$	0.6			µs
STOP Condition Setup Time[2]	$t_{SU, STO}$	0.6			µs
Data Hold Time[2]	$t_{HD, DAT}$			0.9	µs
Data Setup Time[2]	$t_{SU, DAT}$	100			ns
SCL Clock Low Period[2]	t_{LOW}	1.3			µs
SCL Clock High Period[2]	t_{HIGH}	0.7			µs
Rise Time of Both SDA and SCL Signals, Receiving[2]	t_R		$20+0.1C_b$	300	ns
Fall Time of Both SDA and SCL Signals, Receiving[2]	t_F		$20+0.1C_b$	300	ns
Fall Time of SDA Transmitting[2]	$t_{F.TX}$		$20+0.1C_b$	250	ns
Pulse Width of Spike Suppressed[2]	t_{SP}		25		ns
Capacitive Load for Each Bus Line[2]	C_b			400	pF

1. Parameters tested 100% at final test at room temperature; limits at -40°C and +85°C, verified by characterization, not test in production.
2. Limits verified by characterization, not tested in production.

PACKAGE DIMENSIONS

© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	**MECHANICAL OUTLINE**	PRINT VERSION NOT TO SCALE	
TITLE: DUAL FLAT NO LEAD COL PACKAGE (DFN-COL) 10 TERMINAL, 0.5 PITCH (3 X 3 X 0.9)	DOCUMENT NO: 98ASA10816D	REV: B	
	CASE NUMBER: 2002-03	14 AUG 2008	
	STANDARD: NON JEDEC		

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DETAIL N

DETAIL M
PIN 1 BACKSIDE INDEX

0.1
0.1

R0.05

DETAIL N
PIN 1 BACKSIDE INDEX

// 0.1 C

1.0
0.8

1.00
0.75

0.05 C ⚐ 4

0.05
0.00

(0.22)

(0.5)

C

SEATING PLANE

DETAIL G

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TITLE: DUAL FLAT NO LEAD COL PACKAGE (DFN−COL) 10 TERMINAL, 0.5 PITCH (3 X 3 X 0.9)	DOCUMENT NO: 98ASA10816D	REV: B	
	CASE NUMBER: 2002−03	14 AUG 2008	
	STANDARD: NON JEDEC		

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PACKAGE DIMENSIONS

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.

2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M−1994.

3. THIS IS NON JEDEC REGISTERED PACKAGE.

4. COPLANARITY APPLIES TO LEADS AND ALL OTHR BOTTOM SURFACE METALLIZATION.

5. MIN. METAL GAP SHOULD BE 0.2MM.

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TITLE: DUAL FLAT NO LEAD COL PACKAGE (DFN−COL) 10 TERMINAL, 0.5 PITCH (3 X 3 X 0.9)	DOCUMENT NO: 98ASA10816D	REV: B	
	CASE NUMBER: 2002−03	14 AUG 2008	
	STANDARD: NON JEDEC		

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Table 2. Revision History

Revision number	Revision date	Description of changes
9	03/2012	• Changed pin 10 from N/C to RESERVED on page 1, Figure 1, Figure 2 and Table 1: Pin description.

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Japan:
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064
Japan
0120 191014 or +81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:
Freescale Semiconductor China Ltd.
Exchange Building 23F
No. 118 Jianguo Road
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China
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