

# ±1.5g Dual Axis Micromachined Accelerometer

The MMA6200 series of low cost capacitive micromachined accelerometers feature signal conditioning, a 1-pole low pass filter and temperature compensation. Zero-g offset full scale span and filter cut-off are factory set and require no external devices. A full system self-test capability verifies system functionality.

## Features

- High Sensitivity
- Low Noise
- Low Power
- 2.7 V to 3.6 V Operation
- 6mm x 6mm x 1.98mm QFN
- Integral Signal Conditioning with Low Pass Filter
- Linear Output
- Ratiometric Performance
- Self-Test
- Robust Design, High Shocks Survivability

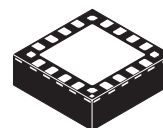
## Typical Applications

- Tilt Monitoring
- Position & Motion Sensing
- Freefall Detection
- Impact Monitoring
- Appliance Control
- Vibration Monitoring and Recording
- Smart Portable Electronics

**MMA6260Q**  
**MMA6261Q**  
**MMA6262Q**  
**MMA6263Q**

**MMA6260Q Series: X-Y AXIS  
SENSITIVITY MICROMACHINED  
ACCELEROMETER**  
**±1.5 g**

**Bottom View**

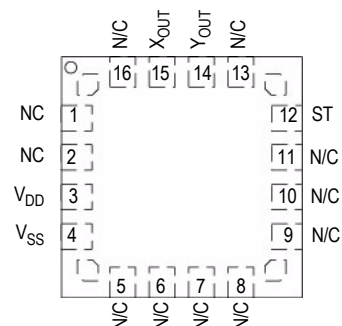


**16-LEAD  
QFN  
CASE 1477-02**

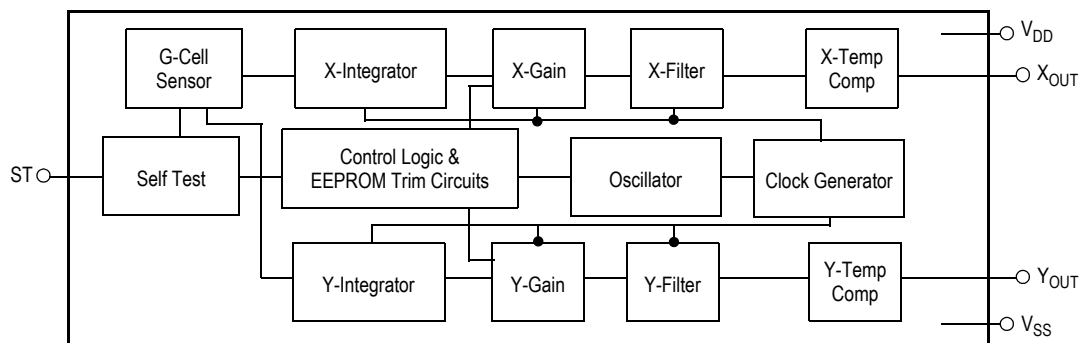
## ORDERING INFORMATION

Device Name	Bandwidth Response	I <sub>DD</sub>	Case No.	Package
MMA6260Q	50 Hz	1.2 mA	1477-02	QFN-16, Tube
MMA6260QR2	50 Hz	1.2 mA	1477-02	QFN-16,Tape & Reel
MMA6261Q	300 Hz	1.2 mA	1477-02	QFN-16, Tube
MMA6261QR2	300 Hz	1.2 mA	1477-02	QFN-16,Tape & Reel
MMA6262Q	150 Hz	2.2 mA	1477-02	QFN-16,Tube
MMA6262QR2	150 Hz	2.2 mA	1477-02	QFN-16,Tape & Reel
MMA6263Q	900 Hz	2.2 mA	1477-02	QFN-16, Tube
MMA6263QR2	900 Hz	2.2 mA	1477-02	QFN-16,Tape & Reel

**Top View**



**Figure 1. Pin Connections**



**Figure 2. Simplified Accelerometer Functional Block Diagram**

**Table 1. Maximum Ratings**

(Maximum ratings are the limits to which the device can be exposed without causing permanent damage.)

Rating	Symbol	Value	Unit
Maximum Acceleration (all axis)	$g_{max}$	$\pm 2000$	g
Supply Voltage	$V_{DD}$	-0.3 to +3.6	V
Drop Test <sup>(1)</sup>	$D_{drop}$	1.2	m
Storage Temperature Range	$T_{stg}$	-40 to +125	°C

1. Dropped onto concrete surface from any axis.

## ELECTRO STATIC DISCHARGE (ESD)

**WARNING:** This device is sensitive to electrostatic discharge.

Although the Freescale accelerometers contain internal 2 kV ESD protection circuitry, extra precaution must be taken by the user to protect the chip from ESD. A charge of over 2000 volts can accumulate on the human body or associated test equipment. A charge of this magnitude can alter the

performance or cause failure of the chip. When handling the accelerometer, proper ESD precautions should be followed to avoid exposing the device to discharges which may be detrimental to its performance.

**Table 2. Operating Characteristics**Unless otherwise noted:  $-20^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ ,  $3.0\text{ V} \leq V_{DD} \leq 3.6\text{ V}$ , Acceleration =  $0g$ , Loaded output <sup>(1)</sup>

Characteristic	Symbol	Min	Typ	Max	Unit
Operating Range <sup>(2)</sup>					
Supply Voltage <sup>(3)</sup>	$V_{DD}$	2.7	3.3	3.6	V
Supply Current					
MMA6260Q, MMA6261Q	$I_{DD}$	—	1.2	1.5	mA
MMA6262Q, MMA6263Q	$I_{DD}$	—	2.2	3.0	mA
Operating Temperature Range	$T_A$	-20	—	+85	$^{\circ}\text{C}$
Acceleration Range	$g_{FS}$	—	1.5	—	g
Output Signal					
Zero g ( $T_A = 25^{\circ}\text{C}$ , $V_{DD} = 3.3\text{ V}$ ) <sup>(4)</sup>	$V_{OFF}$	1.485	1.65	1.815	V
Zero g	$V_{OFF}, T_A$	—	2.0	—	mg/ $^{\circ}\text{C}$
Sensitivity ( $T_A = 25^{\circ}\text{C}$ , $V_{DD} = 3.3\text{ V}$ )	S	740	800	860	mV/g
Sensitivity	S, $T_A$	—	0.015	—	%/ $^{\circ}\text{C}$
Bandwidth Response					
MMA6260Q	$f_{-3dB}$	—	50	—	Hz
MMA6261Q	$f_{-3dB}$	—	300	—	Hz
MMA6262Q	$f_{-3dB}$	—	150	—	Hz
MMA6263Q	$f_{-3dB}$	—	900	—	Hz
Nonlinearity	$NL_{OUT}$	-1.0	—	+1.0	% FSO
Noise					
MMA6260Q RMS (0.1 Hz – 1 kHz)	$n_{RMS}$	—	1.8	—	mVrms
MMA6261Q RMS (0.1 Hz – 1 kHz)	$n_{RMS}$	—	3.5	—	
MMA6262Q RMS (0.1 Hz – 1 kHz)	$n_{RMS}$	—	1.3	—	
MMA6263Q RMS (0.1 Hz – 1 kHz)	$n_{RMS}$	—	2.5	—	
Power Spectral Density RMS (0.1 Hz – 1 kHz)					
MMA6260Q, MMA6261Q	$n_{PSD}$	—	300	—	ug/v/Hz
MMA6262Q, MMA6263Q	$n_{PSD}$	—	200	—	
Self-Test					
Output Response	$V_{ST}$	$0.9 V_{DD}$	—	$V_{DD}$	V
Input Low	$V_{IL}$	—	—	$0.3 V_{DD}$	V
Input High	$V_{IH}$	$0.7 V_{DD}$	—	$V_{DD}$	V
Pull-Down Resistance <sup>(5)</sup>	$R_{PO}$	43	57	71	k $\Omega$
Response Time <sup>(6)</sup>	$t_{ST}$	—	2.0	—	ms
Output Stage Performance					
Full-Scale Output Range ( $I_{OUT} = 200\text{ }\mu\text{A}$ )	$V_{FSO}$	$V_{SS} + 0.25$	—	$V_{DD} - 0.25$	V
Capacitive Load Drive <sup>(7)</sup>	$C_L$	—	—	100	pF
Output Impedance	$Z_O$	—	50	300	$\Omega$
Power-Up Response Time					
MMA6260Q	$t_{RESPONSE}$	—	14	—	ms
MMA6261Q	$t_{RESPONSE}$	—	2.0	—	ms
MMA6262Q	$t_{RESPONSE}$	—	4.0	—	ms
MMA6263Q	$t_{RESPONSE}$	—	0.7	—	ms
Mechanical Characteristics					
Transverse Sensitivity <sup>(8)</sup>	$V_{ZX}, YX, ZY$	-5.0	—	+5.0	% FSO

1. For a loaded output, the measurements are observed after an RC filter consisting of a 1.0 k $\Omega$  resistor and a 0.1  $\mu\text{F}$  capacitor to ground.
2. These limits define the range of operation for which the part will meet specification.
3. Within the supply range of 2.7 and 3.6 V, the device operates as a fully calibrated linear accelerometer. Beyond these supply limits the device may operate as a linear device but is not guaranteed to be in calibration.
4. The device can measure both + and - acceleration. With no input acceleration the output is at midsupply. For positive acceleration the output will increase above  $V_{DD}/2$ . For negative acceleration, the output will decrease below  $V_{DD}/2$ .
5. The digital input pin has an internal pull-down resistance to prevent inadvertent self-test initiation due to external board level leakages.
6. Time for the output to reach 90% of its final value after a self-test is initiated.
7. Preserves phase margin (60 $^{\circ}$ ) to guarantee output amplifier stability.
8. A measure of the device's ability to reject an acceleration applied 90 $^{\circ}$  from the true axis of sensitivity.

## PRINCIPLE OF OPERATION

The Freescale accelerometer is a surface-micromachined integrated-circuit accelerometer.

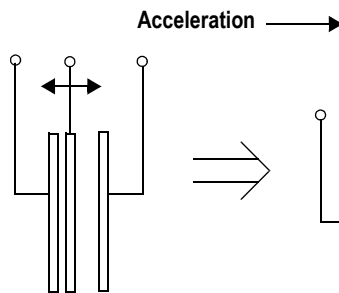
The device consists of a surface micromachined capacitive sensing cell (g-cell) and a signal conditioning ASIC contained in a single integrated circuit package. The sensing element is sealed hermetically at the wafer level using a bulk micromachined *cap wafer*.

The g-cell is a mechanical structure formed from semiconductor materials (polysilicon) using semiconductor processes (masking and etching). It can be modeled as a set of beams attached to a movable central mass that moves between fixed beams. The movable beams can be deflected from their rest position by subjecting the system to an acceleration (Figure 3).

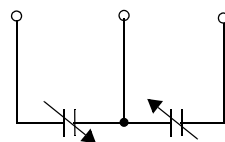
As the beams attached to the central mass move, the distance from them to the fixed beams on one side will increase by the same amount that the distance to the fixed beams on the other side decreases. The change in distance is a measure of acceleration.

The g-cell plates form two back-to-back capacitors (Figure 4). As the center plate moves with acceleration, the distance between the plates changes and each capacitor's value will change, ( $C = A\epsilon/D$ ). Where A is the area of the plate,  $\epsilon$  is the dielectric constant, and D is the distance between the plates.

The ASIC uses switched capacitor techniques to measure the g-cell capacitors and extract the acceleration data from the difference between the two capacitors. The ASIC also signal conditions and filters (switched capacitor) the signal, providing a high level output voltage that is ratiometric and proportional to acceleration.



**Figure 3. Transducer Physical Model**



**Figure 4. Equivalent Circuit Model**

## SPECIAL FEATURES

### Filtering

These Freescale accelerometers contain an onboard single-pole switched capacitor filter. Because the filter is realized using switched capacitor techniques, there is no requirement for external passive components (resistors and capacitors) to set the cut-off frequency.

### Self-Test

The sensor provides a self-test feature allowing the verification of the mechanical and electrical integrity of the accelerometer at any time before or after installation. A fourth plate is used in the g-cell as a self-test plate. When a logic high input to the self-test pin is applied, a calibrated potential is applied across the self-test plate and the moveable plate. The resulting electrostatic force ( $F_e = \frac{1}{2} AV^2/d^2$ ) causes the center plate to deflect. The resultant deflection is measured by the accelerometer's ASIC and a proportional output voltage results. This procedure assures both the mechanical (g-cell) and electronic sections of the accelerometer are functioning.

Freescale accelerometers include fault detection circuitry and a fault latch. Parity of the EEPROM bits becomes odd in number.

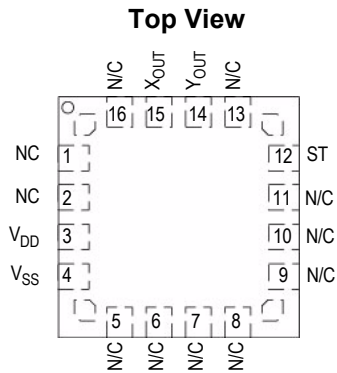
Self-test is disabled when EEPROM parity error occurs.

### Ratiometricity

Ratiometricity simply means the output offset voltage and sensitivity will scale linearly with applied supply voltage. That is, as supply voltage is increased, the sensitivity and offset increase linearly; as supply voltage decreases, offset and sensitivity decrease linearly. This is a key feature when interfacing to a microcontroller or an A/D converter because it provides system level cancellation of supply induced errors in the analog to digital conversion process.

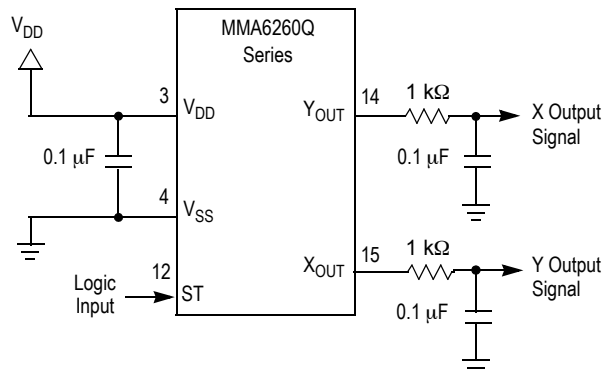
## BASIC CONNECTIONS

### Pinout Description



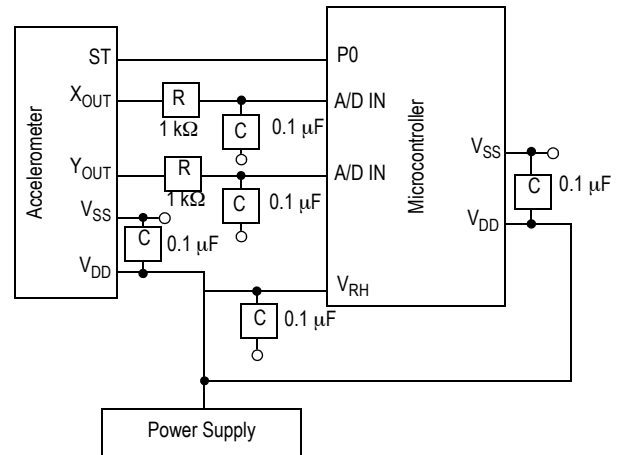
**Figure 4. Pinout Description**

Pin No.	Pin Name	Description
1, 5 – 7, 13, 16	N/C	No internal connection. Leave unconnected.
14	Y <sub>OUT</sub>	Output voltage of the accelerometer. Y Direction.
15	X <sub>OUT</sub>	Output voltage of the accelerometer. X Direction.
3	V <sub>DD</sub>	Power supply input.
4	V <sub>SS</sub>	The power supply ground.
2, 8 – 11	N/C	Used for factory trim. Leave unconnected.
12	ST	Logic input pin used to initiate self-test.



**Figure 5. Accelerometer with Recommended Connection Diagram**

### PCB Layout

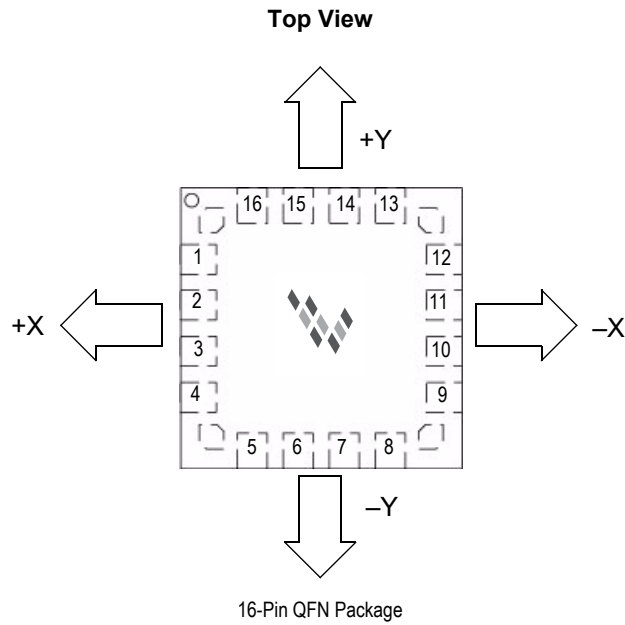


**Figure 6. Recommend PCB Layout for Interfacing Accelerometer to Microcontroller**

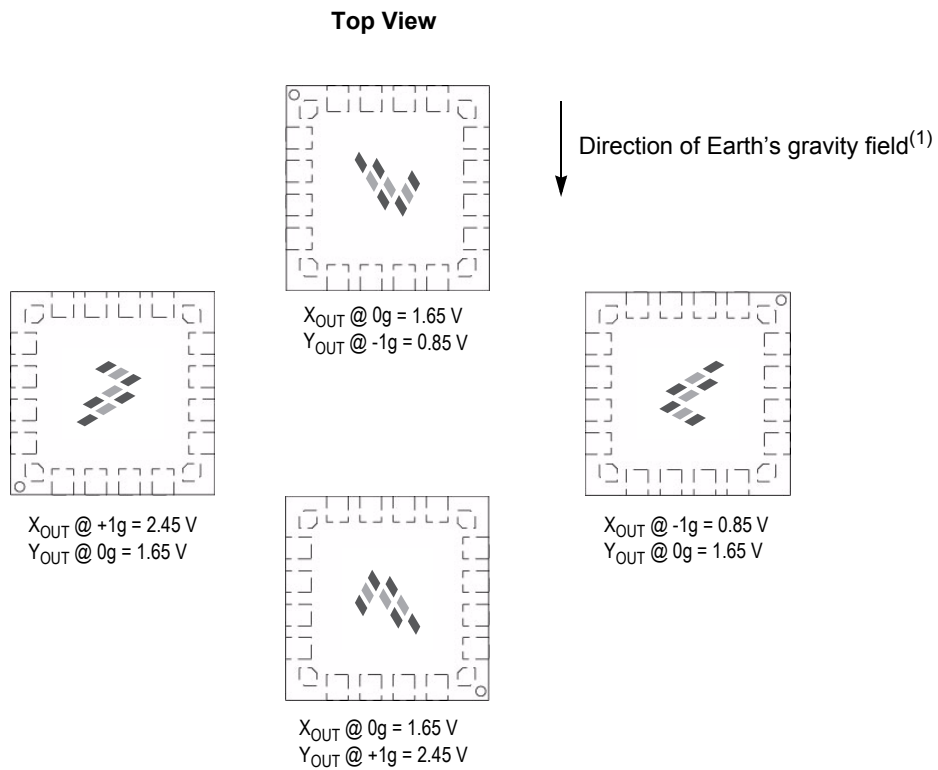
#### NOTES:

1. Use 0.1 µF capacitor on V<sub>DD</sub> to decouple the power source.
2. Physical coupling distance of the accelerometer to the microcontroller should be minimal.
3. Flag underneath package is connected to ground.
4. Place a ground plane beneath the accelerometer to reduce noise, the ground plane should be attached to all of the open ended terminals shown in [Figure 6](#).
5. Use an RC filter with 1.0 kΩ and 0.1 µF on the outputs of the accelerometer to minimize clock noise (from the switched capacitor filter circuit).
6. PCB layout of power and ground should not couple power supply noise.
7. Accelerometer and microcontroller should not be a high current path.
8. A/D sampling rate and any external power supply switching frequency should be selected such that they do not interfere with the internal accelerometer sampling frequency (16 kHz for Low I<sub>DD</sub> and 52 kHz for Standard I<sub>DD</sub> for the sampling frequency). This will prevent aliasing errors.
9. PCB layout should not run traces or vias under the QFN part. This could lead to ground shorting to the accelerometer flag.

## DYNAMIC ACCELERATION



## STATIC ACCELERATION

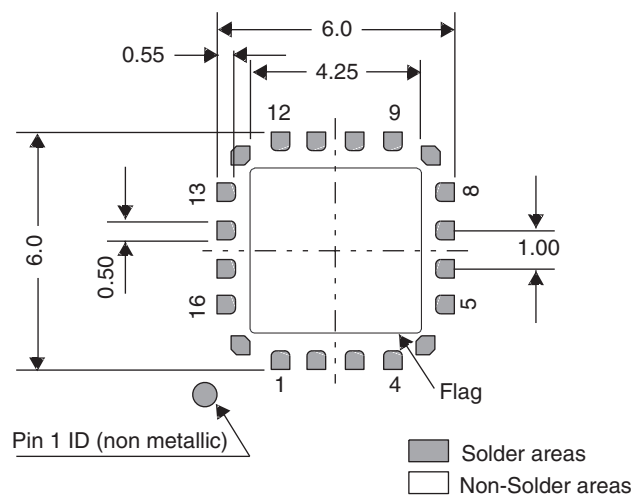


1. When positioned as shown, the Earth's gravity will result in a positive 1g output.

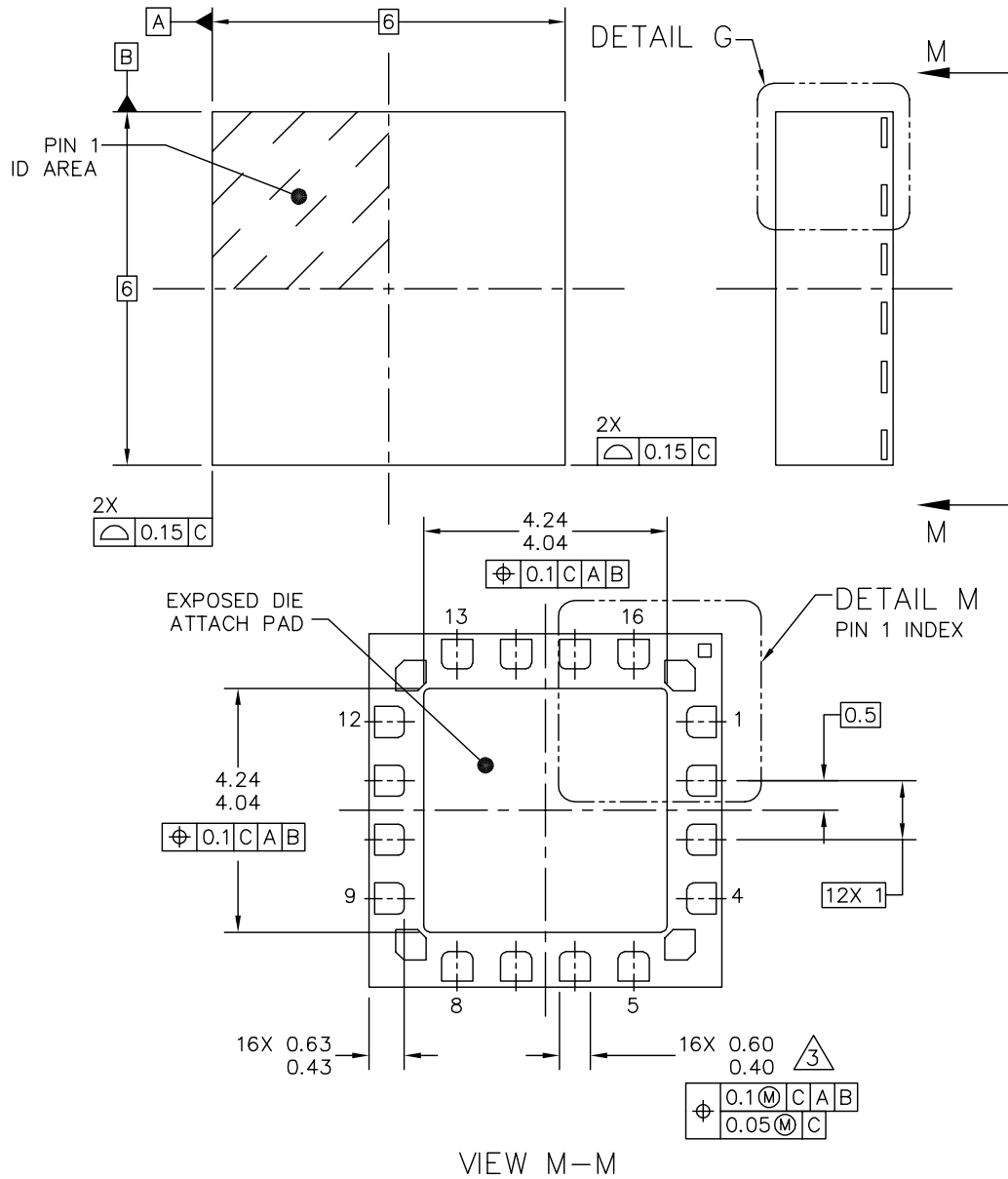
## MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the surface mount packages must be the correct size to ensure proper solder connection interface between the board and the package.

With the correct footprint, the packages will self-align when subjected to a solder reflow process. It is always recommended to design boards with a solder mask layer to avoid bridging and shorting between solder pads.



## PACKAGE DIMENSIONS



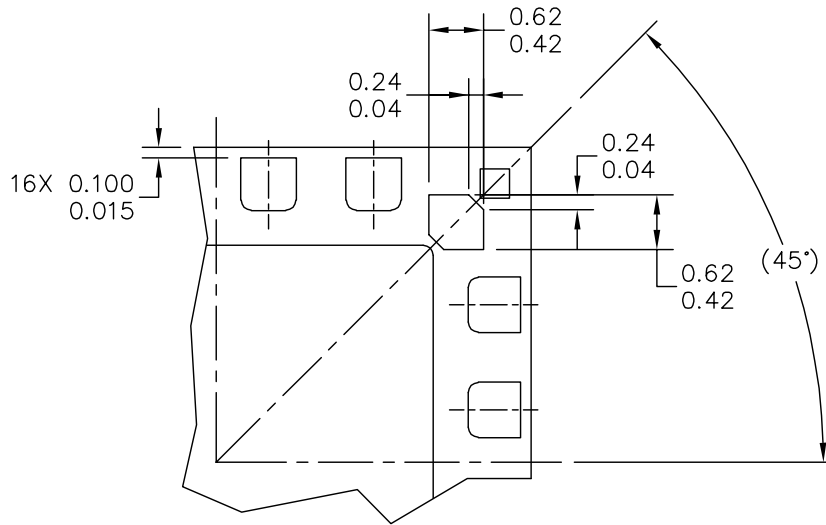
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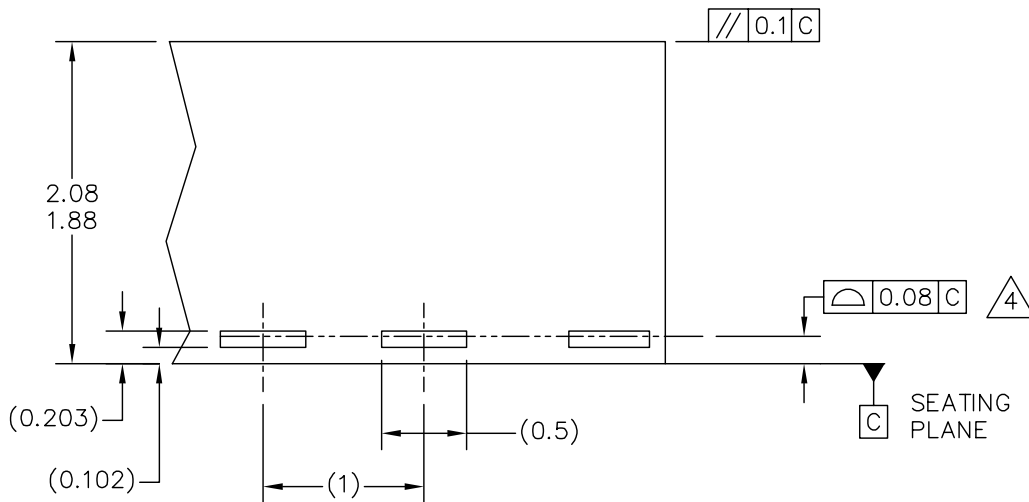
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16-LEAD QFN**



## PACKAGE DIMENSIONS



DETAIL M



DETAIL G  
VIEW ROTATED 90° CW

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16-LEAD QFN**

**MMA6260Q**

## PACKAGE DIMENSIONS

### NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
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3. THIS DIMENSION APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25MM AND 0.30MM FROM TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED HEAT SLUG, TERMINALS AND CORNER PADS.
5. RADIUS ON TERMINAL IS OPTIONAL.
6. MINIMUM METAL GAP SHOULD BE 0.2MM EXCEPT GAP BETWEEN CORNER PADS AND THE EXPOSED HEAT SLUG.

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