

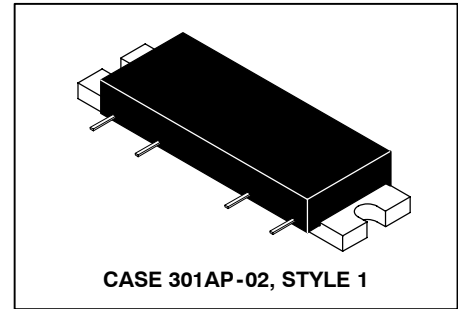
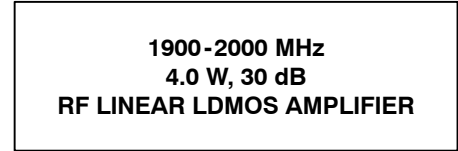
PCS Band RF Linear LDMOS Amplifier

Designed for ultra-linear amplifier applications in 50 ohm systems operating in the PCS frequency band. A silicon FET Class A design provides outstanding linearity and gain. In addition, the excellent group delay and phase linearity characteristics are ideal for digital modulation systems, such as TDMA and CDMA.

- Third Order Intercept: 46 dBm Typ
- Power Gain: 30 dB Typ (@ f = 1960 MHz)
- Input VSWR ≤ 1.5:1

Features

- Excellent Phase Linearity and Group Delay Characteristics
- Ideal for Feedforward Base Station Applications
- RoHS Compliant



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Table 1. Absolute Maximum Ratings (T_C = 25°C unless otherwise noted)

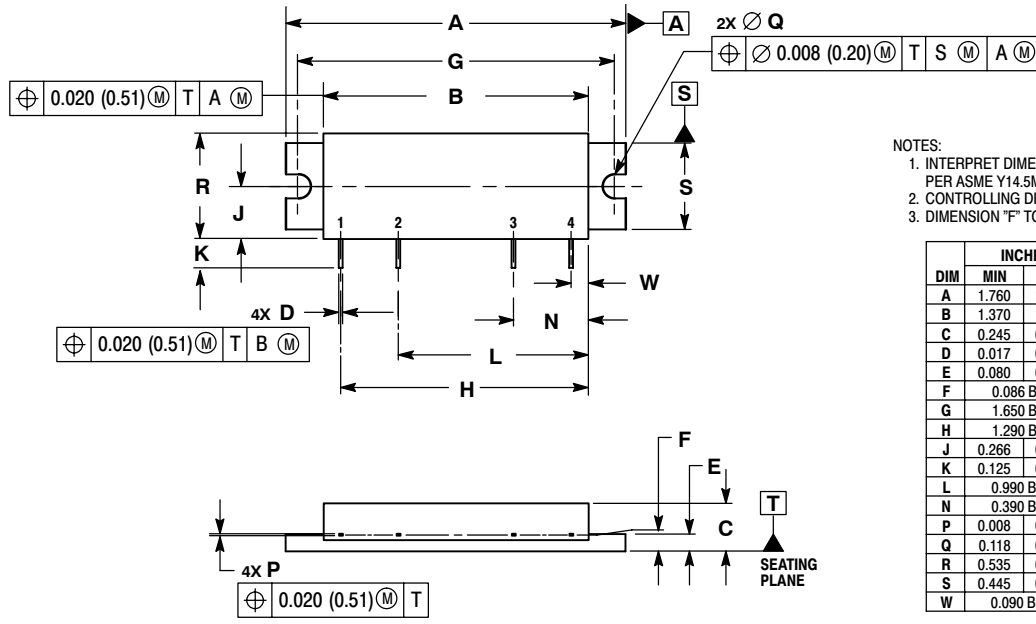
Rating	Symbol	Value	Unit
DC Supply Voltage	V _{DD}	30	Vdc
RF Input Power	P _{in}	+10	dBm
Storage Temperature Range	T _{stg}	- 40 to +100	°C
Operating Case Temperature Range	T _C	- 20 to +100	°C

Table 2. Electrical Characteristics (V_{DD} = 28 Vdc, T_C = 25°C; 50 Ω System)

Characteristic	Symbol	Min	Typ	Max	Unit
Supply Current	I _{DD}	—	500	525	mA
Power Gain (f = 1960 MHz)	G _p	29	30	32	dB
Gain Flatness (f = 1900 - 2000 MHz)	G _F	—	0.1	0.4	dB
Power Output @ 1 dB Compression (f = 1950 MHz)	P1dB	35	36	—	dBm
Third Order Intercept (f1 = 1950 MHz, f2 = 1955 MHz)	ITO	45	46	—	dBm
Noise Figure (f = 2000 MHz)	NF	—	4.2	4.5	dB

NOTE - CAUTION - MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

PACKAGE DIMENSIONS



- NOTES:
 1. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
 2. CONTROLLING DIMENSION: INCH.
 3. DIMENSION "F" TO CENTER OF LEADS.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.760	1.780	44.70	45.21
B	1.370	1.390	34.80	35.31
C	0.245	0.265	6.22	6.73
D	0.017	0.023	0.43	0.58
E	0.080	0.100	2.03	2.54
F	0.086 BSC		2.18 BSC	
G	1.650 BSC		41.91 BSC	
H	1.290 BSC		32.77 BSC	
J	0.266	0.280	6.76	7.11
K	0.125	0.165	3.18	4.19
L	0.990 BSC		25.15 BSC	
N	0.390 BSC		9.91 BSC	
P	0.008	0.013	0.20	0.33
Q	0.118	0.132	3.00	3.35
R	0.535	0.555	13.59	14.10
S	0.445	0.465	11.30	11.81
W	0.090 BSC		2.29 BSC	

- STYLE 1:
 PIN 1: RF INPUT
 2: VDD1
 3: VDD2
 4: RF OUTPUT
 CASE: GROUND

**CASE 301AP-02
 ISSUE E**

REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
0	Dec. 2006	<ul style="list-style-type: none">Initial Release of Data Sheet

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