

Advance Information

128K x 8 Bit Fast Static Random Access Memory

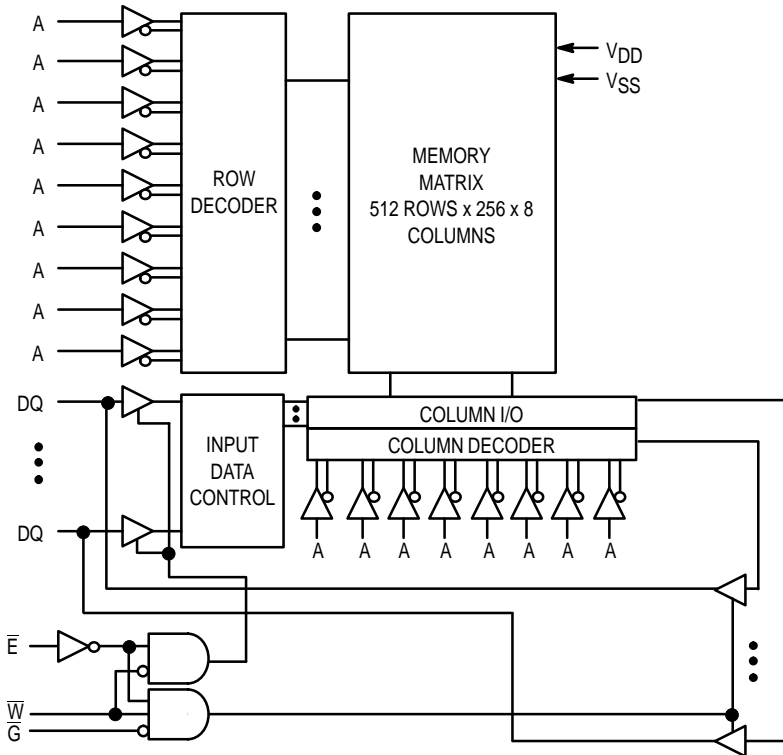
The MCM6926A is a 1,048,576 bit static random access memory organized as 131,072 words of 8 bits. Static design eliminates the need for external clocks or timing strobes.

Output enable (\bar{G}) is a special control feature that provides increased system flexibility and eliminates bus contention problems.

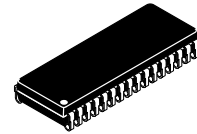
This device meets JEDEC standards for functionality and revolutionary pinout, and is available in a 400 mil plastic small-outline J-leaded package.

- Single 3.3 V Power Supply
- Fully Static — No Clock or Timing Strokes Necessary
- All Inputs and Outputs Are TTL Compatible
- Three State Outputs
- Fast Access Times: 8, 10, 12, 15 ns
- Center Power and I/O Pins for Reduced Noise
- Fully 3.3 V BiCMOS

BLOCK DIAGRAM



MCM6926A



WJ PACKAGE
400 MIL SOJ
CASE 857A-02

PIN ASSIGNMENT

A	1	32	A
A	2	31	A
A	3	30	A
A	4	29	A
\bar{E}	5	28	\bar{G}
DQ	6	27	DQ
DQ	7	26	DQ
VDD	8	25	VSS
VSS	9	24	VDD
DQ	10	23	DQ
DQ	11	22	DQ
\bar{W}	12	21	A
A	13	20	A
A	14	19	A
A	15	18	A
A	16	17	A

PIN NAMES

A	Address Input
\bar{E}	Chip Enable
\bar{W}	Write Enable
\bar{G}	Output Enable
DQ	Data Input/Output
VDD	+ 3.3 V Power Supply
VSS	Ground

This document contains information on a new product. Motorola reserves the right to change or discontinue this product without notice.

REV 2
8/14/98

TRUTH TABLE (X = Don't Care)

\bar{E}	\bar{G}	\bar{W}	Mode	V _{DD} Current	Output	Cycle
H	X	X	Not Selected	I _{SB1} , I _{SB2}	High-Z	—
L	H	H	Output Disabled	I _{DDA}	High-Z	—
L	L	H	Read	I _{DDA}	D _{out}	Read Cycle
L	X	L	Write	I _{DDA}	High-Z	Write Cycle

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V _{DD}	- 0.5 to + 4.6	V
Voltage Relative to V _{SS} for Any Pin Except V _{DD}	V _{in} , V _{out}	- 0.5 to V _{DD} + 0.5	V
Output Current	I _{out}	± 30	mA
Power Dissipation	P _D	0.6	W
Temperature Under Bias	T _{bias}	- 10 to + 85	°C
Operating Temperature	T _A	0 to + 70	°C
Storage Temperature — Plastic	T _{stg}	- 55 to + 125	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high-impedance circuits.

This BiCMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{DD} = 3.3 V + 10%, - 5%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V _{DD}	3.135	3.3	3.6	V
Input High Voltage	V _{IH}	2.2	—	V _{DD} + 0.3**	V
Input Low Voltage	V _{IL}	- 0.5*	—	0.8	V

* V_{IL} (min) = - 0.5 V dc; V_{IL} (min) = - 2.0 V ac (pulse width ≤ 2.0 ns) for I ≤ 20.0 mA.

** V_{IH} (max) = V_{DD} + 0.3 V dc; V_{IH} (max) = V_{DD} + 2 V ac (pulse width ≤ 2.0 ns) for I ≤ 20.0 mA.

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V _{in} = 0 to V _{DD})	I _{lkg(I)}	—	± 1.0	μA
Output Leakage Current (\bar{E} = V _{IH} , V _{out} = 0 to V _{DD})	I _{lkg(O)}	—	± 1.0	μA
Output Low Voltage (I _{OL} = + 8.0 mA)	V _{OL}	—	0.4	V
Output High Voltage (I _{OH} = - 4.0 mA)	V _{OH}	2.4	—	V

Freescale Semiconductor, Inc.

POWER SUPPLY CURRENTS (See Note 1)

Parameter	Symbol	6926A-8		6926A-10		6926A-12		6926A-15		Unit	Notes
		Typ	Max	Typ	Max	Typ	Max	Typ	Max		
AC Active Supply Current ($I_{out} = 0$ mA) ($V_{DD} = \max$, $f = f_{max}$)	I_{DDA}	—	100	—	100	—	100	—	100	mA	2, 3, 4
Active Quiescent Current ($\bar{E} = V_{IL}$, $V_{DD} = \max$, $f = 0$ MHz)	I_{DD2}	—	80	—	80	—	80	—	80	mA	
AC Standby Current ($\bar{E} = V_{IH}$, $V_{DD} = \max$, $f = f_{max}$)	I_{SB1}	—	50	—	45	—	40	—	35	mA	2, 3, 4
CMOS Standby Current ($V_{DD} = \max$, $f = 0$ MHz, $\bar{E} \geq V_{DD} - 0.2$ V, $V_{in} \leq V_{SS} + 0.2$ V, or $\geq V_{DD} - 0.2$ V)	I_{SB2}	—	20	—	20	—	20	—	20	mA	

NOTES:

1. Typical current = 25°C @ 3.3 V.
2. Reference AC Operating Conditions and Characteristics for input and timing (V_{IH}/V_{IL} , t_r/t_f , pulse level 0 to 3.0 V, $V_{IH} = 3.0$ V).
3. All address transition simultaneously low (LSB) and then high (MSB).
4. Data states are all zero.

CAPACITANCE ($f = 1.0$ MHz, $dV = 3.0$ V, $T_A = 25^\circ\text{C}$, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Typ	Max	Unit
Address Input Capacitance	C_{in}	—	6	pF
Control Pin Input Capacitance	C_{in}	—	6	pF
Input/Output Capacitance	$C_{I/O}$	—	8	pF

Freescale Semiconductor, Inc.

AC OPERATING CONDITIONS AND CHARACTERISTICS

($V_{DD} = 3.3\text{ V} + 10\%, -5\%$, $T_A = 0\text{ to }+70^\circ\text{C}$, Unless Otherwise Noted)

Input Timing Measurement Reference Level 1.5 V
 Input Pulse Levels 0 to 3.0 V
 Input Rise/Fall Time 2 ns

Output Timing Measurement Reference Level 1.5 V
 Output Load See Figure 1

READ CYCLE TIMING (See Notes 1 and 2)

Parameter	Symbol	6926A-8		6926A-10		6926A-12		6926A-15		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	8	—	10	—	12	—	15	—	ns	3
Address Access Time	t_{AVQV}	—	8	—	10	—	12	—	15	ns	
Enable Access Time	t_{ELQV}	—	8	—	10	—	12	—	15	ns	
Output Enable Access Time	t_{GLQV}	—	4	—	5	—	6	—	7	ns	
Output Hold from Address Change	t_{AXQX}	3	—	3	—	3	—	3	—	ns	
Enable Low to Output Active	t_{ELQX}	3	—	3	—	3	—	3	—	ns	4, 5, 6
Output Enable Low to Output Active	t_{GLQX}	0	—	0	—	0	—	0	—	ns	4, 5, 6
Enable High to Output High-Z	t_{EHQZ}	—	4	—	5	—	6	—	7	ns	4, 5, 6
Output Enable High to Output High-Z	t_{GHQZ}	—	4	—	5	—	6	—	7	ns	4, 5, 6

NOTES:

- \bar{W} is high for read cycle.
- For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycles.
- All read cycle timings are referenced from the last valid address to the first transitioning address.
- At any given voltage and temperature, $t_{EHQZ}\text{ max} < t_{ELQX}\text{ min}$, and $t_{GHQZ}\text{ max} < t_{GLQX}\text{ min}$, both for a given device and from device to device.
- Transition is measured 200 mV from steady-state voltage.
- This parameter is sampled and not 100% tested.
- Device is continuously selected ($\bar{E} = V_{IL}$, $\bar{G} = V_{IL}$).
- Addresses valid prior to or coincident with \bar{E} going low.

TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time. On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

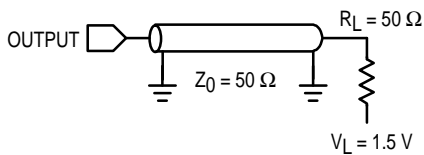
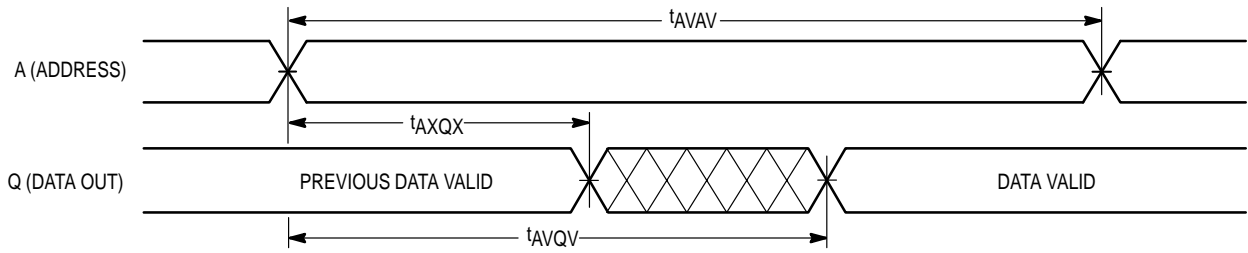


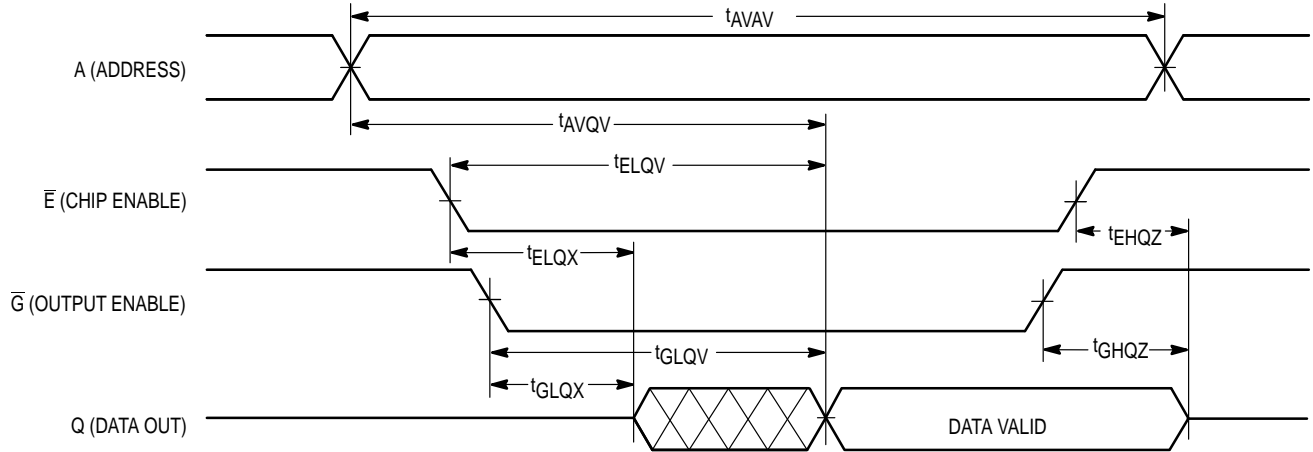
Figure 1. AC Test Load

Freescale Semiconductor, Inc.

READ CYCLE 1 (See Note 7)



READ CYCLE 2 (See Note 8)



Freescale Semiconductor, Inc.

Freescale Semiconductor, Inc.

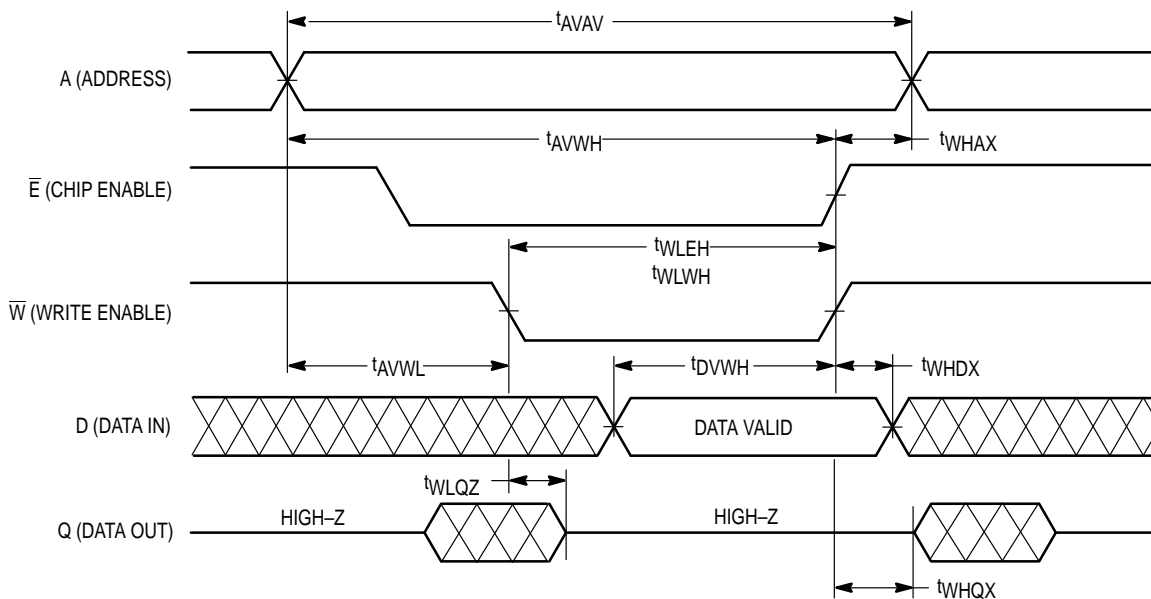
WRITE CYCLE 1 (\overline{W} Controlled, See Notes 1 and 2)

Parameter	Symbol	6926A-8		6926A-10		6926A-12		6926A-15		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	8	—	10	—	12	—	15	—	ns	3
Address Setup Time	t_{AVWL}	0	—	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVWH}	8	—	9	—	10	—	12	—	ns	
Address Valid to End of Write, \overline{C} High	t_{AVWH}	7	—	8	—	9	—	10	—	ns	
Write Pulse Width	t_{WLWH} , t_{WLEH}	8	—	9	—	10	—	12	—	ns	
Write Pulse Width, \overline{C} High	t_{WLWH} , t_{WLEH}	7	—	8	—	9	—	10	—	ns	
Data Valid to End of Write	t_{DVWH}	4	—	5	—	6	—	7	—	ns	
Data Hold Time	t_{WHDX}	0	—	0	—	0	—	0	—	ns	
Write Low to Data High-Z	t_{WLQZ}	—	3.5	—	3.5	—	3.5	—	3.5	ns	4, 5, 6
Write High to Output Active	t_{WHQX}	3	—	3	—	3	—	3	—	ns	4, 5, 6
Write Recovery Time	t_{WHAX}	0	—	0	—	0	—	0	—	ns	

NOTES:

1. A write occurs during the overlap of \overline{E} low and \overline{W} low.
2. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycles.
3. All write cycle timings are referenced from the last valid address to the first transitioning address.
4. Transition is measured 200 mV from steady-state voltage.
5. This parameter is sampled and not 100% tested.
6. At any given voltage and temperature, $t_{WLQZ} \text{ max} < t_{WHQX} \text{ min}$ both for a given device and from device to device.

WRITE CYCLE 1



Freescale Semiconductor, Inc.

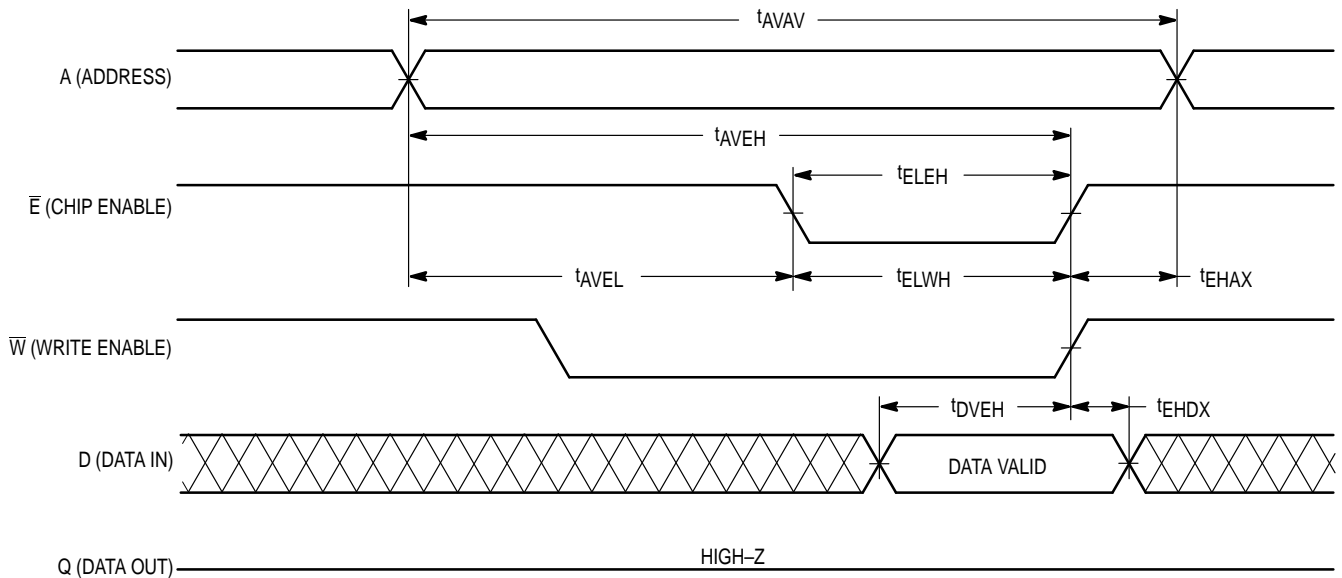
WRITE CYCLE 2 (\bar{E} Controlled, See Notes 1 and 2)

Parameter	Symbol	6926A-8		6926A-10		6926A-12		6926A-15		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	8	—	10	—	12	—	15	—	ns	3
Address Setup Time	t_{AVEL}	0	—	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVEH}	7	—	8	—	9	—	10	—	ns	
Enable to End of Write	t_{ELEH} , t_{ELWH}	7	—	8	—	9	—	10	—	ns	4,5
Data Valid to End of Write	t_{DVEH}	4	—	5	—	6	—	7	—	ns	
Data Hold Time	t_{EHDH}	0	—	0	—	0	—	0	—	ns	
Write Recovery Time	t_{EHAX}	0	—	0	—	0	—	0	—	ns	

NOTES:

1. A write occurs during the overlap of \bar{E} low and \bar{W} low.
2. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycles.
3. All write cycle timings are referenced from the last valid address to the first transitioning address.
4. If \bar{E} goes low coincident with or after \bar{W} goes low, the output will remain in a high impedance condition.
5. If \bar{E} goes high coincident with or before \bar{W} goes high, the output will remain in a high impedance condition.

WRITE CYCLE 2



ORDERING INFORMATION (Order by Full Part Number)

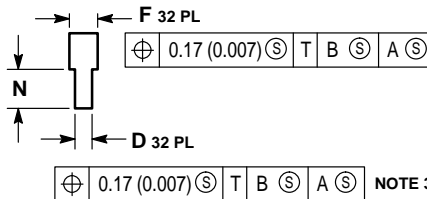
MCM 6926A WJ XX X
 Motorola Memory Prefix _____
 Part Number _____
 Shipping Method (R = Tape and Reel, Blank = Rails)
 Speed (8 = 8 ns, 10 = 10 ns, 12 = 12 ns, 15 = 15 ns)
 Package (WJ = 400 mil SOJ)

Full Part Numbers — MCM6926AWJ8 MCM6926AWJ10 MCM6926AWJ12 MCM6926AWJ15
 MCM6926AWJ8R MCM6926AWJ10R MCM6926AWJ12R MCM6926AWJ15R

Freescale Semiconductor, Inc.

PACKAGE DIMENSIONS

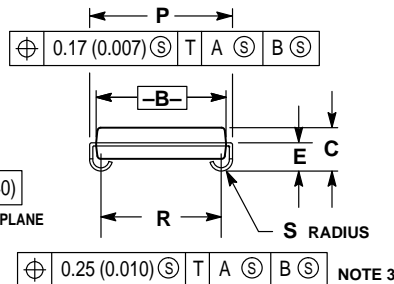
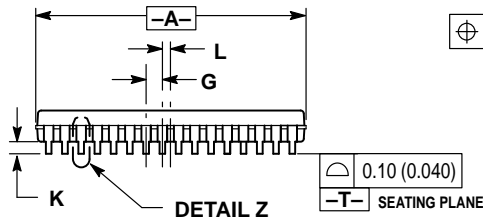
32-LEAD
400 MIL SOJ
CASE 857A-02



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. TO BE DETERMINED AT PLANE -T-.
4. DIMENSION A AND D DO NOT INCLUDE MOLD PROTRUSION. MOLD PROTRUSION SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
5. DIMENSION A AND B INCLUDE MOLD MISMATCH AND ARE DETERMINED AT THE PARTING LINE.

DETAIL Z



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.820	0.830	20.83	21.08
B	0.395	0.405	10.03	10.29
C	0.128	0.148	3.26	3.75
D	0.016	0.020	0.41	0.50
E	0.088	0.098	2.24	2.48
F	0.026	0.032	0.67	0.81
G	0.050 BSC		1.27 BSC	
K	0.035	0.045	0.89	1.14
L	0.025 BSC		0.64 BSC	
N	0.030	0.045	0.76	1.14
P	0.435	0.445	11.05	11.30
R	0.365	0.375	9.27	9.52
S	0.030	0.040	0.77	1.01

Motorola reserves the right to make changes without further notice to any products herein. Motorola makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Motorola assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters which may be provided in Motorola data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. Motorola does not convey any license under its patent rights nor the rights of others. Motorola products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Motorola product could create a situation where personal injury or death may occur. Should Buyer purchase or use Motorola products for any such unintended or unauthorized application, Buyer shall indemnify and hold Motorola and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Motorola was negligent regarding the design or manufacture of the part. Motorola and are registered trademarks of Motorola, Inc. Motorola, Inc. is an Equal Opportunity/Affirmative Action Employer.

Mfax is a trademark of Motorola, Inc.

How to reach us:

USA/EUROPE/Locations Not Listed: Motorola Literature Distribution;
P.O. Box 5405, Denver, Colorado, 80217. 1-303-675-2140 or 1-800-441-2447

JAPAN: Nippon Motorola Ltd.; SPD, Strategic Planning Office, 141,
4-32-1 Nishi-Gotanda, Shinagawa-ku, Tokyo, Japan. 81-3-5487-8488

Mfax™: RMFAX0@email.sps.mot.com – TOUCHTONE 1-602-244-6609
Motorola Fax Back System – US & Canada ONLY 1-800-774-1848
– http://sps.motorola.com/mfax/

ASIA/PACIFIC: Motorola Semiconductors H.K. Ltd.; 8B Tai Ping Industrial Park,
51 Ting Kok Road, Tai Po, N.T., Hong Kong. 852-26629298

HOME PAGE : <http://motorola.com/sps/>

CUSTOMER FOCUS CENTER: 1-800-521-6274



For More Information On This Product,
Go to: www.freescale.com

MCM6926A/D

Freescale Semiconductor, Inc.