μPA2593

MOS FIELD EFFECT TRANSISTOR

R07DS0012EJ0200
Rev.2.00
Sep 10, 2010

Description

The μPA2593 is N- and P-channel MOSFETs designed for DC/DC converters and power management applications of portable equipments.

N- and P-channel MOSFETs are assembled in one package, to contribute minimize the equipments.

Features

- 4.5 V drive available
- Low on-state resistance
  N-channel
  — $R_{DS(on)1}$ = 58 mΩ MAX. (V_{GS} = 10 V, I_D = 2 A)
  — $R_{DS(on)2}$ = 103 mΩ MAX. (V_{GS} = 4.5 V, I_D = 2 A)
  P-channel
  — $R_{DS(on)1}$ = 140 mΩ MAX. (V_{GS} = –10 V, I_D = –2 A)
  — $R_{DS(on)2}$ = 195 mΩ MAX. (V_{GS} = –4.5 V, I_D = –2 A)
- Built-in gate protection diode
- Small and surface mount package (8-pin VSOF (2429))

Ordering Information

Part No.	LEAD PLATING	PACKING	Package
μPA2593T1H-T1-AT *1	Pure Sn (Tin)	8 mm embossed taping 3000 p/reel	8-pin VSOF (2429)
μPA2593T1H-T2-AT *1			

Note: *1. Pb-free (This product does not contain Pb in the external electrode and other parts.)
Marking: 2593

Absolute Maximum Ratings (T_A = 25°C)

Item	Symbol	N-CHANNEL	P-CHANNEL	Unit
Drain to Source Voltage (V_{GS} = 0 V)	V_{DSS}	40	–40	V
Gate to Source Voltage (V_{DS} = 0 V)	V_{GSS}	±18	∓18	V
Drain Current (DC)	$I_{D(DC)}$	±4.5	∓3.5	A
Drain Current (pulse) *1	$I_{D(pulse)}$	±18	∓18	A
Total Power Dissipation (1 unit, 5 s) *2	P_{T1}	1.5		W
Total Power Dissipation (2 unit, 5 s) *2	P_{T2}	1.24		W
Channel Temperature	T_{ch}	150		°C
Storage Temperature	T_{stg}	–55 to +150		°C

Notes: *1. PW ≤ 10 μs, Duty Cycle ≤ 1%
*2. Mounted on FR-4 board of 25.4 mm x 25.4 mm x 0.8 mmt

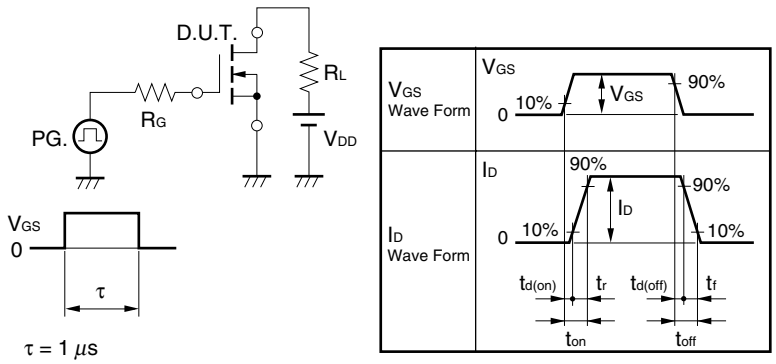
Electrical Characteristics (T_A = 25°C)

N-channel MOSFET

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Zero Gate Voltage Drain Current	I_{DSS}			1	μA	V_{DS} = 40 V, V_{GS} = 0 V
Gate Leakage Current	I_{GSS}			±10	μA	V_{GS} = ±14 V, V_{DS} = 0 V
Gate Cut-off Voltage	$V_{GS(off)}$	1.0		2.5	V	V_{DS} = 10 V, I_D = 1 mA
Forward Transfer Admittance *1	$\|y_{fs}\|$	2.0			S	V_{DS} = 5 V, I_D = 2 A
Drain to Source On-state Resistance *1	$R_{DS(on)1}$		50	58	mΩ	V_{GS} = 10 V, I_D = 2 A
	$R_{DS(on)2}$		70	103	mΩ	V_{GS} = 4.5 V, I_D = 2 A
Input Capacitance	C_{iss}		315		pF	V_{DS} = 10 V,
Output Capacitance	C_{oss}		70		pF	V_{GS} = 0 V,
Reverse Transfer Capacitance	C_{rss}		38		pF	f = 1 MHz
Turn-on Delay Time	$t_{d(on)}$		5		ns	V_{DD} = 20 V, I_D = 2 A,
Rise Time	t_r		3		ns	V_{GS} = 10 V,
Turn-off Delay Time	$t_{d(off)}$		21		ns	R_G = 6 Ω
Fall Time	t_f		3		ns	
Total Gate Charge	Q_G		7		nC	V_{DD} = 32 V, V_{GS} = 10 V, I_D = 4.5 A
Body Diode Forward Voltage *1	$V_{F(S-D)}$		0.9		V	I_F = 4.5 A, V_{GS} = 0 V

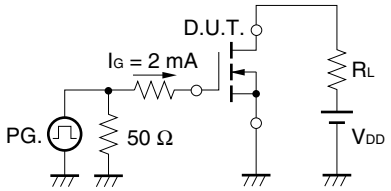
Note: *1. Pulsed

TEST CIRCUIT 1 SWITCHING TIME



τ = 1 μs
Duty Cycle ≤ 1%

TEST CIRCUIT 2 GATE CHARGE

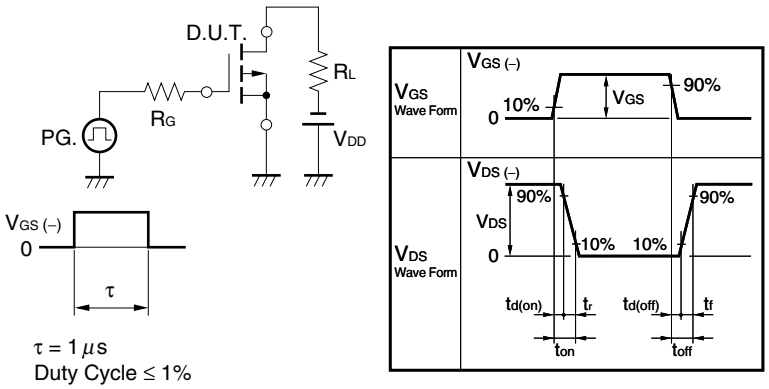


P-channel MOSFET

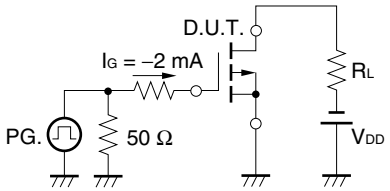
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Zero Gate Voltage Drain Current	I_{DSS}			−1	μA	V_{DS} = −40 V, V_{GS} = 0 V
Gate Leakage Current	I_{GSS}			∓10	μA	V_{GS} = ∓14 V, V_{DS} = 0 V
Gate Cut-off Voltage	$V_{GS(off)}$	−1.0		−2.5	V	V_{DS} = −10 V, I_D = −1 mA
Forward Transfer Admittance *1	$\|y_{fs}\|$	2.0			S	V_{DS} = −5 V, I_D = −2 A
Drain to Source On-state Resistance *1	$R_{DS(on)1}$		115	140	mΩ	V_{GS} = −10 V, I_D = −2 A
	$R_{DS(on)2}$		135	195	mΩ	V_{GS} = −4.5 V, I_D = −2 A
Input Capacitance	C_{iss}		350		pF	V_{DS} = −10 V,
Output Capacitance	C_{oss}		60		pF	V_{GS} = 0 V,
Reverse Transfer Capacitance	C_{rss}		47		pF	f = 1 MHz
Turn-on Delay Time	$t_{d(on)}$		5.5		ns	V_{DD} = −20 V, I_D = −2 A,
Rise Time	t_r		3.5		ns	V_{GS} = −10 V,
Turn-off Delay Time	$t_{d(off)}$		40		ns	R_G = 6 Ω
Fall Time	t_f		8		ns	
Total Gate Charge	Q_G		8		nC	V_{DD} = −32 V, V_{GS} = −10 V I_D = −3.5 A
Body Diode Forward Voltage *1	$V_{F(S-D)}$		0.95		V	I_F = −3.5 A, V_{GS} = 0 V

Note: *1. Pulsed

TEST CIRCUIT 1 SWITCHING TIME



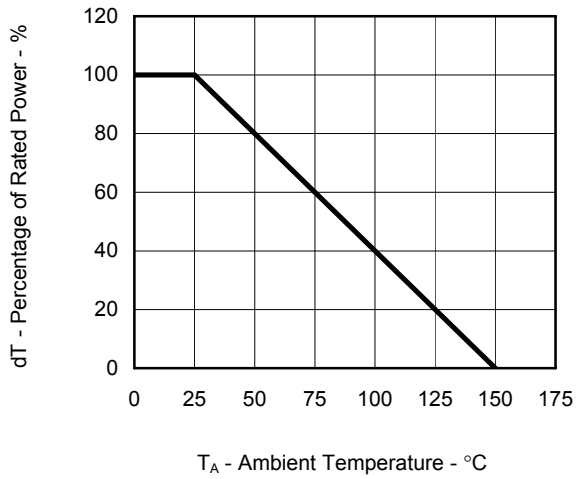
TEST CIRCUIT 2 GATE CHARGE



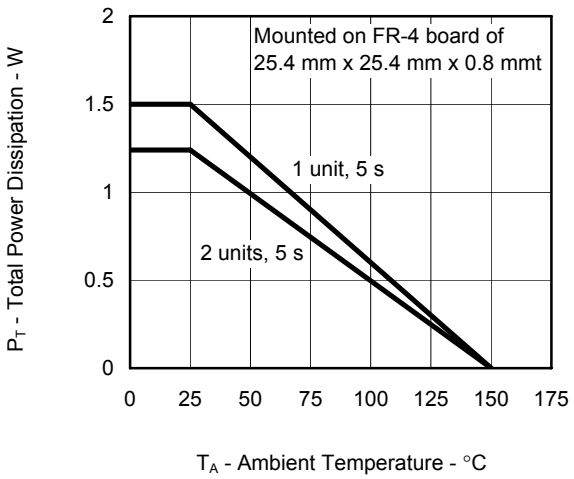
Typical Characteristics (T_A = 25°C)

(1) N-channel MOSFET

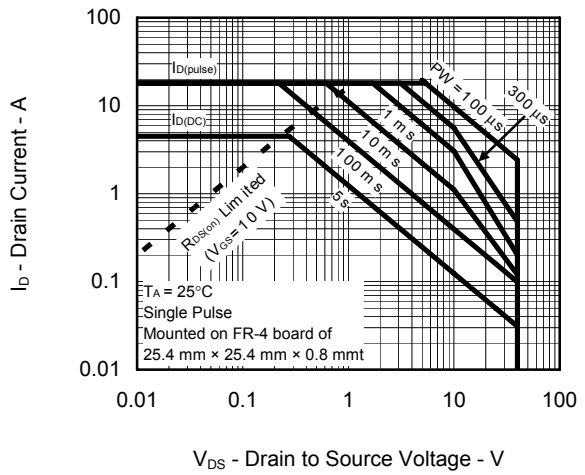
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



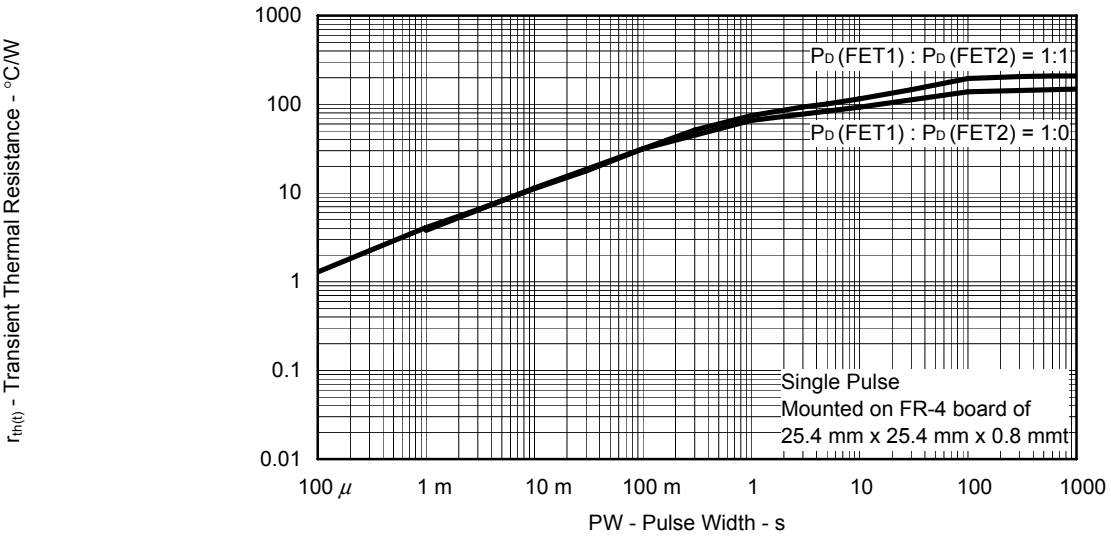
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



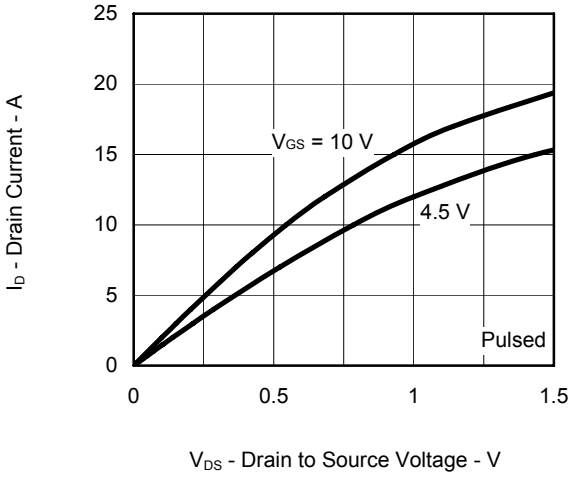
FORWARD BIAS SAFE OPERATING AREA



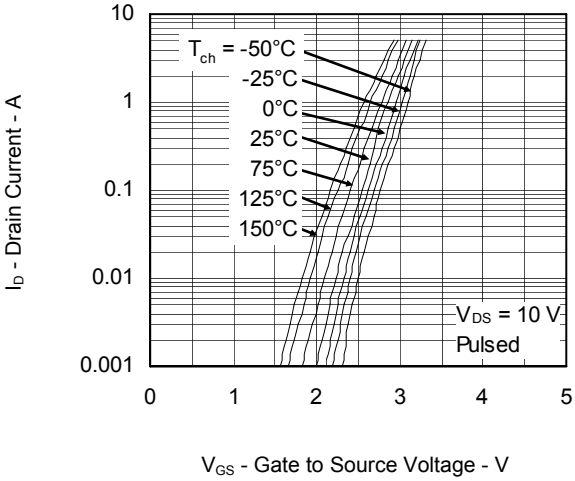
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



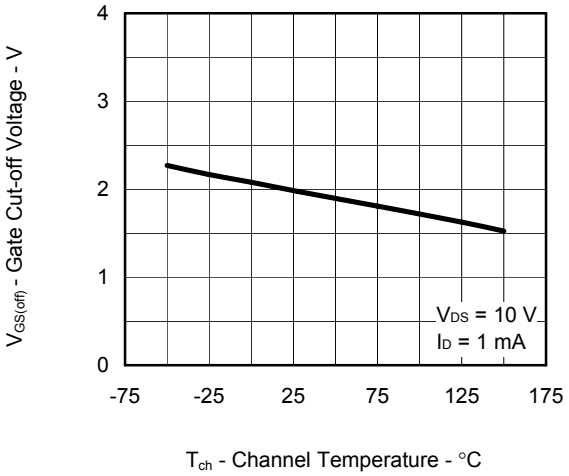
DRAIN CURRENT vs.
DRAIN TO SOURCE VOLTAGE



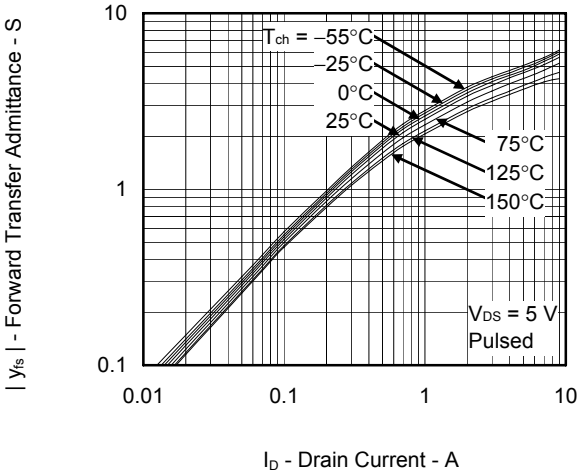
FORWARD TRANSFER CHARACTERISTICS



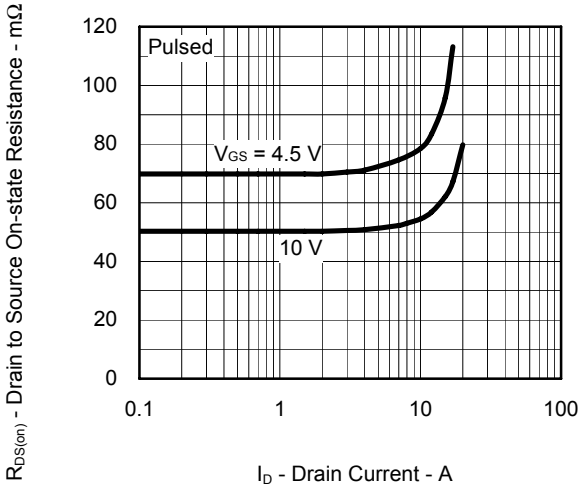
GATE CUT-OFF VOLTAGE vs.
CHANNEL TEMPERATURE



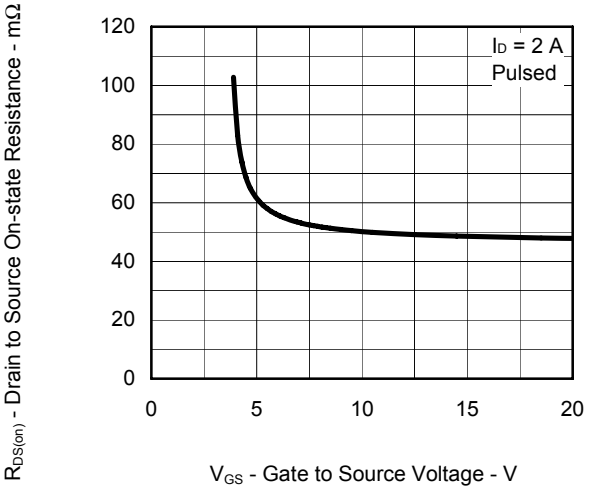
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



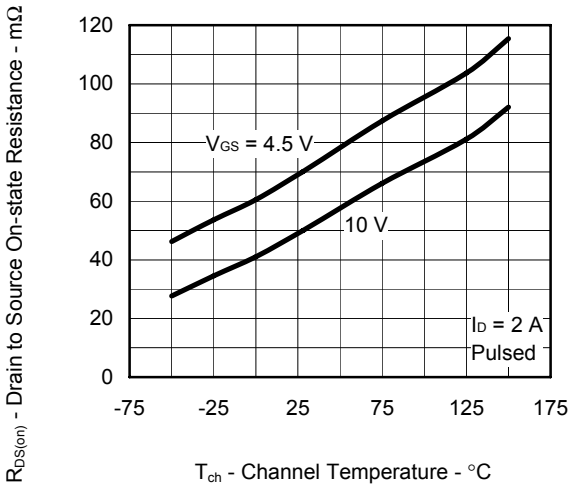
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
DRAIN CURRENT



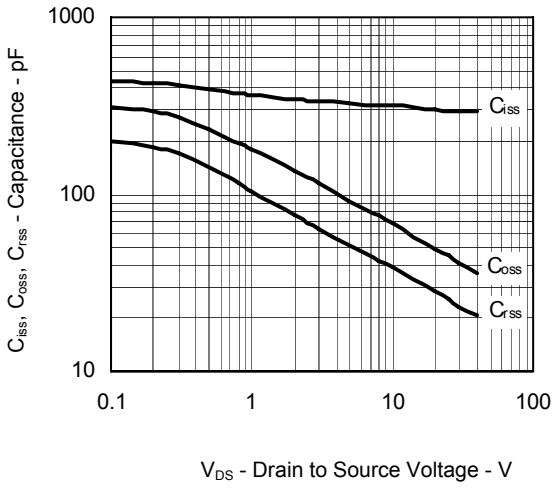
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
GATE TO SOURCE VOLTAGE



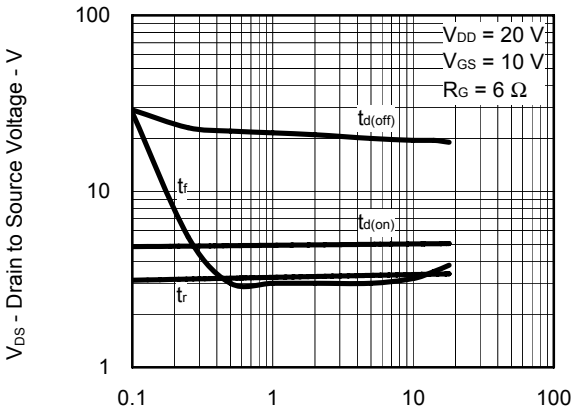
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



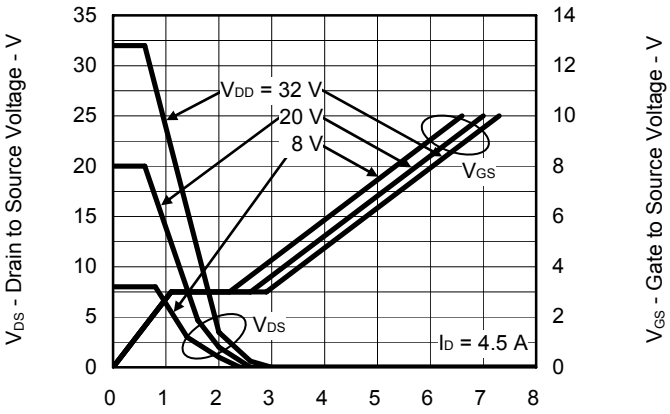
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



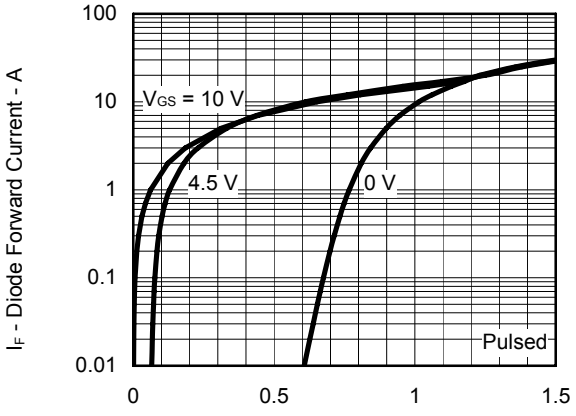
SWITCHING CHARACTERISTICS



DYNAMIC INPUT/OUTPUT CHARACTERISTICS

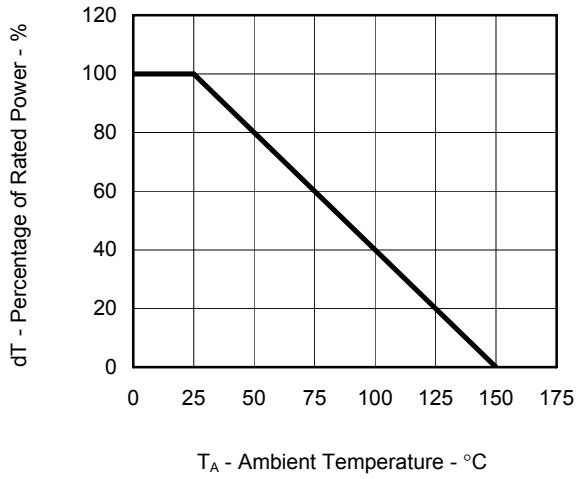


SOURCE TO DRAIN DIODE FORWARD VOLTAGE

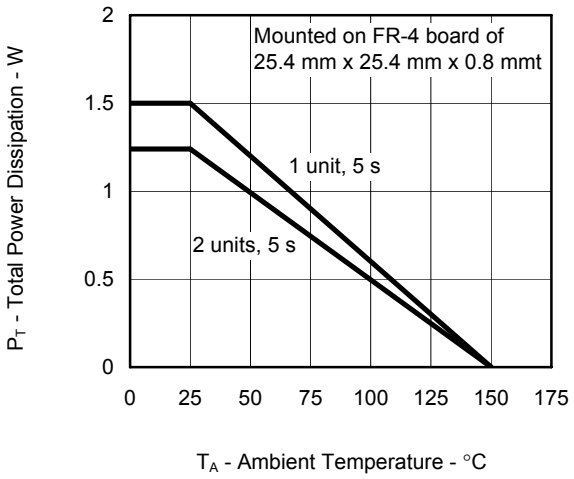


(2) P-channel MOSFET

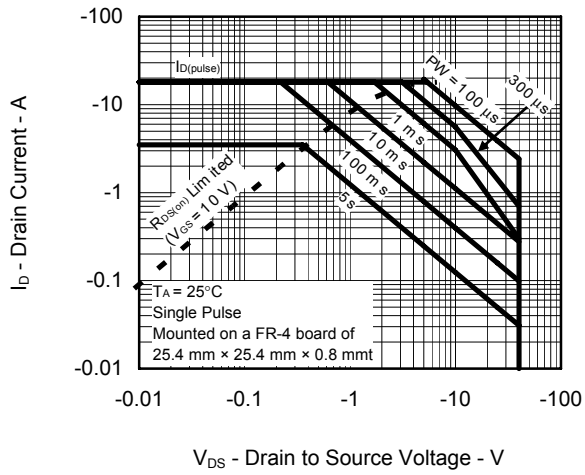
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



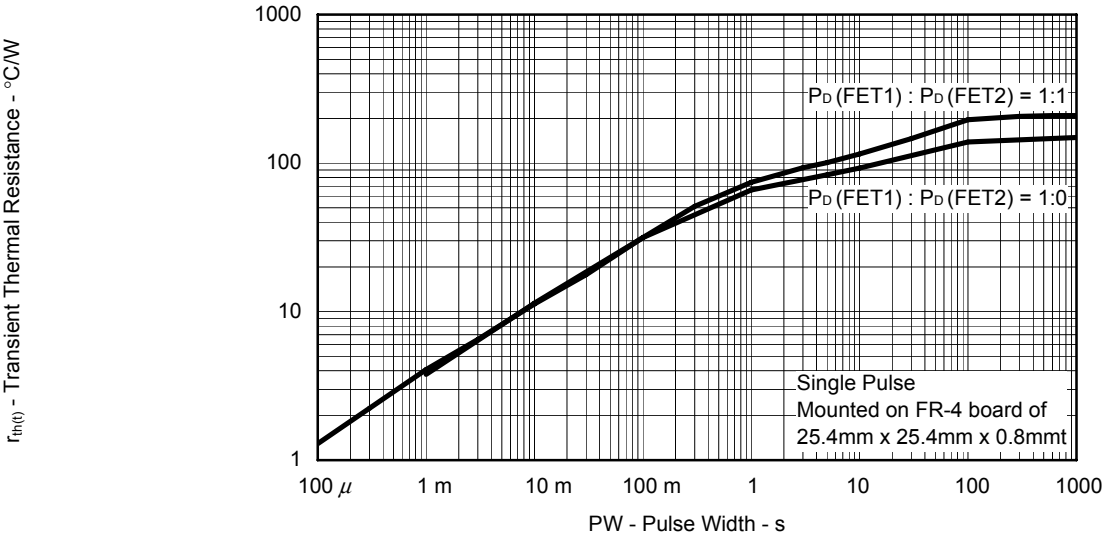
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



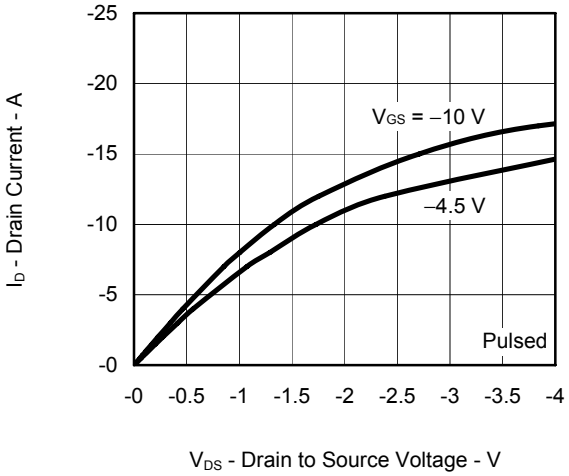
FORWARD BIAS SAFE OPERATING AREA



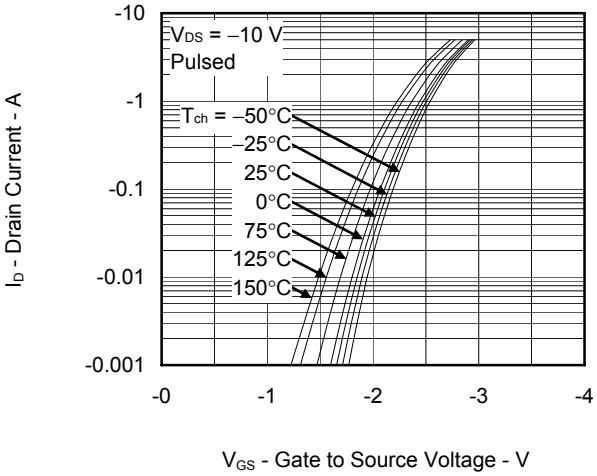
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



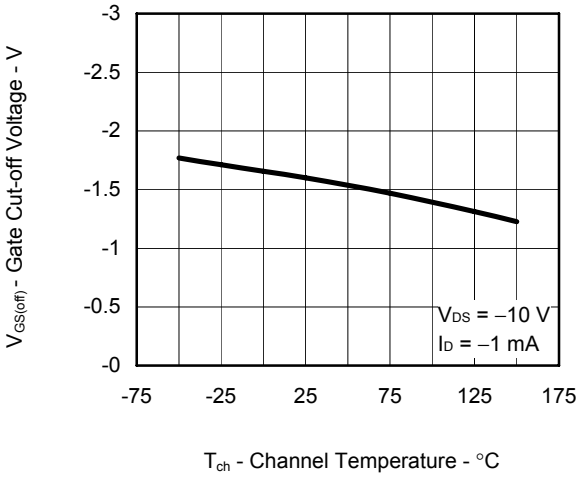
DRAIN CURRENT vs.
DRAIN TO SOURCE VOLTAGE



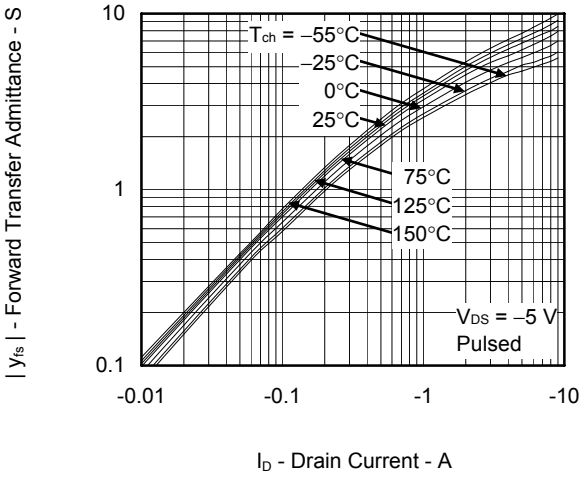
FORWARD TRANSFER CHARACTERISTICS



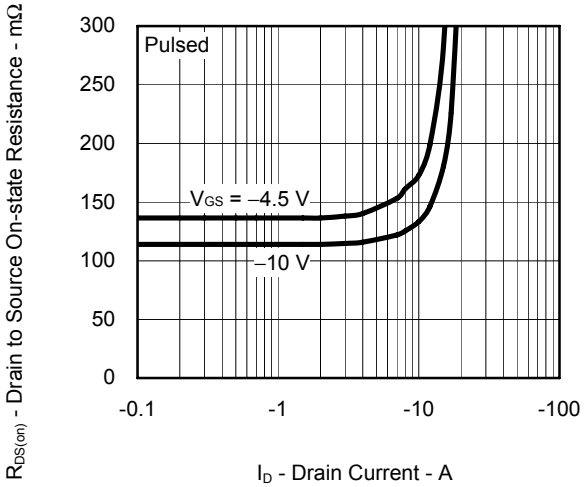
GATE CUT-OFF VOLTAGE vs.
CHANNEL TEMPERATURE



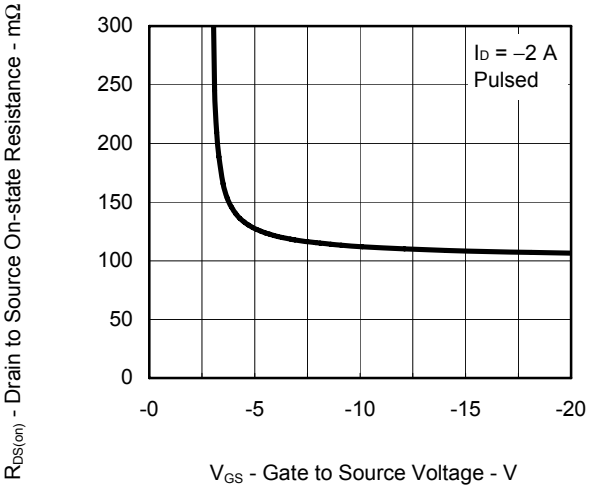
FORWARD TRANSFER ADMITTANCE vs.
DRAIN CURRENT



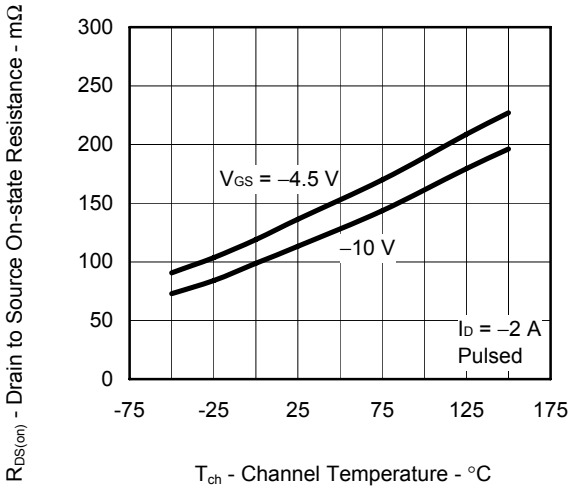
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
DRAIN CURRENT



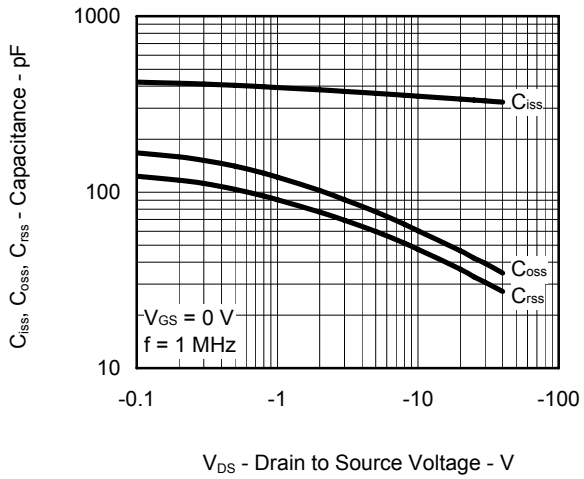
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
GATE TO SOURCE VOLTAGE



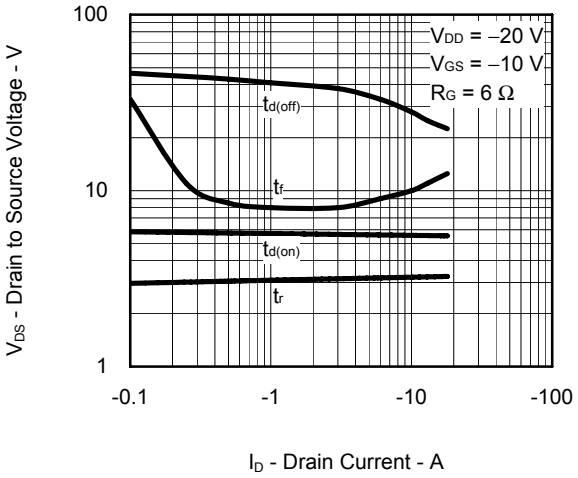
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



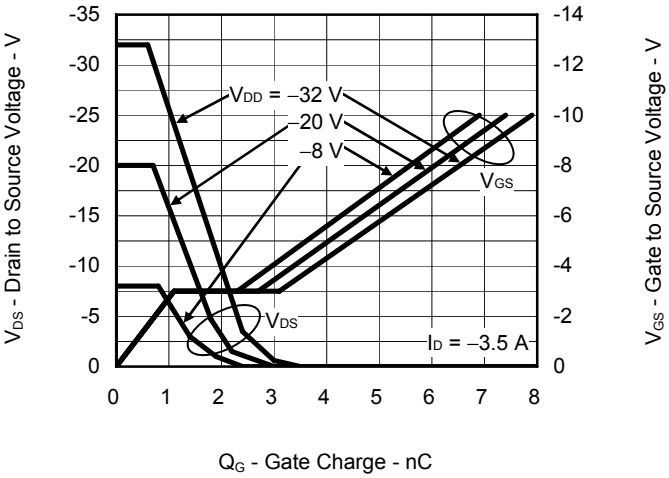
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



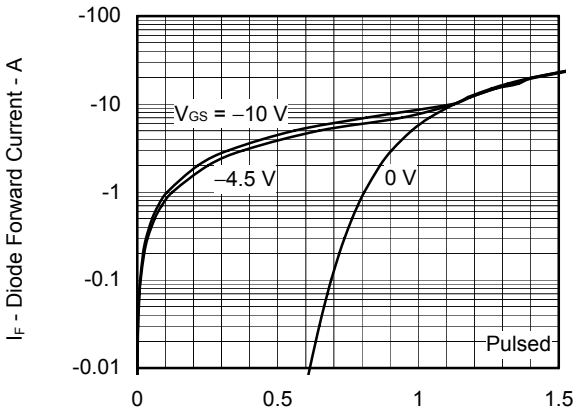
SWITCHING CHARACTERISTICS



DYNAMIC INPUT/OUTPUT CHARACTERISTICS

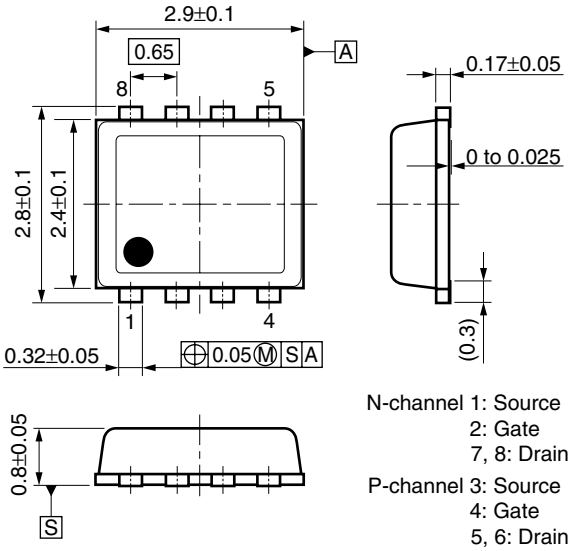


SOURCE TO DRAIN DIODE FORWARD VOLTAGE



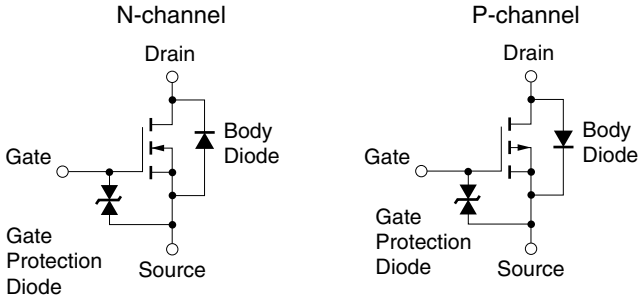
Package Drawings (Unit: mm)

8-pin VSOF (2429)



N-channel 1: Source
2: Gate
7, 8: Drain
P-channel 3: Source
4: Gate
5, 6: Drain

Equivalent Circuit



Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

Rev.	Date	Description	
		Page	Summary
1.00	Jul 01, 2010	–	First Eddition Issued
2.00	Sep 10,2010	5, 6	Change of graphs

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