# μPA2561T1H

## MOS FIELD EFFECT TRANSISTOR

R07DS0006EJ0100
Rev.1.00
Jul 08, 2010

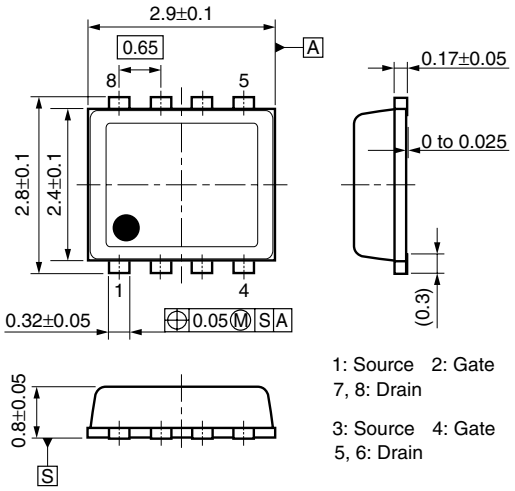
## Description

The μPA2561 is Dual N-channel MOSFETs designed for back light inverters and power management applications of portable equipments. Dual N-channel MOSFETs are assembled in one package, to contribute minimize the equipments.

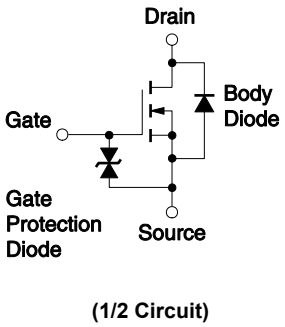
## Features

- 2.5 V drive available
- Low on-state resistance
  - $R_{DS(on)1}$ = 50 mΩ MAX. ($V_{GS}$ = 4.5 V, $I_D$ = 2 A)
  - $R_{DS(on)2}$ = 65 mΩ MAX. ($V_{GS}$ = 2.5 V, $I_D$ = 2 A)

## Package Drawing (Unit: mm)




## Equivalent Circuit




## Ordering Information

| Part No. | Lead Plating | Packing | Package |
|---|---|---|---|
| μPA2561T1H-T1-AT[Note] | Pure Sn | 8 mm Embossed Taping<br>3000 p/reel | 8-pin VSOF (2429) |
| μPA2561T1H-T2-AT[Note] | | | |

Note: This product does not contain Pb in external electrode and other parts.
Marking: 2561

## Absolute Maximum Ratings ($T_A$ = 25°C)

| Item | Symbol | Ratings | Unit |
|---|---|---|---|
| Drain to Source Voltage ($V_{GS}$ = 0 V) | $V_{DSS}$ | 20 | V |
| Gate to Source Voltage ($V_{DS}$ = 0 V) | $V_{GSS}$ | ±12 | V |
| Drain Current (DC) | $I_{D(DC)}$ | ±4.5 | A |
| Drain Current (pulse) [Note1] | $I_{D(pulse)}$ | ±18 | A |
| Total Power Dissipation (1 unit, 5s)[Note2] | $P_{T1}$ | 1.5 | W |
| Total Power Dissipation (2 unit, 5s) [Note2] | $P_{T2}$ | 2.2 | W |
| Channel Temperature | $T_{ch}$ | 150 | °C |
| Storage Temperature | $T_{stg}$ | -55 to + 150 | °C |

Notes 1. PW ≤ 10 μs, Duty Cycle ≤ 1%
2. Mounted on FR-4 board of 25.4 mm x 25.4 mm x 0.8 mmt

Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

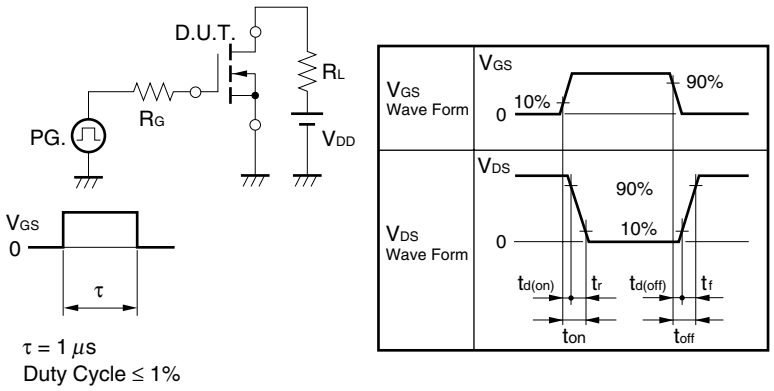
**Caution** This product is electrostatic-sensitive device due to low ESD capability and should be handled with caution for electrostatic discharge.

## Electrical Characteristics ($T_A$ = 25°C)

| Item | Symbol | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| Zero Gate Voltage Drain Current | $I_{DSS}$ | | | 1 | μA | $V_{DS}$ = 20 V, $V_{GS}$ = 0 V |
| Gate Leakage Current | $I_{GSS}$ | | | ±10 | μA | $V_{GS}$ = ±12 V, $V_{DS}$ = 0 V |
| Gate to Source Cut-off Voltage | $V_{GS(off)}$ | 0.5 | | 1.5 | V | $V_{DS}$ = 10 V, $I_D$ = 1 mA |
| Forward Transfer Admittance Note | $\|y_{fs}\|$ | 2.0 | | | S | $V_{DS}$ = 10 V, $I_D$ = 2 A |
| Drain to Source On-state Resistance Note | $R_{DS(on)1}$ | | 29 | 50 | mΩ | $V_{GS}$ = 4.5 V, $I_D$ = 2 A |
| | $R_{DS(on)2}$ | | 41 | 65 | mΩ | $V_{GS}$ = 2.5 V, $I_D$ = 2 A |
| Input Capacitance | $C_{iss}$ | | 455 | | pF | $V_{DS}$ = 10 V<br>$V_{GS}$ = 0 V<br>f = 1.0 MHz |
| Output Capacitance | $C_{oss}$ | | 75 | | pF | |
| Reverse Transfer Capacitance | $C_{rss}$ | | 47 | | pF | |
| Turn-on Delay Time | $t_{d(on)}$ | | 8.0 | | ns | $V_{DD}$ = 10 V, $I_D$ = 2 A,<br>$V_{GS}$ = 4.5 V,<br>$R_G$ = 6 Ω |
| Rise Time | $t_r$ | | 8.0 | | ns | |
| Turn-off Delay Time | $t_{d(off)}$ | | 20 | | ns | |
| Fall Time | $t_f$ | | 6.0 | | ns | |
| Total Gate Charge | $Q_G$ | | 5.4 | | nC | $V_{DD}$ = 16 V,<br>$V_{GS}$ = 4.5 V,<br>$I_D$ = 4 A |
| Gate to Source Charge | $Q_{GS}$ | | 0.9 | | nC | |
| Gate to Drain Charge | $Q_{GD}$ | | 1.6 | | nC | |
| Diode Forward Voltage Note | $V_{F(S-D)}$ | | 0.85 | | V | $I_F$ = 4 A, $V_{GS}$ = 0 V |

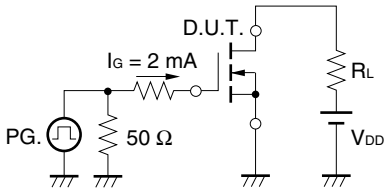
Note: Pulsed

**TEST CIRCUIT 1 SWITCHING TIME**



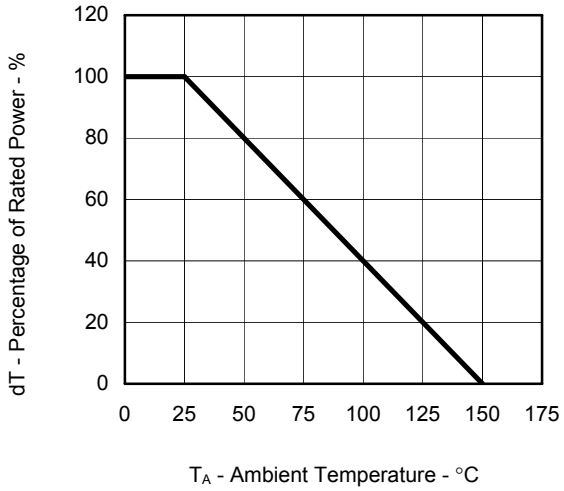

τ = 1 μs
Duty Cycle ≤ 1%

**TEST CIRCUIT 2 GATE CHARGE**

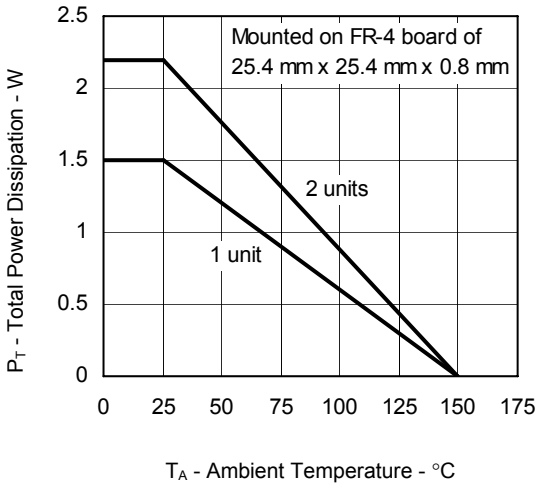


## Typical Characteristics ($T_A$ = 25°C)

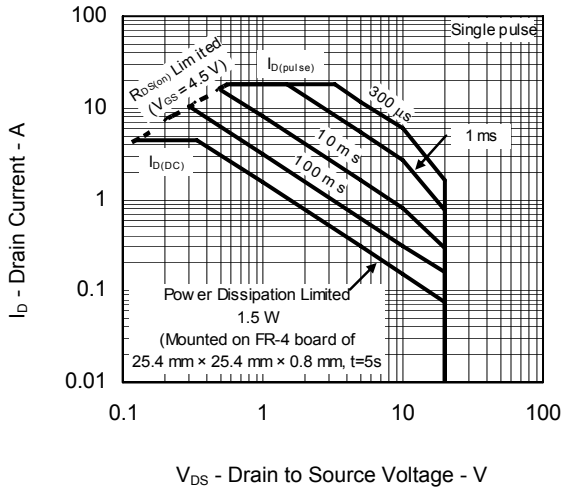
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



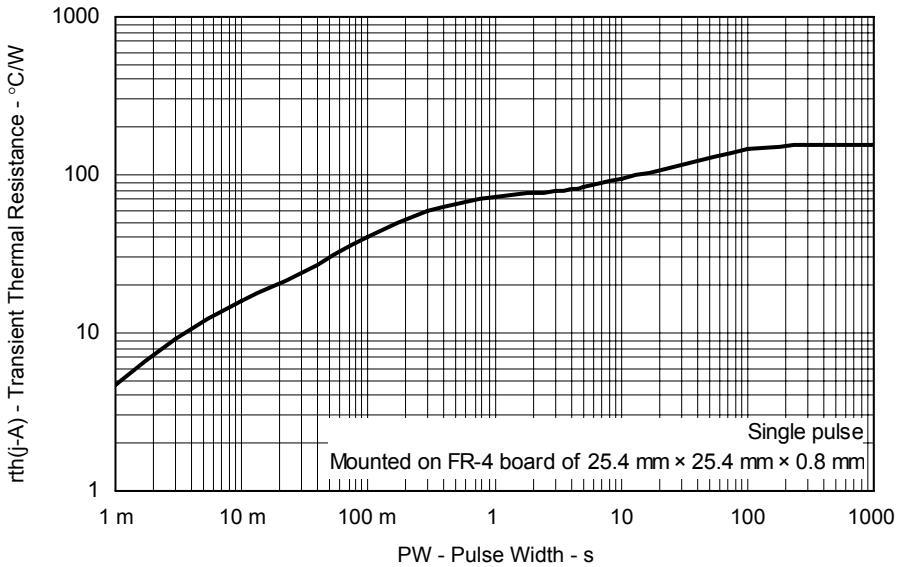

TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



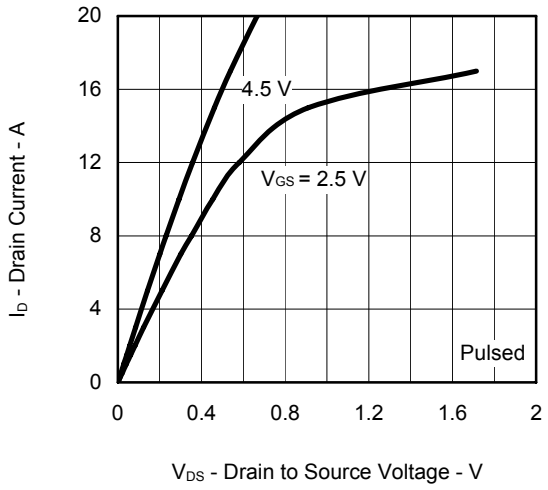

FORWARD BIAS SAFE OPERATING AREA



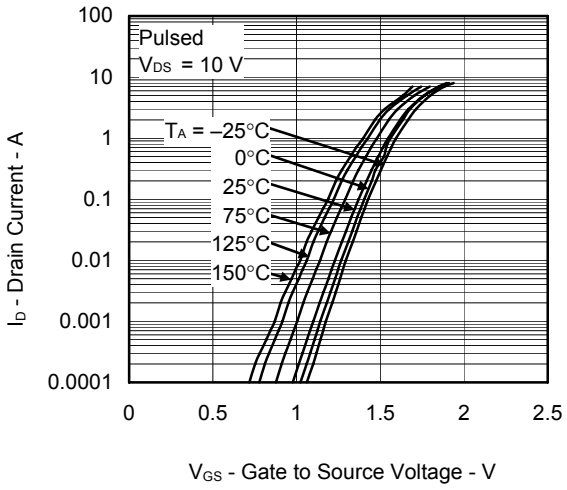

TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



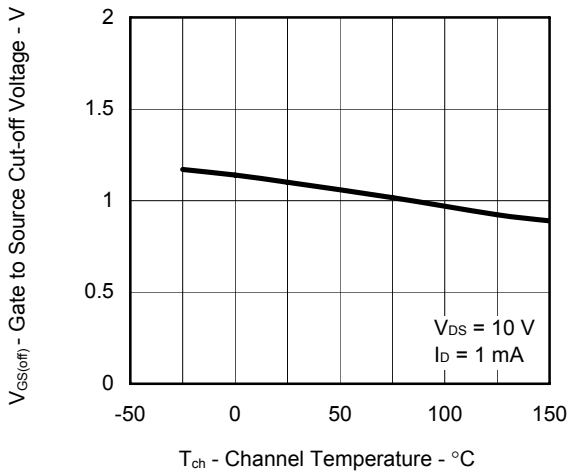
DRAIN CURRENT vs.
DRAIN TO SOURCE VOLTAGE



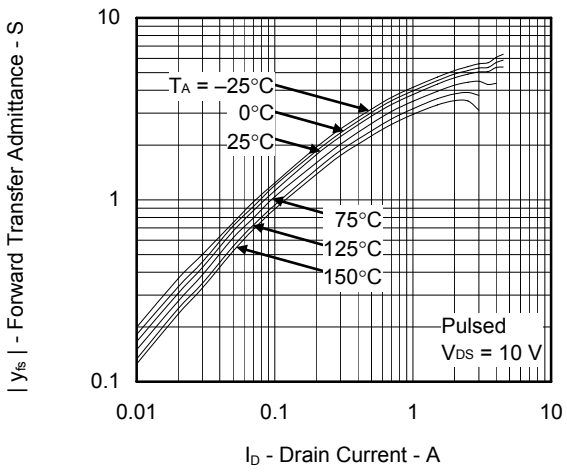

FORWARD TRANSFER CHARACTERISTICS



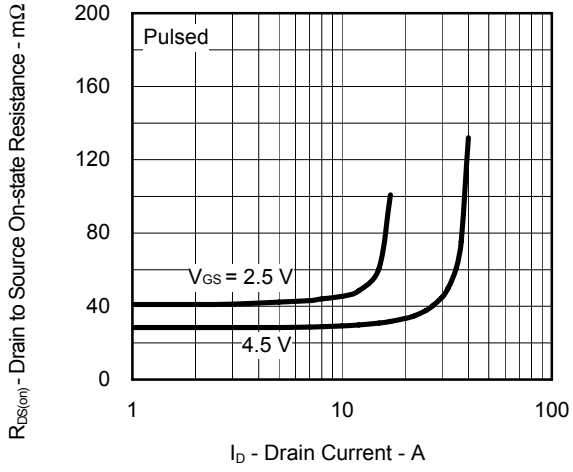

GATE TO SOURCE CUT-OFF VOLTAGE vs.
CHANNEL TEMPERATURE



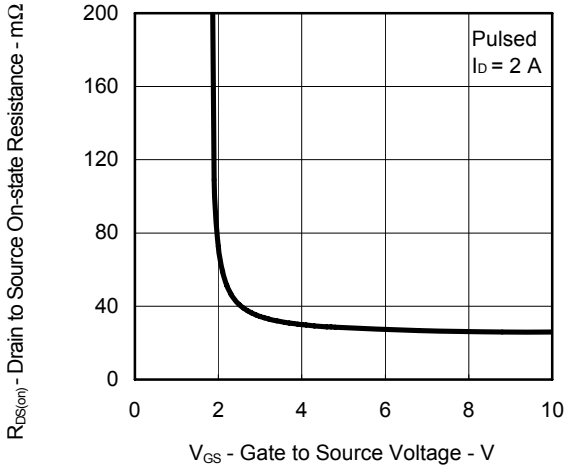

FORWARD TRANSFER ADMITTANCE vs.
DRAIN CURRENT



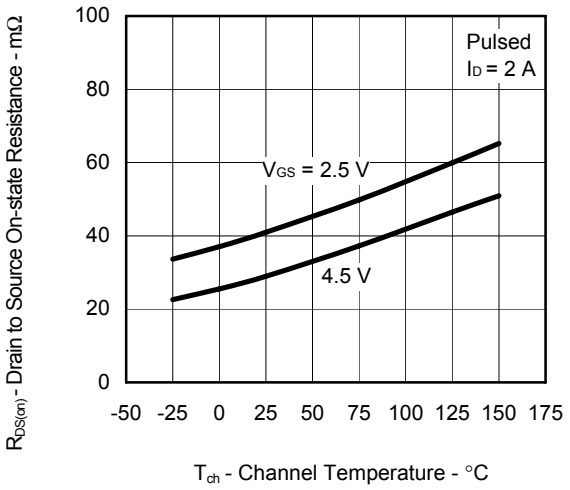

DRAIN TO SOURCE ON-STATE RESISTANCE vs.
DRAIN CURRENT



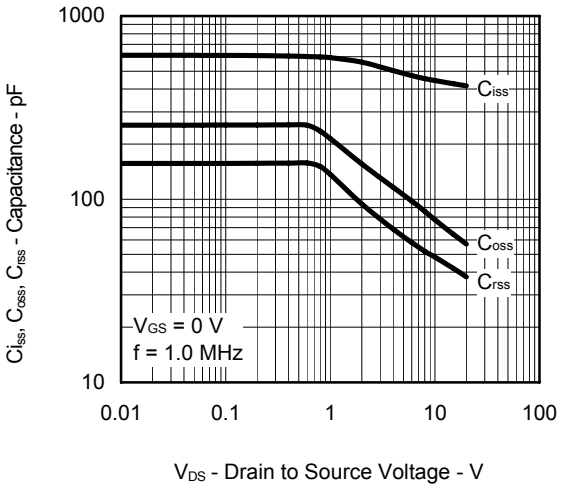

DRAIN TO SOURCE ON-STATE RESISTANCE vs.
GATE TO SOURCE VOLTAGE



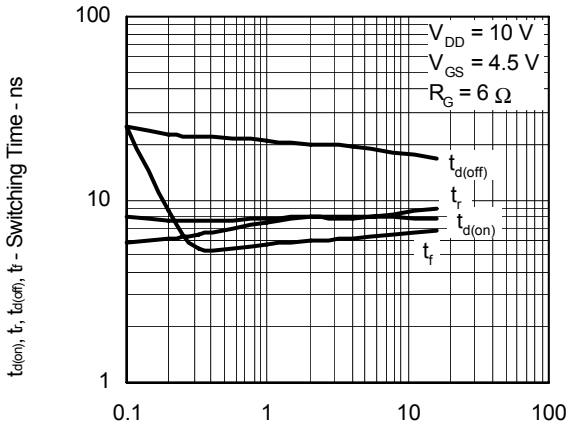
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



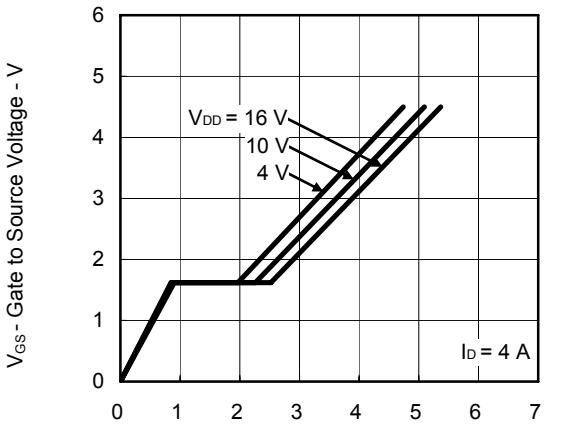

CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



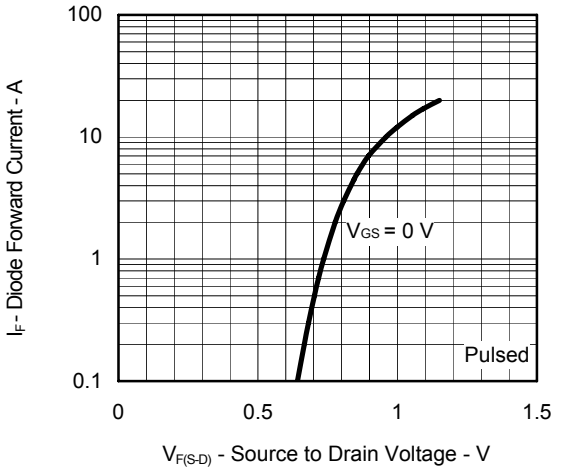

SWITCHING CHARACTERISTICS




DYNAMIC INPUT CHARACTERISTICS




SOURCE TO DRAIN DIODE FORWARD VOLTAGE



| Revision History | μPA2561T1H |
|---|---|

| Rev. | Date | Description | |
|---|---|---|---|
| | | Page | Summary |
| 1.00 | Jul 08, 2010 | - | First Edition issued |
| | | | |

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