

To our customers,

Old Company Name in Catalogs and Other Documents

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Renesas Electronics website: <http://www.renesas.com>

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (<http://www.renesas.com>)

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(Note 2) “Renesas Electronics product(s)” means any product developed or manufactured by or for Renesas Electronics.

MOS FIELD EFFECT TRANSISTOR

μ PA2791GR

SWITCHING

N- AND P-CHANNEL POWER MOS FET

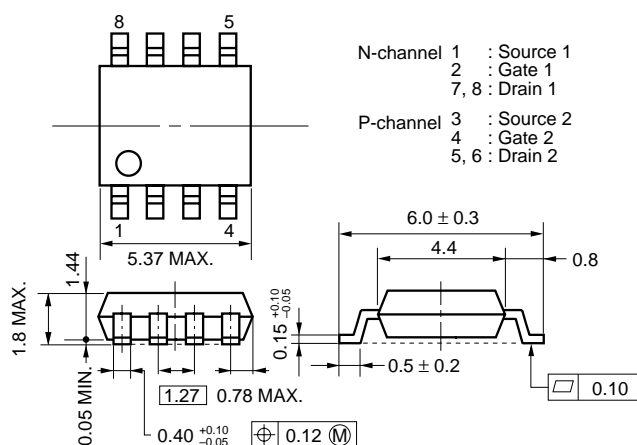
DESCRIPTION

The μ PA2791GR is N- and P-channel MOS Field Effect Transistors designed for switching application.

FEATURES

- Low on-state resistance
 - N-channel $R_{DS(on)1} = 36.0 \text{ m}\Omega \text{ MAX.}$ ($V_{GS} = 10 \text{ V}$, $I_D = 3.0 \text{ A}$)
 - $R_{DS(on)2} = 50.0 \text{ m}\Omega \text{ MAX.}$ ($V_{GS} = 4.5 \text{ V}$, $I_D = 3.0 \text{ A}$)
 - P-channel $R_{DS(on)1} = 82 \text{ m}\Omega \text{ MAX.}$ ($V_{GS} = -10 \text{ V}$, $I_D = -3.0 \text{ A}$)
 - $R_{DS(on)2} = 110 \text{ m}\Omega \text{ MAX.}$ ($V_{GS} = -4.5 \text{ V}$, $I_D = -3.0 \text{ A}$)
- Low gate charge
 - N-channel $Q_G = 10 \text{ nC TYP.}$ ($V_{GS} = 10 \text{ V}$)
 - P-channel $Q_G = 8.3 \text{ nC TYP.}$ ($V_{GS} = -10 \text{ V}$)
- Built-in gate protection diode
- Small and surface mount package (Power SOP8)

PACKAGE DRAWING (Unit: mm)

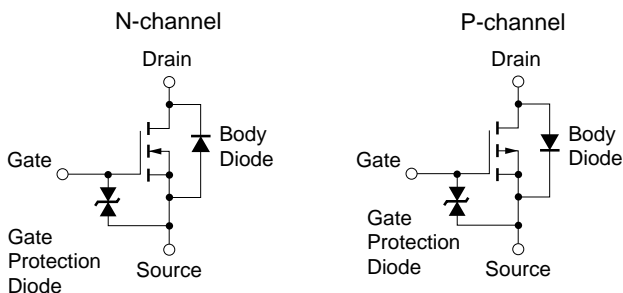


ORDERING INFORMATION

PART NUMBER	LEAD PLATING	PACKING	PACKAGE
μ PA2791GR-E1-AT <small>Note</small>	Pure Sn	Tape 2500 p/reel	Power SOP8
μ PA2791GR-E2-AT <small>Note</small>			

Note Pb-free (This product does not contain Pb in the external electrode and other parts.)

EQUIVALENT CIRCUIT



Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

Caution This product is electrostatic-sensitive device due to low ESD capability and should be handled with caution for electrostatic discharge. $V_{ESD} \pm 600 \text{ V TYP.}$ ($C = 100 \text{ pF}$, $R = 1.5 \text{ k}\Omega$)

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ABSOLUTE MAXIMUM RATINGS (T_A = 25°C. All terminals are connected.)

PARAMETER	SYMBOL	N-CHANNEL	P-CHANNEL	UNIT
Drain to Source Voltage (V _{GS} = 0 V)	V _{DSS}	30	-30	V
Gate to Source Voltage (V _{DS} = 0 V)	V _{GSS}	±20	∓20	V
Drain Current (DC) (T _C = 25°C) ^{Note2}	I _{D(DC)}	±5	∓5	A
Drain Current (pulse) ^{Note1}	I _{D(pulse)}	±20	∓20	A
Total Power Dissipation (1 unit) ^{Note2}	P _{T1}	1.7		W
Total Power Dissipation (2 units) ^{Note2}	P _{T2}	2.0		W
Channel Temperature	T _{ch}	150		°C
Storage Temperature	T _{stg}	-55 to +150		°C
<R> Single Avalanche Current ^{Note3}	I _{AS}	5	-5	A
<R> Single Avalanche Energy ^{Note3}	E _{AS}	2.5		mJ

Notes 1. PW ≤ 10 μs, Duty Cycle ≤ 1%

2. Mounted on ceramic substrate of 2000 mm² x 1.6 mm

<R> **3.** Starting T_{ch} = 25°C, V_{DD} = 1/2 x V_{DSS}, R_G = 25 Ω, L = 100 μH, V_{GS} = V_{GSS} → 0 V

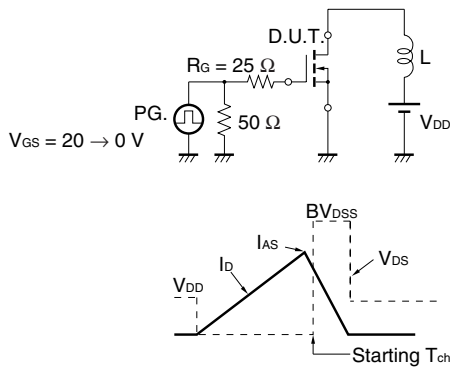
ELECTRICAL CHARACTERISTICS (TA = 25°C. All terminals are connected.)

N-channel

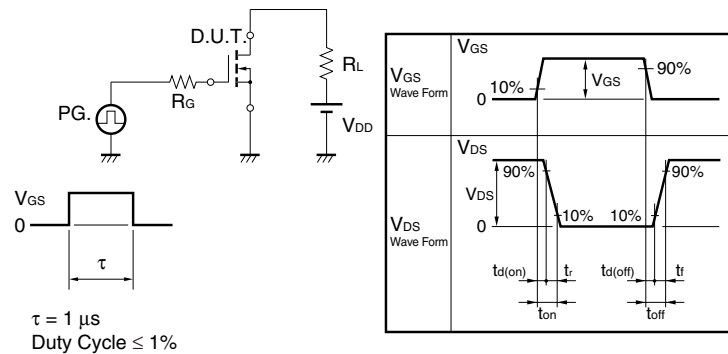
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 30 V, V _{GS} = 0 V			10	μA
Gate Leakage Current	I _{GSS}	V _{GS} = ±16 V, V _{DS} = 0 V			±10	μA
Gate to Source Cut-off Voltage	V _{GS(off)}	V _{DS} = 10 V, I _D = 1 mA	1.0		2.5	V
Forward Transfer Admittance ^{Note}	y _{fs}	V _{DS} = 10 V, I _D = 3 A	2.0			S
Drain to Source On-state Resistance ^{Note}	R _{DS(on)1}	V _{GS} = 10 V, I _D = 3.0 A		28.5	36.0	mΩ
	R _{DS(on)2}	V _{GS} = 4.5 V, I _D = 3.0 A		36.0	50.0	mΩ
Input Capacitance	C _{iss}	V _{DS} = 10 V,		400		pF
Output Capacitance	C _{oss}	V _{GS} = 0 V,		80		pF
Reverse Transfer Capacitance	C _{rss}	f = 1 MHz		50		pF
Turn-on Delay Time	t _{d(on)}	V _{DD} = 15 V, I _D = 3 A,		7		ns
Rise Time	t _r	V _{GS} = 10 V,		4		ns
Turn-off Delay Time	t _{d(off)}	R _G = 10 Ω		21		ns
Fall Time	t _f			5		ns
Total Gate Charge	Q _G	I _D = 5 A,		10		nC
Gate to Source Charge	Q _{GS}	V _{DD} = 24 V,		1.5		nC
Gate to Drain Charge	Q _{GD}	V _{GS} = 10 V		2.7		nC
Body Diode Forward Voltage ^{Note}	V _{F(S-D)}	I _F = 5 A, V _{GS} = 0 V		0.86		V
Reverse Recovery Time	t _{rr}	I _F = 5 A, V _{GS} = 0 V,		20		ns
Reverse Recovery Charge	Q _{rr}	di/dt = 50 A/μs		16		nC

Note Pulsed

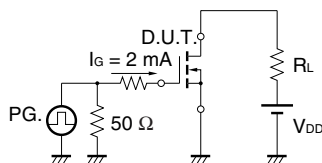
<R> **TEST CIRCUIT 1 AVALANCHE CAPABILITY**



TEST CIRCUIT 2 SWITCHING TIME



TEST CIRCUIT 3 GATE CHARGE

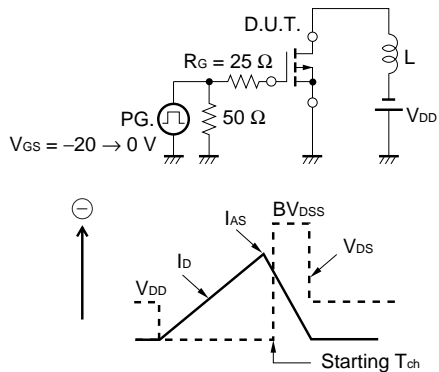


P-channel

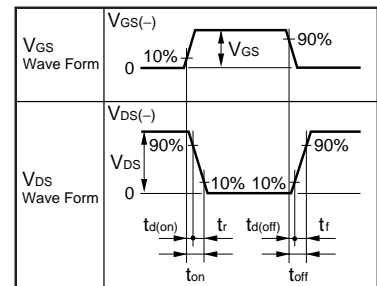
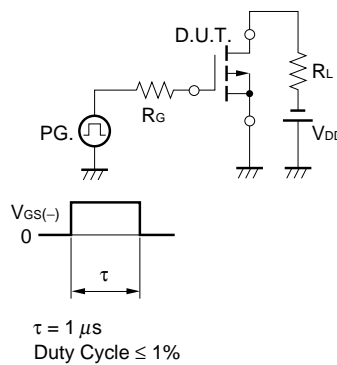
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -30\text{ V}, V_{GS} = 0\text{ V}$			-10	μA
Gate Leakage Current	I_{GSS}	$V_{GS} = \pm 16\text{ V}, V_{DS} = 0\text{ V}$			∓ 10	μA
Gate to Source Cut-off Voltage	$V_{GS(off)}$	$V_{DS} = -10\text{ V}, I_D = -1\text{ mA}$	-1.0		-2.5	V
Forward Transfer Admittance ^{Note}	$ y_{fs} $	$V_{DS} = -10\text{ V}, I_D = -3\text{ A}$	1.0			S
Drain to Source On-state Resistance ^{Note}	$R_{DS(on)1}$	$V_{GS} = -10\text{ V}, I_D = -3.0\text{ A}$		63	82	$\text{m}\Omega$
	$R_{DS(on)2}$	$V_{GS} = -4.5\text{ V}, I_D = -3.0\text{ A}$		79	110	$\text{m}\Omega$
Input Capacitance	C_{iss}	$V_{DS} = -10\text{ V},$		300		pF
Output Capacitance	C_{oss}	$V_{GS} = 0\text{ V},$		75		pF
Reverse Transfer Capacitance	C_{rss}	$f = 1\text{ MHz}$		60		pF
Turn-on Delay Time	$t_{d(on)}$	$V_{DD} = -15\text{ V}, I_D = -3\text{ A},$		8		ns
Rise Time	t_r	$V_{GS} = -10\text{ V},$		14		ns
Turn-off Delay Time	$t_{d(off)}$	$R_G = 10\ \Omega$		50		ns
Fall Time	t_f			40		ns
Total Gate Charge	Q_G	$I_D = -5\text{ A},$		8.3		nC
Gate to Source Charge	Q_{GS}	$V_{DD} = -24\text{ V},$		1.2		nC
Gate to Drain Charge	Q_{GD}	$V_{GS} = -10\text{ V}$		2.4		nC
Body Diode Forward Voltage ^{Note}	$V_{F(S-D)}$	$I_F = 5\text{ A}, V_{GS} = 0\text{ V}$		0.96		V
Reverse Recovery Time	t_{rr}	$I_F = 5\text{ A}, V_{GS} = 0\text{ V},$		37		ns
Reverse Recovery Charge	Q_{rr}	$di/dt = 50\text{ A}/\mu\text{s}$		29		nC

Note Pulsed

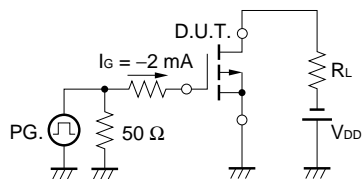
<R> **TEST CIRCUIT 1 AVALANCHE CAPABILITY**



TEST CIRCUIT 2 SWITCHING TIME

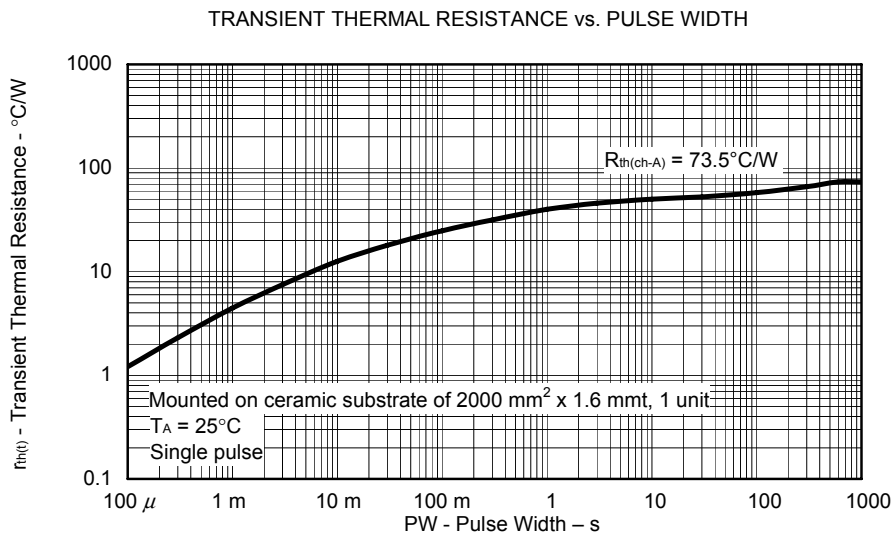
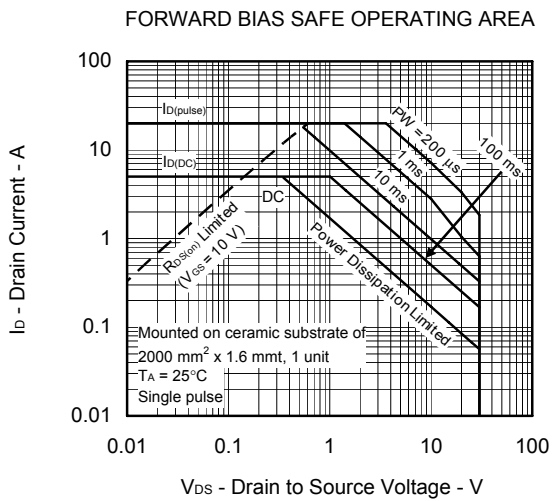
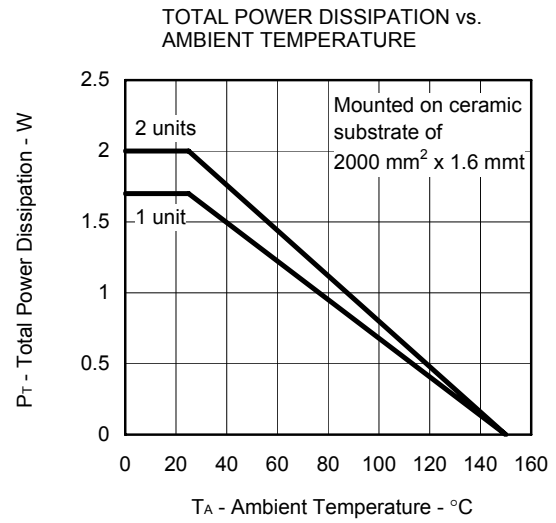
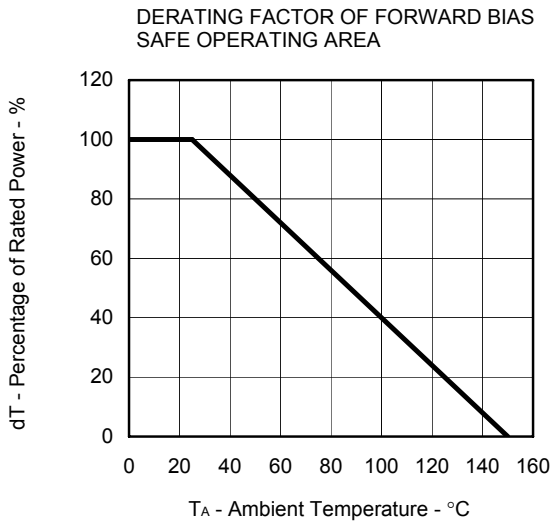


TEST CIRCUIT 3 GATE CHARGE

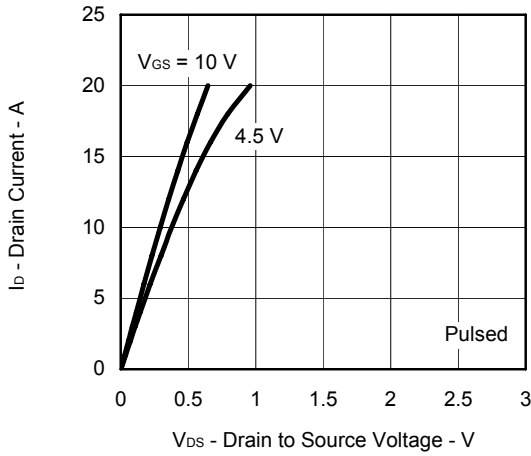


TYPICAL CHARACTERISTICS (T_A = 25°C)

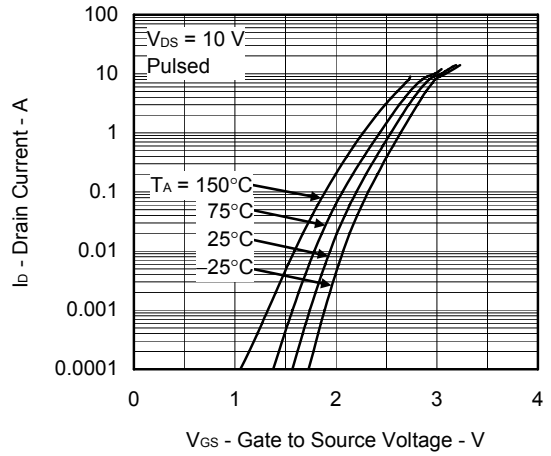
(1) N-channel



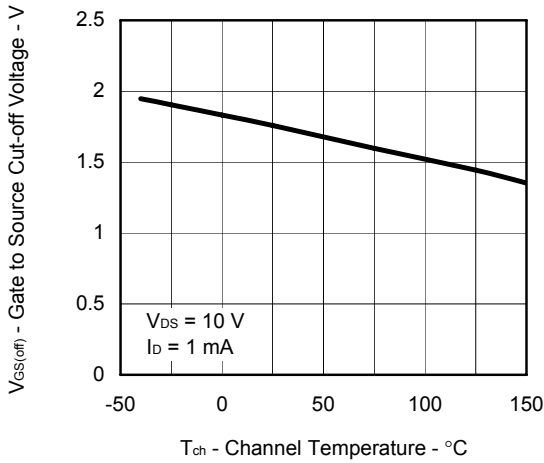
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



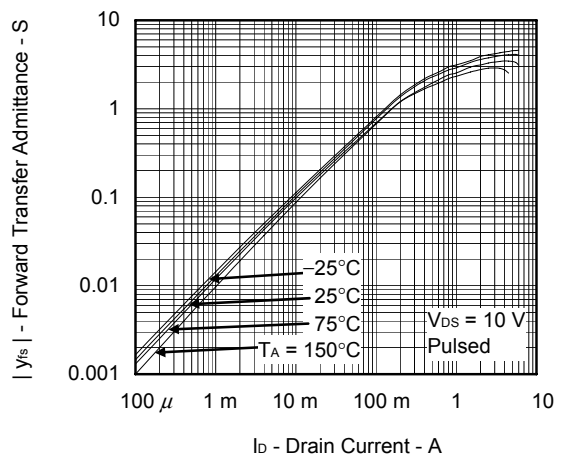
FORWARD TRANSFER CHARACTERISTICS



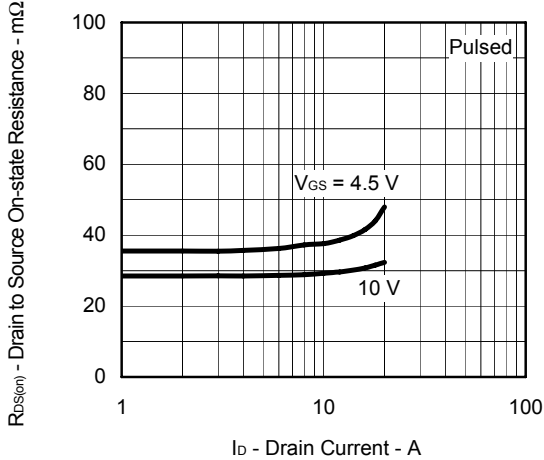
GATE TO SOURCE CUT-OFF VOLTAGE vs. CHANNEL TEMPERATURE



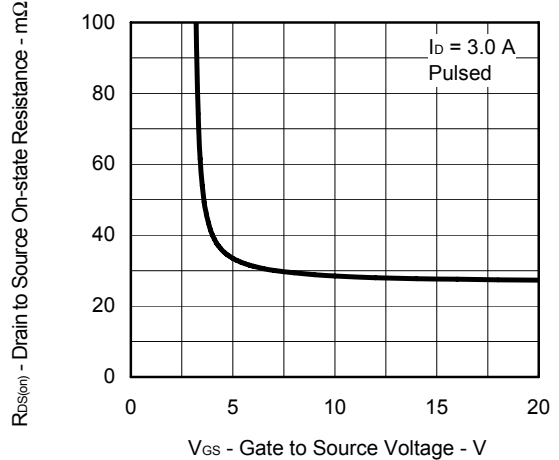
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



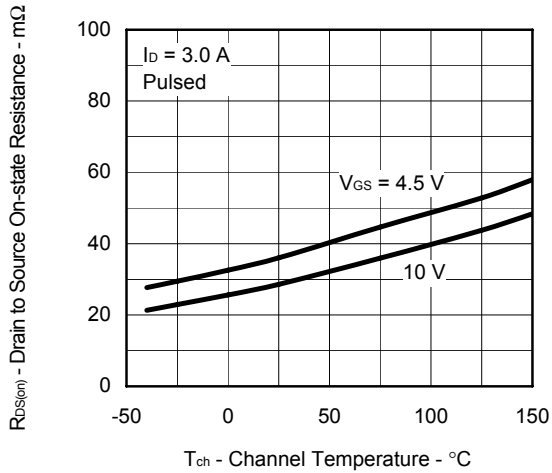
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



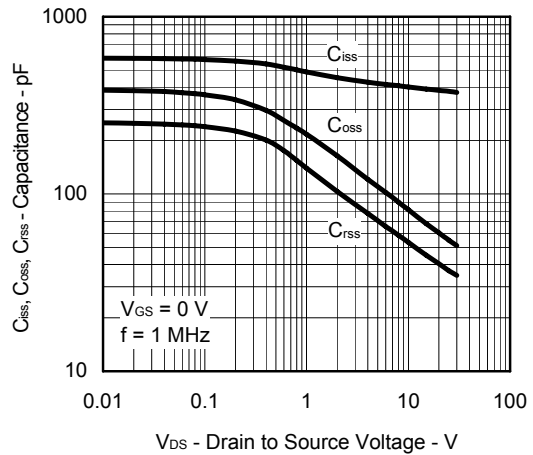
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



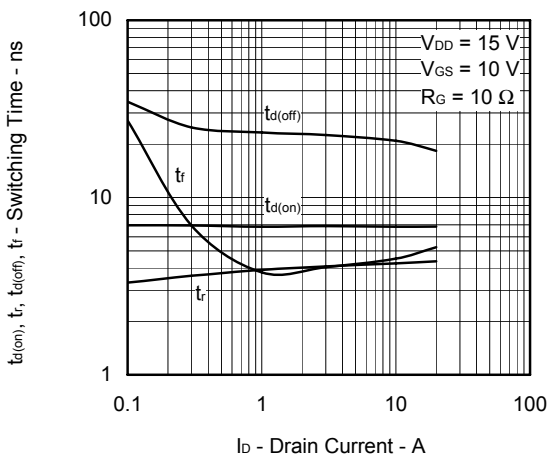
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



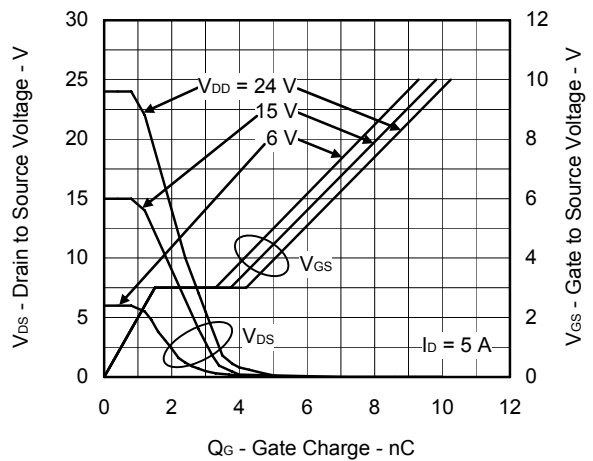
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



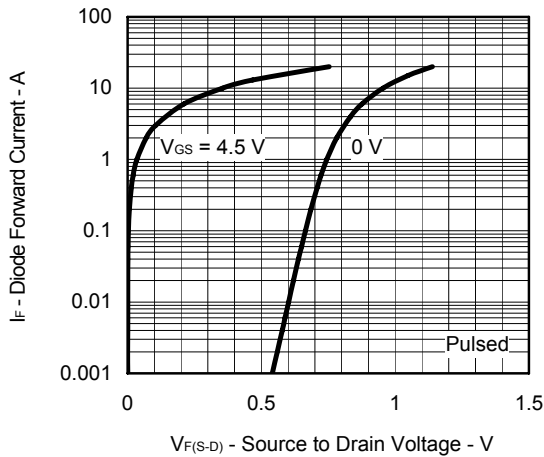
SWITCHING CHARACTERISTICS



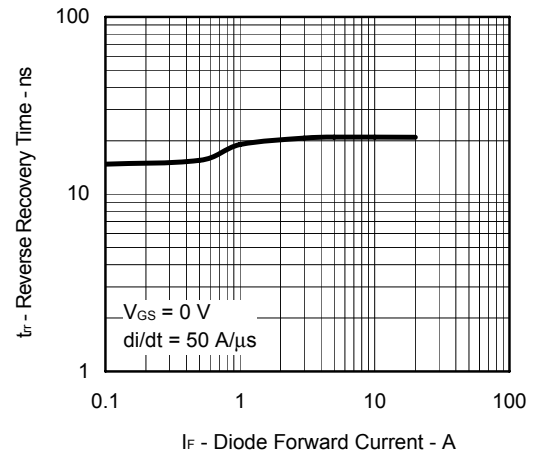
DYNAMIC INPUT/OUTPUT CHARACTERISTICS



SOURCE TO DRAIN DIODE FORWARD VOLTAGE

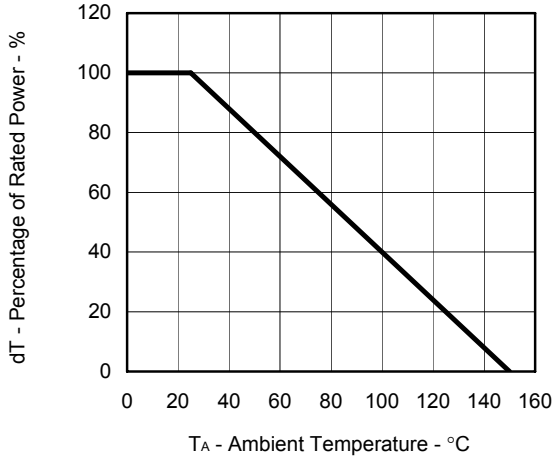


REVERSE RECOVERY TIME vs. DIODE FORWARD CURRENT

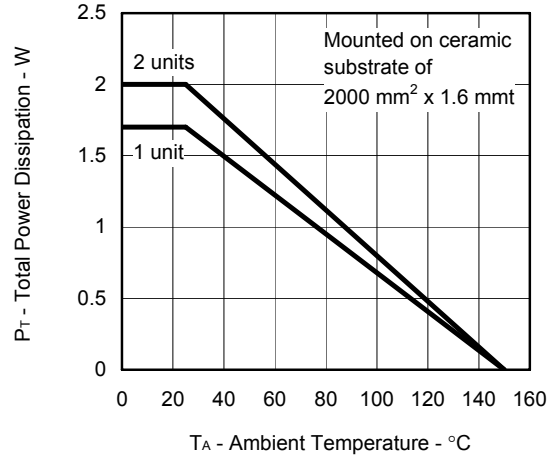


(2) P-channel

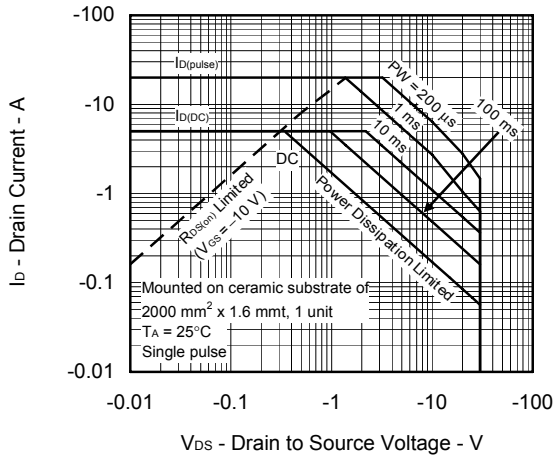
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



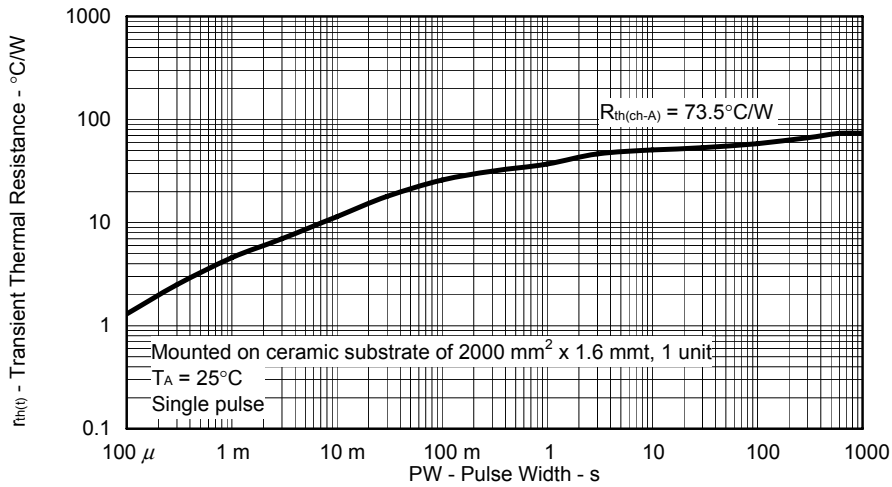
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



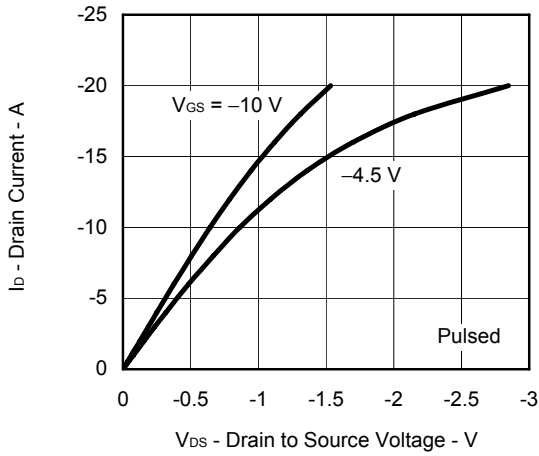
FORWARD BIAS SAFE OPERATING AREA



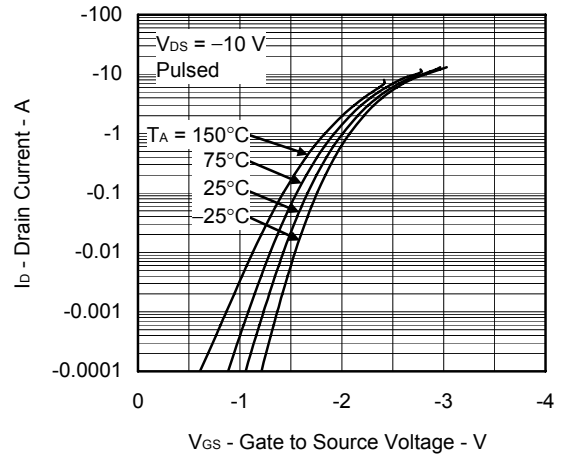
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



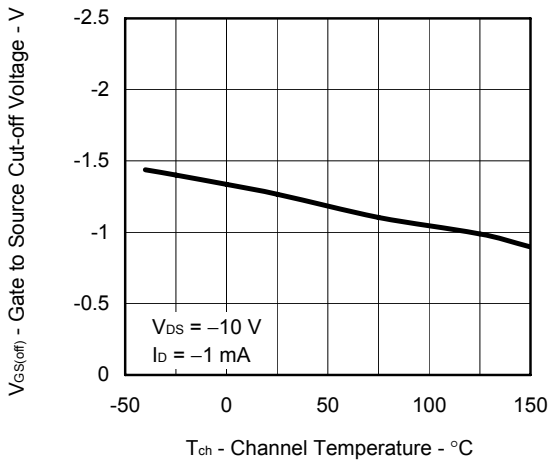
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



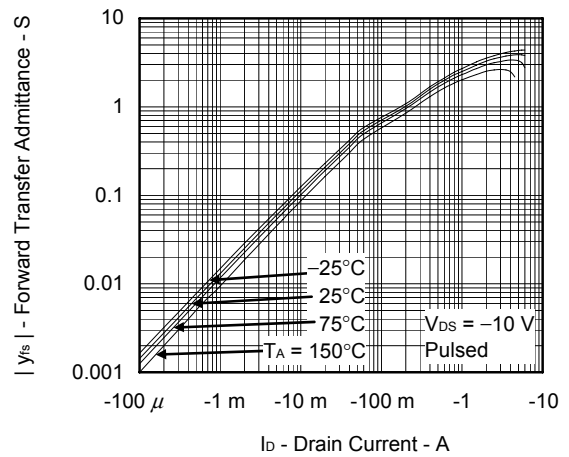
FORWARD TRANSFER CHARACTERISTICS



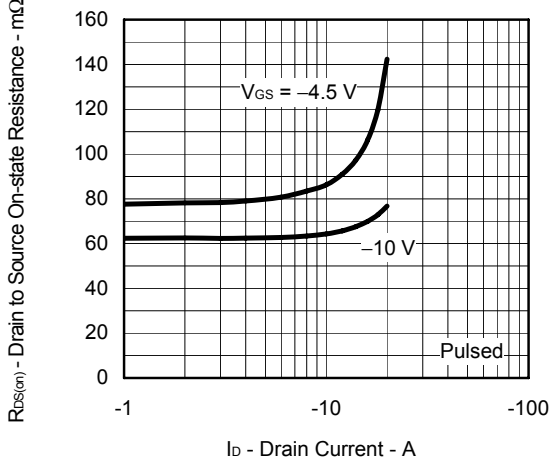
GATE TO SOURCE CUT-OFF VOLTAGE vs. CHANNEL TEMPERATURE



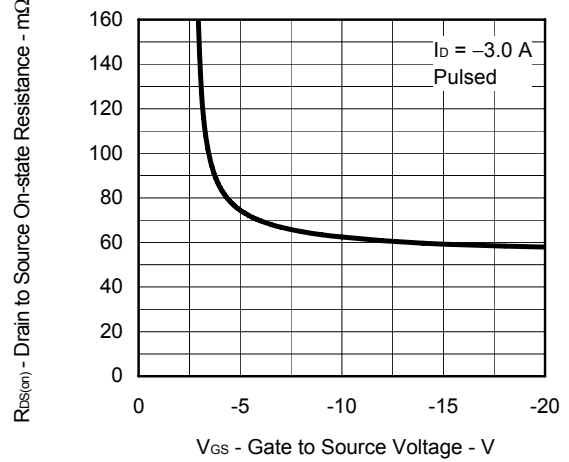
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



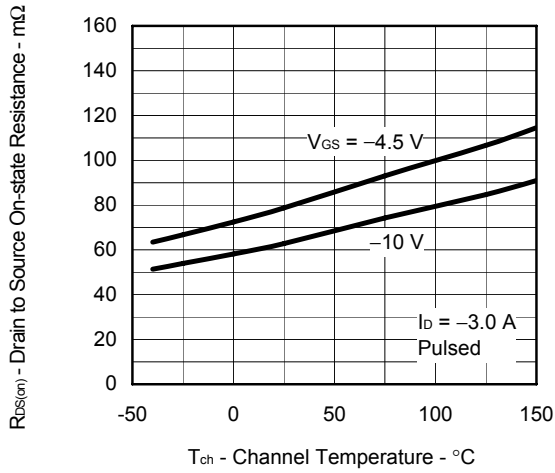
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



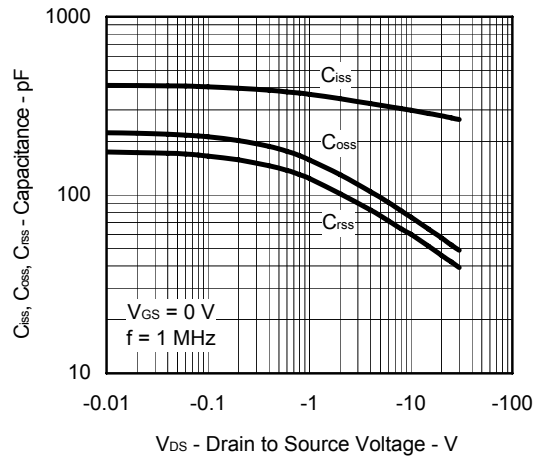
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



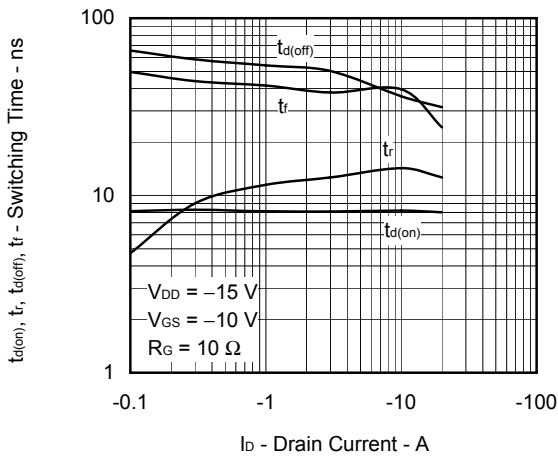
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



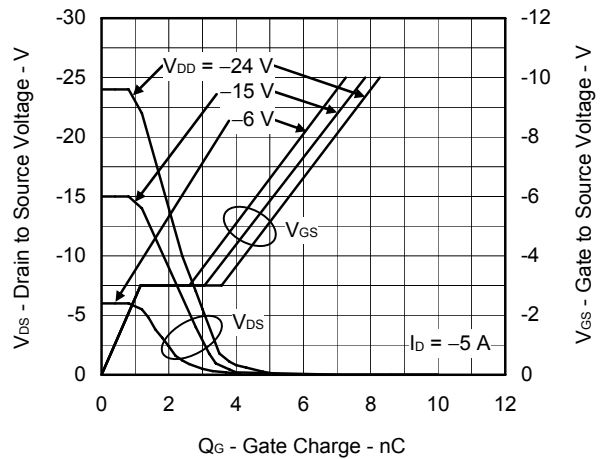
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



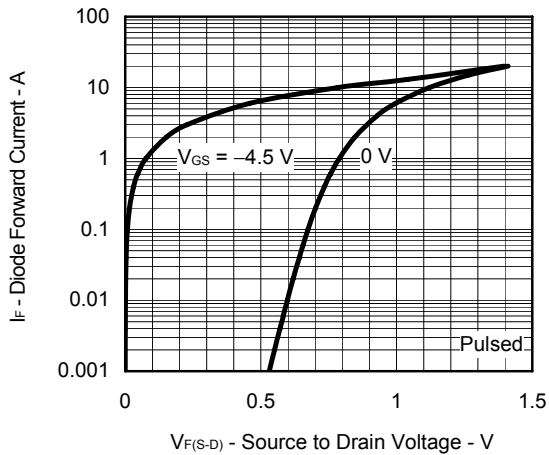
SWITCHING CHARACTERISTICS



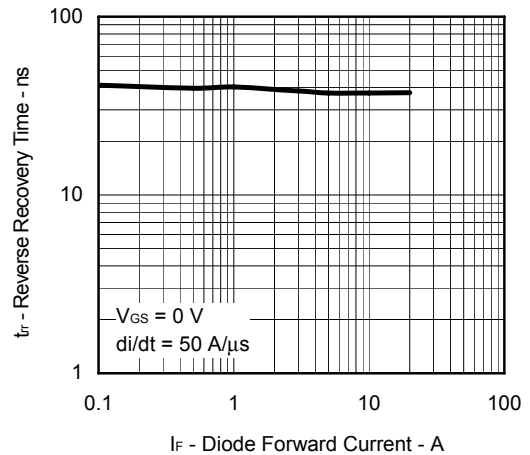
DYNAMIC INPUT/OUTPUT CHARACTERISTICS



SOURCE TO DRAIN DIODE FORWARD VOLTAGE

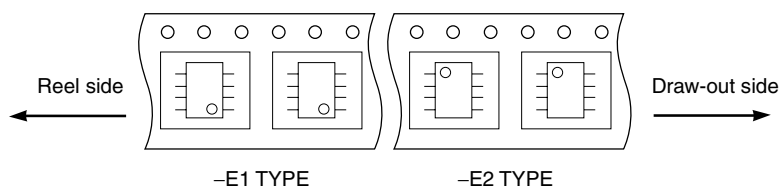


REVERSE RECOVERY TIME vs. DIODE FORWARD CURRENT

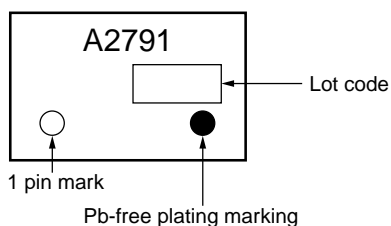


TAPE INFORMATION

There are two types (-E1, -E2) of taping depending on the direction of the device.



MARKING INFORMATION



RECOMMENDED SOLDERING CONDITIONS

The μPA2791GR should be soldered and mounted under the following recommended conditions.

For soldering methods and conditions other than those recommended below, please contact an NEC Electronics sales representative.

For technical information, see the following website.

Semiconductor Device Mount Manual (<http://www.necel.com/pkg/en/mount/index.html>)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Maximum temperature (Package's surface temperature): 260°C or below Time at maximum temperature: 10 seconds or less Time of temperature higher than 220°C: 60 seconds or less Preheating time at 160 to 180°C: 60 to 120 seconds Maximum number of reflow processes: 3 times Maximum chlorine content of rosin flux (percentage mass): 0.2% or less	IR60-00-3
Partial heating	Maximum temperature (Pin temperature): 350°C or below Time (per side of the device): 3 seconds or less Maximum chlorine content of rosin flux: 0.2% (wt.) or less	P350

Caution Do not use different soldering methods together (except for partial heating).

• **The information in this document is current as of November, 2007. The information is subject to change without notice. For actual design-in, refer to the latest publications of NEC Electronics data sheets or data books, etc., for the most up-to-date specifications of NEC Electronics products. Not all products and/or types are available in every country. Please check with an NEC Electronics sales representative for availability and additional information.**

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