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April 1st, 2010
Renesas Electronics Corporation

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R2S15901SP

Digital Delay IC for “Lip Sync”

REJ03F0151-0100

Rev.1.0

Apr 28, 2005

Description

R2S15901SP is a digital audio delay chip to synchronize the TV video and audio signals.

Features

- CMOS Technology
- 2-Channel 24-bit Audio signals delay
- Delay time is controlled by DC voltage (9steps: 1, 7/8, 3/4, 5/8, 1/2, 3/8, 1/4, 1/8 times)
- 43K bytes RAM up to delay 224ms(@fs = 32kHz)
When fs = 48kHz, maximum delay is 149ms.
- 2 3-state pins for 9-step configuration
- 3.3V signal input available

Recommended Operating Condition

Supply Voltage Range $V_{DD} = 2.5V$ (typ.)

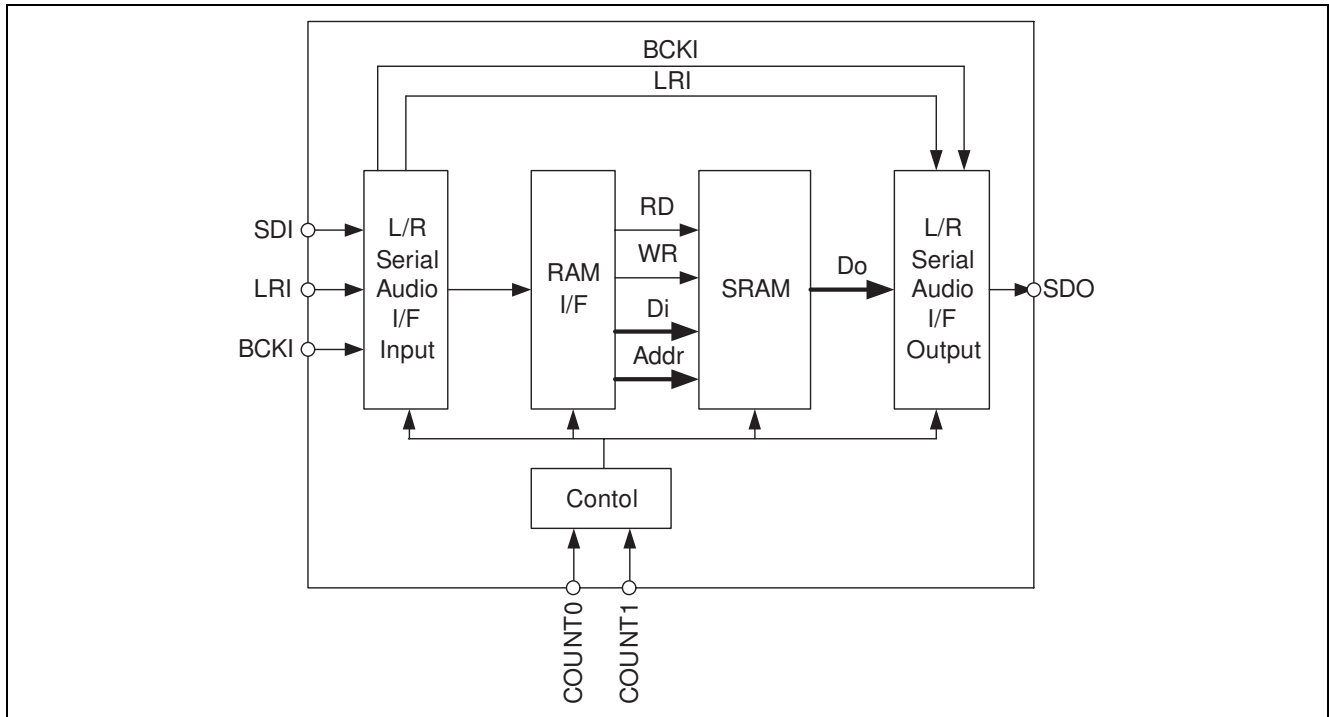
Circuit Current $I_{DD} = 1.0mA$ (typ.)

Operation Temperature $T_{opr} = -20$ to $75^{\circ}C$

Applications

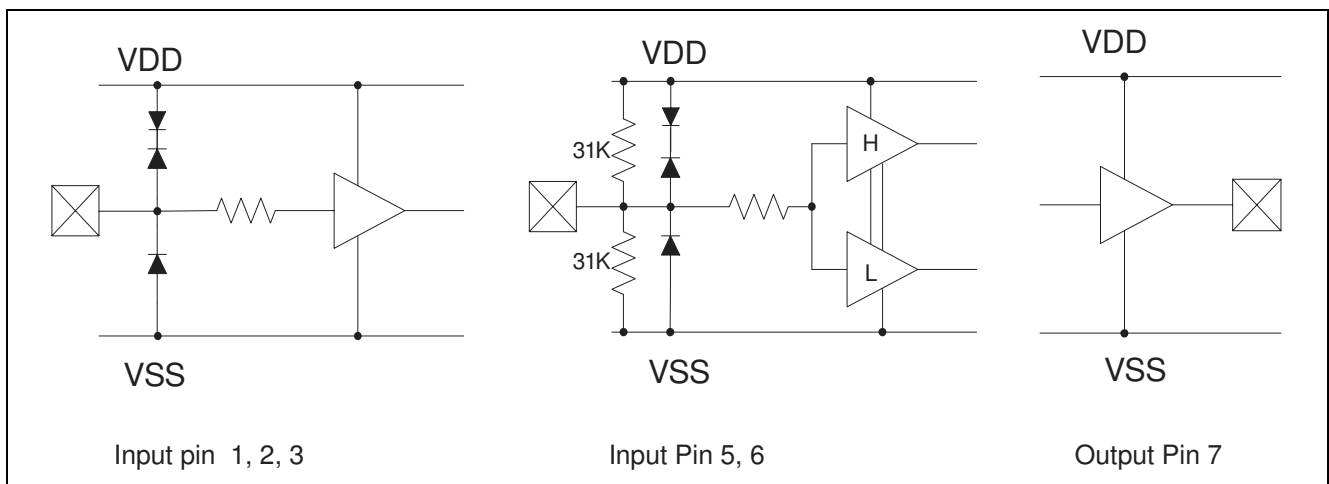
LCD TV, PDP, DVD Recorder, AV Amplifier

Block Diagram

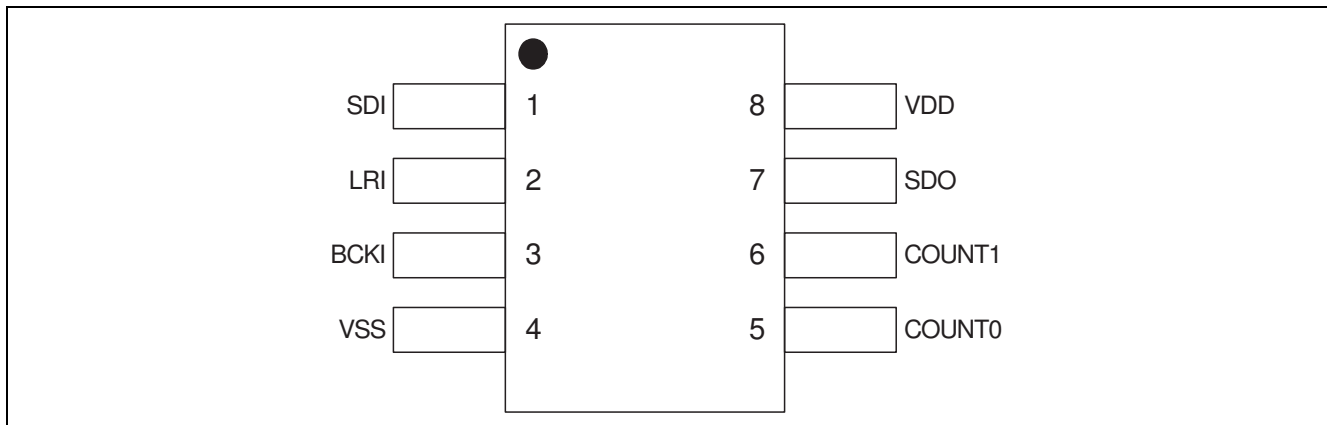


Input/Output Configuration

The schematic diagrams of the input and output circuits of the logic section are shown below:



Pin Configuration

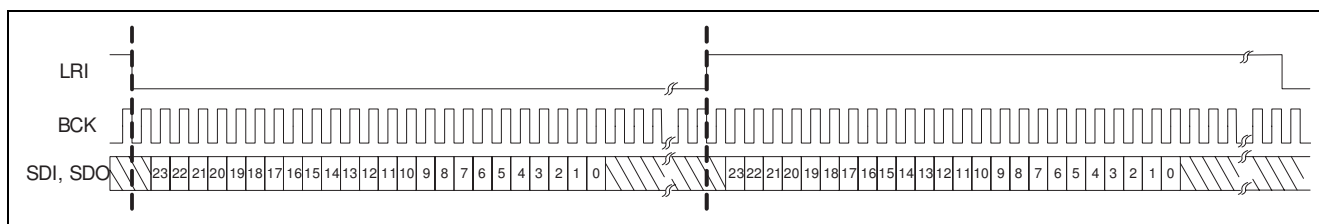


Pin Description

Pin No.	Pin Name	I/O	Description
1	SDI	I	- Serial audio data input - The input audio data are fetched at every LRI edge.
2	LRI	I	- LR clock - Audio sample frequency. - Low indicates the audio input data SDI and output data SDO are left channel data. - High indicates the audio input data SDI and output data SDO are right channel data.
3	BCKI	I	- Bit clock input - BCK clock is 64 times as large as LRI and input audio data.
4	VSS	—	Ground
5 6	COUNT0 COUNT1	I	- Delay time control 0 - Delay time control 1 - Delay time control pin. These two inputs are 3-state input pins that may be set high or low, or left unconnected to generate the third state. With the 3-state condition, 9-step delay time may be organized.
7	SDO	O	- Audio data output - This SDO is the delayed audio data output.
8	VDD	—	Power supply +2.5V

Function Description

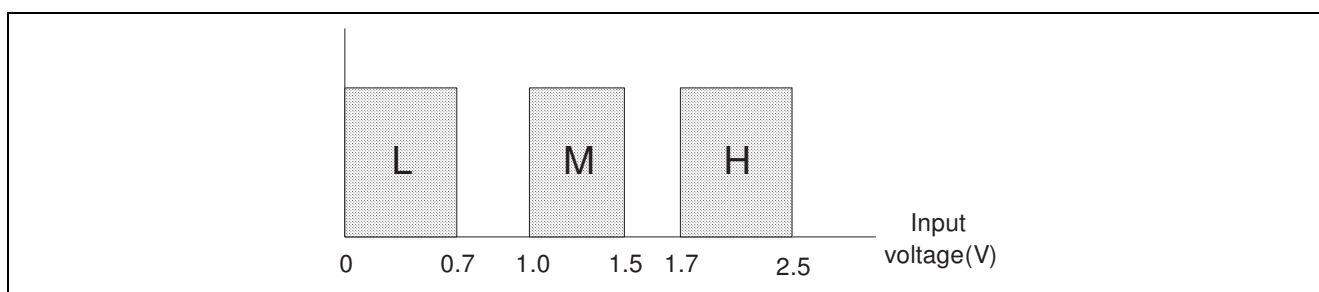
Serial Interface



The input audio data format is I²S 24-bit 64fs as above with the same as output.

Delay Time

The R2S15901SP provides 9 steps time delay by using two control pin COUNT0 and COUNT1. The two control pins provide 3-state respectively to generate 9 steps time delay. COUNT0 and COUNT1 may be tied to high, low or left unconnected. Internal comparator circuitry monitor input state to determine the input is high, low or middle state. Internal Pull high and low resistor keep input at $V_{DD}/2$. The comparator distinguishes terminal voltage level as below.



Sampling Rate (fs)	Max COUNT[1:0]=HH	7/8 COUNT[1:0]=HM	6/8 COUNT[1:0]=HL	5/8 COUNT[1:0]=MH
192kHz	37ms	33ms	28ms	23ms
96kHz	75ms	65ms	56ms	47ms
88.2kHz	81ms	71ms	61ms	51ms
48kHz	149ms	131ms	112ms	93ms
44.1kHz	163ms	142ms	122ms	102ms
32kHz	224ms	196ms	168ms	140ms
(Sampling Counts)	(7168)	(6272)	(5376)	(4480)

Sampling Rate (fs)	4/8 COUNT[1:0]=MM	3/8 COUNT[1:0]=ML	2/8 COUNT[1:0]=LH	1/8 COUNT[1:0]=LM	0 COUNT[1:0]=LL
192kHz	19ms	14ms	9ms	5ms	0ms
96kHz	37ms	28ms	19ms	9ms	0ms
88.2kHz	41ms	30ms	20ms	10ms	0ms
48kHz	75ms	56ms	37ms	19ms	0ms
44.1kHz	81ms	61ms	41ms	20ms	0ms
32kHz	112ms	84ms	56ms	28ms	0ms
(Sampling Counts)	(3584)	(2688)	(1792)	(896)	(0)

The delay time is evaluated by the following formula:

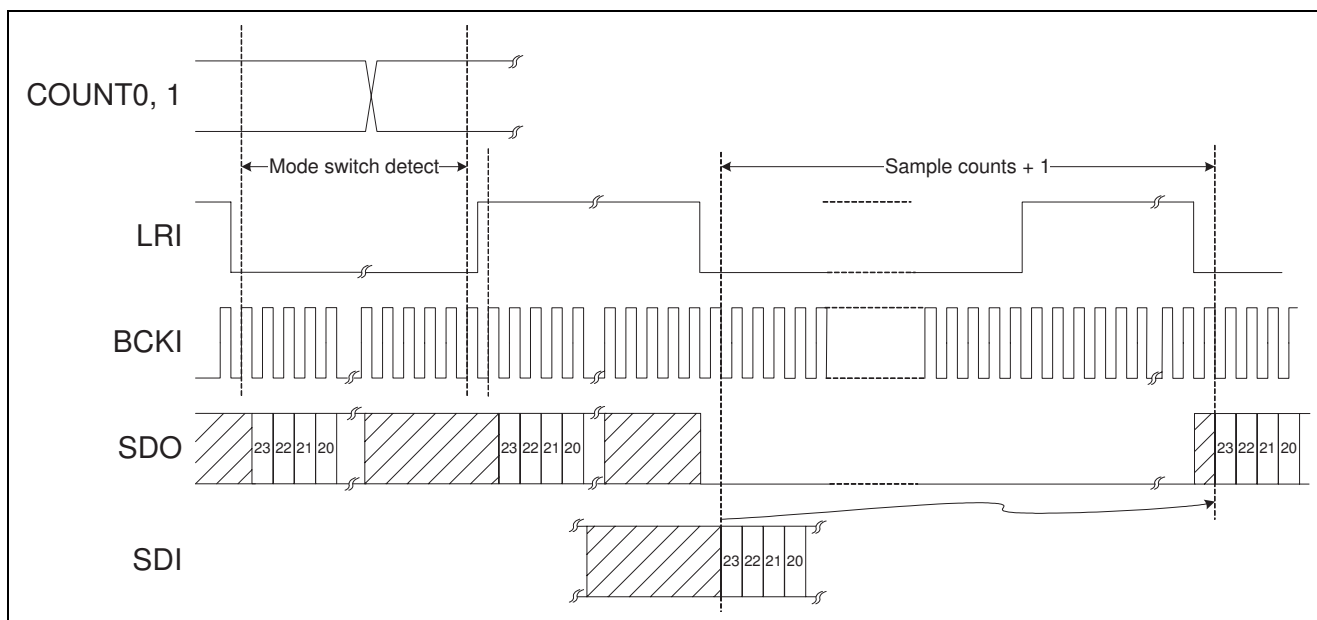
$$\text{Delay Time} = (1/\text{fs}) \times (\text{sampling counts} + 1) \text{ sec}$$

Mode Change

The R2S15901SP samples COUNT0 and COUNT1 pins while LRI is low by BCKI. When COUNT0 and COUNT1 are sampled and changed, they are detected at low interval of LRI. The delay counts start from the following falling edge of LRI with SDO to be delayed by sample counts + 1.

The SDO output is muted before the first new delay data being issued, when the new mode is recognized. An internal POR(Power On Reset) circuitry is to setup the initial mode right after power applied.

Digital Audio Delay



Mode change timing

Absolute Maximum Ratings

(Unless otherwise stated, $V_{DD} = 2.5V$, $V_{SS} = 0V$, $T_a = 25^{\circ}C$)

Parameter	Symbol	Ratings	Unit
Power supply voltage	V_{DD}	-0.3 to +2.75	V
Input pin voltage	V_I	-0.3 to 3.6	V
Power dissipation	P_D	100	mW
Operating temperature	T_{opr}	-20 to +75	$^{\circ}C$
Storage temperature	T_{stg}	-40 to +125	$^{\circ}C$

Electrical Characteristics

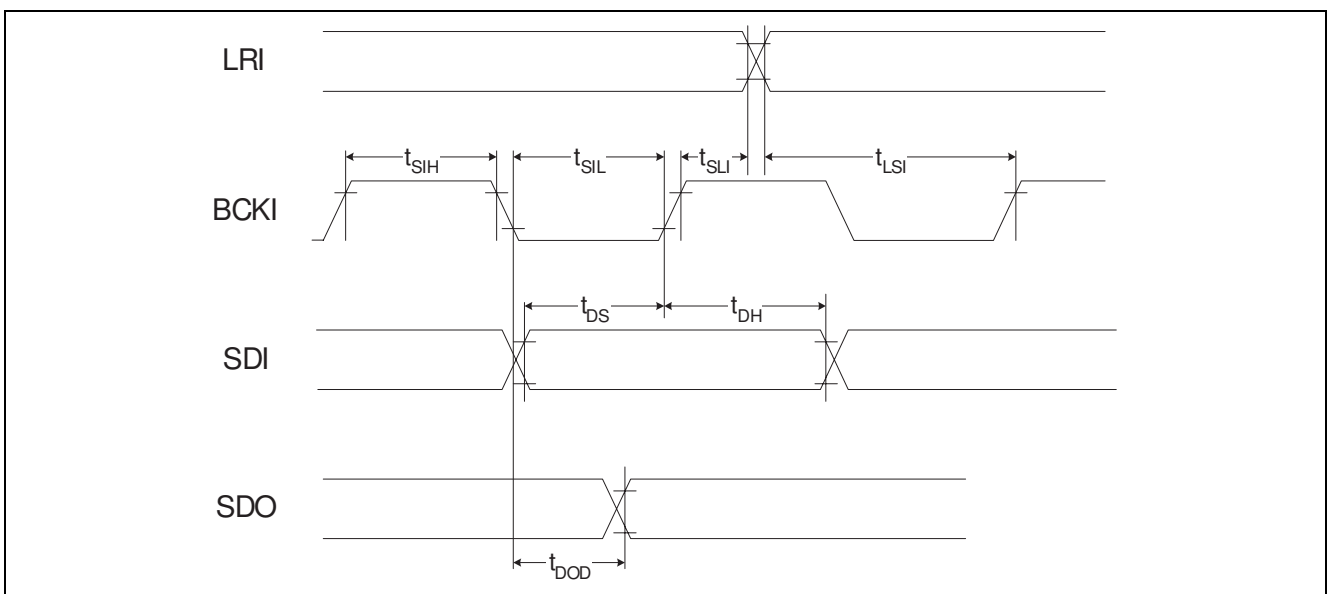
(Unless otherwise stated, $V_{DD} = 2.5V$, $V_{SS} = 0V$, $T_a = 25^\circ C$)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Operating V_{DD} voltage	V_{DD}	2.25	2.5	2.75	V	
Operating current	I_{DD}	—	1	—	mA	BCKI: 13MHz SDO: $C_L = 25pF$
High level input voltage	V_{IH}	1.7	—	3.3	V	LRI, SDI, BCKI
Low level input voltage	V_{IL}	—	—	0.7	V	LRI, SDI, BCKI
Output high voltage	V_{OH}	1.85	—	V_{DD}	V	$I_{OH} = -2mA$
Output low voltage	V_{OL}	0	—	0.4	V	$I_{OL} = 2mA$
Input high current	I_{IH}	-10	—	10	μA	$V_{IN} = V_{DD}$
Input high current with 31k Ω pull down	$I_{IH(PD)}$	40	80	160	μA	$V_{IN} = V_{DD}$ COUNT0, COUNT1
Input low current	I_{IL}	-10	—	10	μA	$V_{IN} = V_{SS}$
Input low current with 31 k Ω pull up	$I_{IL(PU)}$	-160	-80	-40	μA	$V_{IN} = V_{SS}$ COUNT0, COUNT1
Input capacitance	C_{IN}	—	10	—	pF	
Input rise/fall transition time	T_r/T_f	—	—	100	nS	

Serial Audio Timing

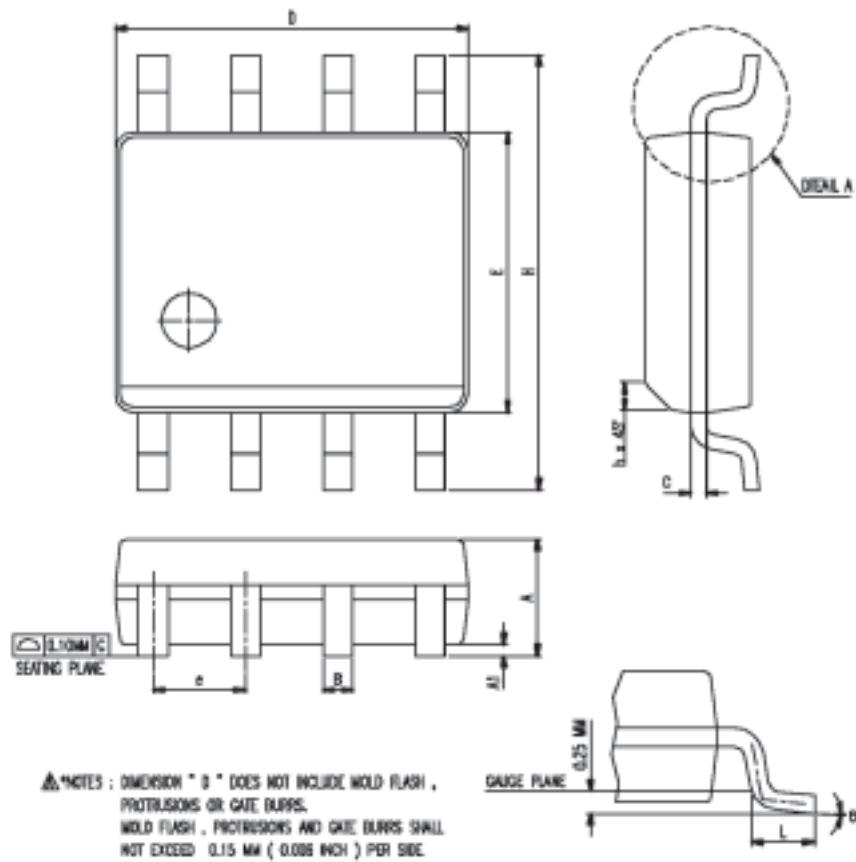
Serial Audio Input Timing Parameters

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Condition
BCKI frequency	f_{BCK}	—	—	13	MHz	
BCKI period	L pulse width	t_{SIL}	35	—	ns	
	H pulse width	t_{SIH}	35	—	ns	
BCKI to LRI time	t_{SLI}	15	—	—	ns	
LRI to BCKI time	t_{LSI}	15	—	—	ns	
Data Setup time	t_{DS}	15	—	—	ns	
Data Hold time	t_{DH}	15	—	—	ns	
Data output delay	t_{DOD}	—	—	15	ns	SDO: $C_L = 25pF$



Package Dimensions

8-Pin, SOP Package Body Size : 150mil Pin pitch : 1.27mm



SYMBOL	DIMENSION IN MM		DIMENSION IN INCH	
	MIN.	MAX.	MIN.	MAX.
A	1.35	1.75	0.0532	0.0688
A1	0.10	0.25	0.0040	0.0098
B	0.33	0.51	0.013	0.020
C	0.19	0.25	0.0075	0.0098
e	1.27 BSC		0.050 BSC	
D	4.80	5.00	0.1890	0.1968
H	5.80	6.20	0.2284	0.2440
E	3.80	4.00	0.1497	0.1574
L	0.40	1.27	0.016	0.050
h	0.25	0.50	0.0099	0.0196
g	G'	G'	G'	G'
JEDEC	MS-012 (AA)			

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