

R2A20168NP/SA/SP

8-bit 8ch D/A Converter with Buffer Amplifiers

R03DS0019EJ0100 Rev.1.00 2011.09.05

Description

The R2A20168 is an integrated circuit semiconductor of CMOS structure with 8 channels of built in D/A unnecessary and enabling configuration of a system with few component parts.

Serial data transfer type input can easily be used through a combination of three lines: DI, CLK, and LD. Outputs incorporate buffer op-amps that have a drive capacity of 1 mA or above for both sink source, and can operate over the entire voltage range from almost ground to Vcc (0 to 5V), making peripheral elements unnecessary and enabling configuration of a system with few component parts.

Very small QFN package is added to lineup. It is suitable for a small mounting and reduces the mounting area.

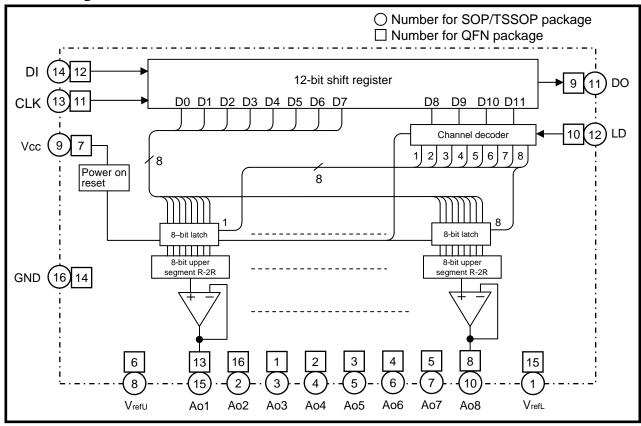
Features

- Guarantee Nonlinearity error : +/-1.0LSB, Differential nonlinearity error : +/-0.7LSB
- Data transfer format: 12-bit serial data input type by 3 wire (DI, SCK, LD)
- Output buffer op-amps: Operable over entire voltage range from almost ground to Vcc (0 to 5V)
- Very small size package line-up: QFN-16(pin pitch: 0.5mm), TSSOP-16(pin pitch 0.65mm)

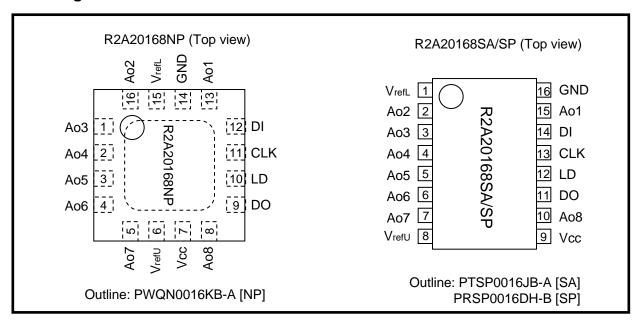
Application

- Conversion from digital data to analog control data for home-use and industrial equipment.
- Signal gain control or automatic adjustment of LCD-TV, PDP-TV or LCD display-monitor.
- Blurring correction control or various control of the interchangeable lens of digital still camera.
- Automatic adjustment by combination with microcomputer and EEPROM. (substitution of half fixed resistance)

Block Diagram



Pin Arrangement



Pin Description

Pin	No.						
[QFN]	[TSSOP /SOP]	Symbol	Function				
12	14	DI	Serial data input terminal. (Input serial data with a 12-bit data length)				
11	13	CLK	Serial clock input terminal (Input signal from DI terminal is input to 12-bit shift register at rise of serial clock.)				
10	12	LD	Load terminal (When High level is input to LD terminal, value in 12-bit shift register is loaded into decoder and 8-bit latch.)				
9	11	Do	Serial data output terminal (Data is sequentially output from the MSB bit.)				
13	15	Ao1					
16	2	Ao2					
1	3	Ao3					
2	4	Ao4	8-bit resolution D/A converter output terminals				
3	5	Ao5	(After power on, all channels are reset and DAC data 00h is output.)				
4	6	Ao6					
5	7	Ao7					
8	10	Ao8					
7	9	Vcc	Power supply terminal				
14	16	GND	GND terminal				
6	8	VrefU	D/A converter upper reference voltage input terminal				
15	1	VrefL	D/A converter lower reference voltage input terminal				

Absolute Maximum Ratings

(Ta= +25deg unless otherwise noted)

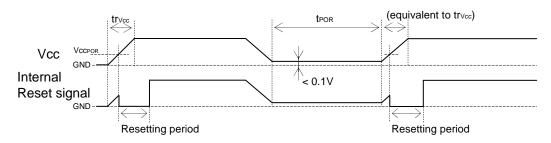
Item	Symbol	Conditions	Ratings	Unit
Supply voltage	Vcc		-0.3 to +6.5	V
D/A converter upper reference voltage	VrefU		-0.3 to +6.5	V
D/A converter lower reference voltage	VrefL		-0.3 to +6.5	V
Buffer amplifier output current	Iao	Continuous	-2.0 to +2.0	mA
Input voltage	Vin		-0.3 to Vcc+0.3 <+6.5	V
Output voltage	Vo		-0.3 to Vcc+0.3 <+6.5	V
Power dissipation	Pd	Ta= +85deg	290(NP) / 150(SA) / 300(SP)	mW
Thermal derating factor	K theta	Ta> +25deg	7.25(NP) / 3.75(SA) / 7.5(SP)	mW/deg
Operating temperature	Topr		-30 to +85	deg
Storage temperature	Tstg		-40 to +125	deg

Electrical Characteristics

« Digital Part » (Vcc, VrefU = +5V +/-10%, Vcc>VrefU, GND, VrefL =0V, Ta= -30 to +85deg, Unless otherwise noted)

lto	0	Tool conditions		1114		
Item	Symbol	Test conditions	Min	Тур	Max	Unit
Supply voltage	Vcc		2.7	5.0	5.5	V
Supply current	Icc	CLK =1MHz, Vcc =5V, Iao =0µA	-	0.4	1.2	mA
Input leak current	lilk	Vin = 0 to Vcc	-10	-	10	μA
Input low voltage V _I ∟			-	-	0.2Vcc	V
Input high voltage	Vih		0.8Vcc	-	-	V
Outrot love valtage	V	4.0V < Vcc, IoL = 2.0mA	-	-	0.4	V
Output low voltage	Vol	Vcc < 4.0V, IoL = 1.5mA	-	-	0.4	V
Output high voltage	Vон	Іон = -400µА	Vcc - 0.4	-	-	V
Supply voltage rise time *1	trvcc	Vcc = 0 to 2.7V	100	-	-	μs
Internal reset operating voltage *1	Vccpor	Vcc = 0 to 2.7V	-	1.5	1.9	V
Power supply restart interval (Power supply OFF → ON) *1	t por	Vcc < 0.1V	1	-	-	ms

*1 : When power supply is turned on, internal circuit is initialized by power on reset circuit. But, if re-powered on quickly, initialize is not operate. So, keep the time period of re-powered on (tpor).



« Analog Part » (Vcc, VrefU = +5V +/-10%, Vcc>VrefU, GND, VrefL =0V, Ta= -30 to +85deg, Unless otherwise noted)

ltom	Compleal	Toot conditions		l lmit		
Item	Symbol	Test conditions	Min	Тур	Max	Unit
Current dissipation	I refU	V _{refU} =5V, V _{refL} =0V, I _A 0=0μA, Data condition: at maximum current	-	1.0	2.0	mA
D/A converter upper reference voltage range *2	VrefU		0.7Vcc	-	Vcc	٧
D/A converter lower reference voltage range *2			GND	-	0.3Vcc	٧
Buffer amplifier output	Vao	IAO = +/- 100 μA	0.1	-	Vcc - 0.1	V
voltage range		Iao = +/- 500 μA	0.2	-	Vcc - 0.2	V
Buffer amplifier output drive range	IAO	Upper side saturation voltage = 0.3V, Lower side saturation voltage = 0.2V	-1.0	-	1.0	mA
Differential nonlinearity	SDL	V _{refU} = 4.79V,	-0.7	-	0.7	LSB
Nonlinearity	SL	V _{refL} = 0.95V,	-1.0	-	1.0	LSB
Zero code error	Szero	Vcc = 5.5V (15mV/LSB),	-2.0	-	2.0	LSB
Full scale error	SFULL	Without load (I _{AO} =0μA)	-2.0	-	2.0	LSB
Output capacitive load	Co		-	-	0.1	μF
Buffer amplifier output impedance	Ro		-	5.0	-	ohm

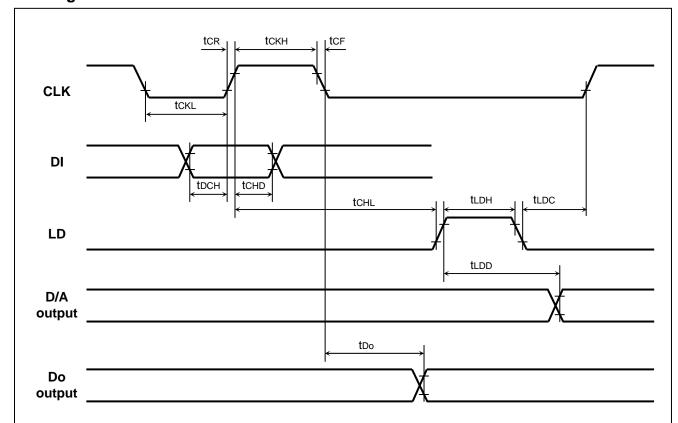
^{*2 :} The output does not necessary be the value with the reference voltage setting range. The output value is determined by the buffer amplifier output voltage range (VAO).

AC Characteristics

(Vcc, $V_{refU} = +5V + /-10\%$, $Vcc \ge V_{refU}$, $GND = V_{refL} = 0V$, Ta = -30 to +85deg, unless otherwise noted)

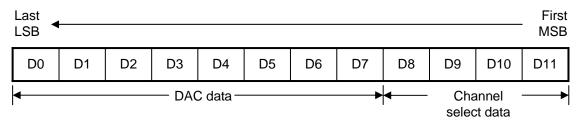
			Limits			
Item	Symbol Test conditions		Min	Тур	Max	Unit
Clock frequency	fclk		-	1.0	10	MHz
Clock low pulse width	tckl		40	-	-	ns
Clock high pulse width	tскн		40	-	-	ns
Clock rise time	tcr		-	-	200	ns
Clock fall time	tcF		-	-	200	ns
Data setup time	tосн		4	-	-	ns
Data hold time	tchd		30	-	-	ns
LD setup time	tchl		40	-	-	ns
LD hold time	tldc		40	-	-	ns
LD high pulse width	t LDH		40	-	-	ns
Data output delay time	tDO	CL < 100 pF	-10	-	50	ns
D/A output settling time tldd		Ta=25deg, CL<100pF, VAO: 0.5←→4.5V, The time until the output becomes the final value of 1/2 LSB.	-	-	150	μs

Timing Chart



(Note) Timing chart above is a schematic representation of the timing of each signal type. CLK signal input is High or Low regardless, LD signal High input is enabled.

Digital Data Format



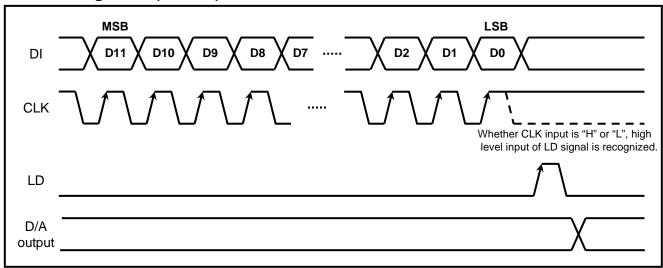
Channel select data

D8	D9	D10	D11	Chanel Selection
0	0	0	0	Don't care
0	0	0	1	Ao1 select
0	0	1	0	Ao2 select
0	0	1	1	Ao3 select
0	1	0	0	Ao4 select
0	1	0	1	Ao5 select
0	1	1	0	Ao6 select
0	1	1	1	Ao7 select
1	0	0	0	Ao8 select
1	0	0	1	Don't care
:	•••	:		:
1	1	1	0	Don't care
1	1	1	1	Don't care

DAC data

D0	D1	D2	D3	D4	D5	D6	D7	D/A Output
0	0	0	0	0	0	0	0	(VrefU - VrefL) / 256 x 1 + VrefL
1	0	0	0	0	0	0	0	(VrefU - VrefL) / 256 x 2 + VrefL
0	1	0	0	0	0	0	0	(VrefU - VrefL) / 256 x 3 + VrefL
1	1	0	0	0	0	0	0	(VrefU - VrefL) / 256 x 4 + VrefL
:	:	:	:	:	:	:	:	:
0	1	1	1	1	1	1	1	(VrefU - VrefL) / 256 x 255 + VrefL
1	1	1	1	1	1	1	1	VrefU

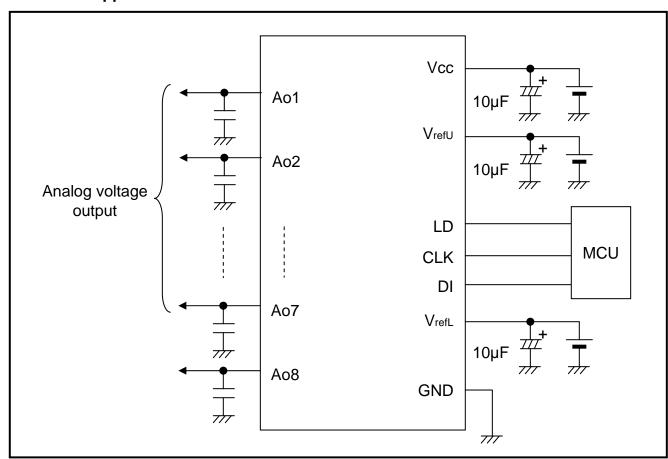
Data Timing Chart (Model)



Precaution For Use

- There are three terminals (Vcc, V_{refU}, V_{refL}) that should be impressed a constant voltage. When ripple or spike noise is input to this terminal, there is fear that the accuracy of D/A conversion becomes lower and this IC malfunction. So, when use this IC, please connect capacitor between these terminals (Vcc, V_{refU}, V_{refL}) and GND for stable D/A conversion.
- This IC's output amplifier has an advantage to capacitive load, So, it's no problem at device action when connect capacitor (0.1µF Max) among output to GND for every noise elimination.

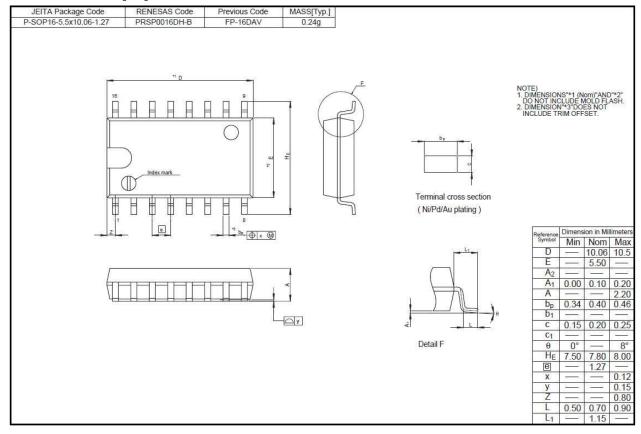
Standard Application Circuit



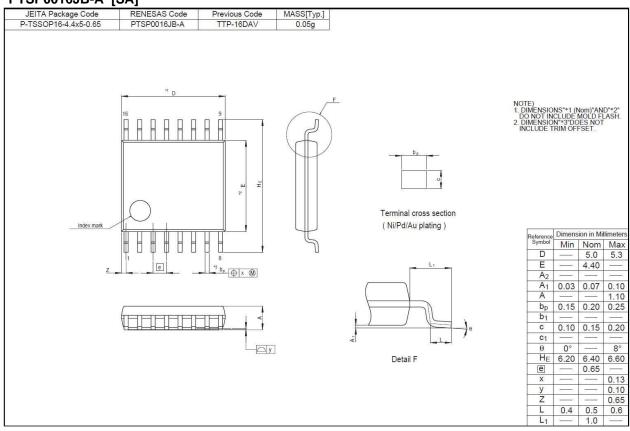
New Product

Package Dimensions

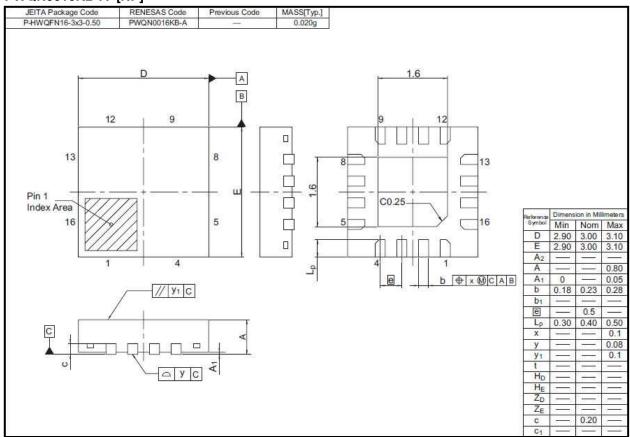
PRSP0016DH-B [SP]



PTSP0016JB-A [SA]



PWQN0016KB-A [NP]



Ordering Information

Order part No.	Package Name	Package Code	Package type No.	Packing/Quantity
R2A20168SP	SOP-16	PRSP0016DH-B	SP	Embossed Taping/2,000 pcs.
R2A20168SA	TSSOP-16	RTSP0016JB-A	SA	Embossed Taping/2,000 pcs.
R2A20168NP	QFN-16	PWQN0016KB-A	NP	Embossed Taping/3,000 pcs.

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