

# NP90N055VUK

## MOS FIELD EFFECT TRANSISTOR

R07DS0578EJ0100

Rev.1.00

Nov 29, 2011

### Description

The NP90N055VUK is N-channel MOS Field Effect Transistor designed for high current switching applications.

### Features

- Super low on-state resistance  
 $R_{DS(on)} = 3.85 \text{ m}\Omega \text{ MAX. (} V_{GS} = 10 \text{ V, } I_D = 45 \text{ A)}$
- Low  $C_{iss}$ :  $C_{iss} = 4000 \text{ pF TYP. (} V_{DS} = 25 \text{ V)}$
- Designed for automotive application and AEC-Q101 qualified

### Ordering Information

Part No.	Lead Plating	Packing		Package
NP90N055VUK-E1-AY *1	Pure Sn (Tin)	Tape 2500 p/reel	Taping (E1 type)	TO-252 (MP-3ZP)
NP90N055VUK-E2-AY *1			Taping (E2 type)	

Note: \*1 Pb-free (This product does not contain Pb in the external electrode)

### Absolute Maximum Ratings ( $T_A = 25^\circ\text{C}$ )

Item	Symbol	Ratings	Unit
Drain to Source Voltage ( $V_{GS} = 0 \text{ V}$ )	$V_{DSS}$	55	V
Gate to Source Voltage ( $V_{DS} = 0 \text{ V}$ )	$V_{GSS}$	$\pm 20$	V
Drain Current (DC) ( $T_C = 25^\circ\text{C}$ )	$I_{D(DC)}$	$\pm 90$	A
Drain Current (pulse) *1	$I_{D(pulse)}$	$\pm 360$	A
Total Power Dissipation ( $T_C = 25^\circ\text{C}$ )	$P_{T1}$	147	W
Total Power Dissipation ( $T_A = 25^\circ\text{C}$ )	$P_{T2}$	1.2	W
Channel Temperature	$T_{ch}$	175	$^\circ\text{C}$
Storage Temperature	$T_{stg}$	-55 to 175	$^\circ\text{C}$
Repetitive Avalanche Current *2	$I_{AR}$	33	A
Repetitive Avalanche Energy *2	$E_{AR}$	108	mJ

Notes: \*1  $T_C = 25^\circ\text{C}$ ,  $P_W \leq 10 \text{ }\mu\text{s}$ , Duty Cycle  $\leq 1\%$

\*2  $R_G = 25 \text{ }\Omega$ ,  $V_{GS} = 20 \rightarrow 0 \text{ V}$

### Thermal Resistance

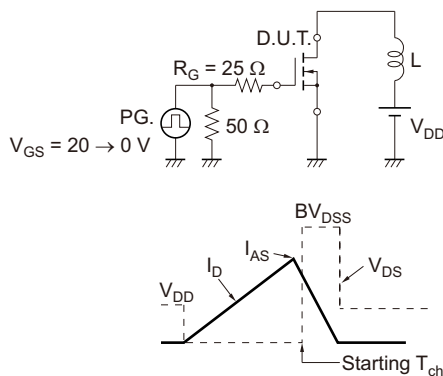
Channel to Case Thermal Resistance	$R_{th(ch-C)}$	1.02	$^\circ\text{C/W}$
Channel to Ambient Thermal Resistance	$R_{th(ch-A)}$	125	$^\circ\text{C/W}$

Electrical Characteristics ( $T_A = 25^\circ\text{C}$ )

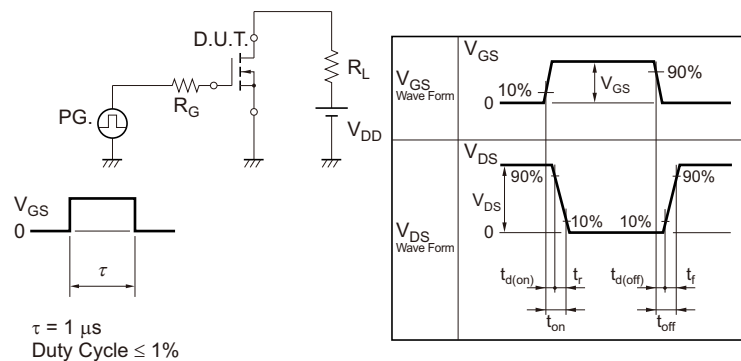
Item	Symbol	MIN.	TYP.	MAX.	Unit	Test Conditions
Zero Gate Voltage Drain Current	$I_{DSS}$	—	—	1	$\mu\text{A}$	$V_{DS} = 55\text{ V}, V_{GS} = 0\text{ V}$
Gate Leakage Current	$I_{GSS}$	—	—	$\pm 100$	nA	$V_{GS} = \pm 20\text{ V}, V_{DS} = 0\text{ V}$
Gate to Source Threshold Voltage	$V_{GS(th)}$	2.0	3.0	4.0	V	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$
Forward Transfer Admittance *1	$ y_{fs} $	30	60	—	S	$V_{DS} = 5\text{ V}, I_D = 45\text{ A}$
Drain to Source On-state Resistance *1	$R_{DS(on)}$	—	3.20	3.85	m $\Omega$	$V_{GS} = 10\text{ V}, I_D = 45\text{ A}$
Input Capacitance	$C_{iss}$	—	4000	6000	pF	$V_{DS} = 25\text{ V}$ $V_{GS} = 0\text{ V}$ $f = 1\text{ MHz}$
Output Capacitance	$C_{oss}$	—	410	620	pF	
Reverse Transfer Capacitance	$C_{rss}$	—	150	270	pF	
Turn-on Delay Time	$t_{d(on)}$	—	25	60	ns	$V_{DD} = 28\text{ V}, I_D = 45\text{ A}$ $V_{GS} = 10\text{ V}$ $R_G = 0\text{ }\Omega$
Rise Time	$t_r$	—	10	30	ns	
Turn-off Delay Time	$t_{d(off)}$	—	65	130	ns	
Fall Time	$t_f$	—	6	20	ns	
Total Gate Charge	$Q_G$	—	68	102	nC	$V_{DD} = 44\text{ V}$
Gate to Source Charge	$Q_{GS}$	—	18	—	nC	$V_{GS} = 10\text{ V}$
Gate to Drain Charge	$Q_{GD}$	—	18	—	nC	$I_D = 90\text{ A}$
Body Diode Forward Voltage *1	$V_{F(S-D)}$	—	0.9	1.5	V	$I_F = 90\text{ A}, V_{GS} = 0\text{ V}$
Reverse Recovery Time	$t_{rr}$	—	47	—	ns	$I_F = 90\text{ A}, V_{GS} = 0\text{ V}$
Reverse Recovery Charge	$Q_{rr}$	—	80	—	nC	$di/dt = 100\text{ A}/\mu\text{s}$

Note: \*1 Pulsed test

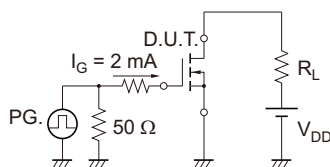
## TEST CIRCUIT 1 AVALANCHE CAPABILITY



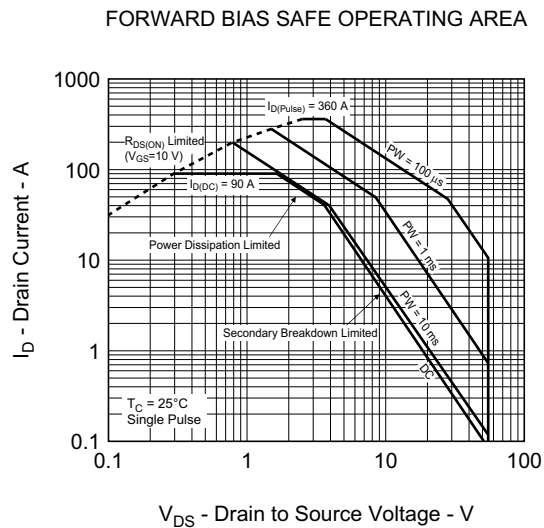
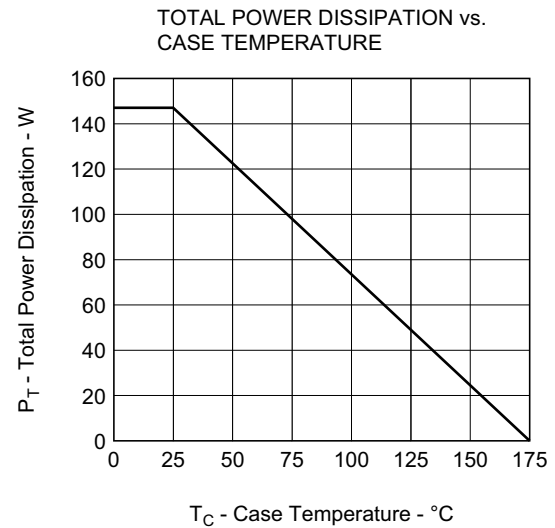
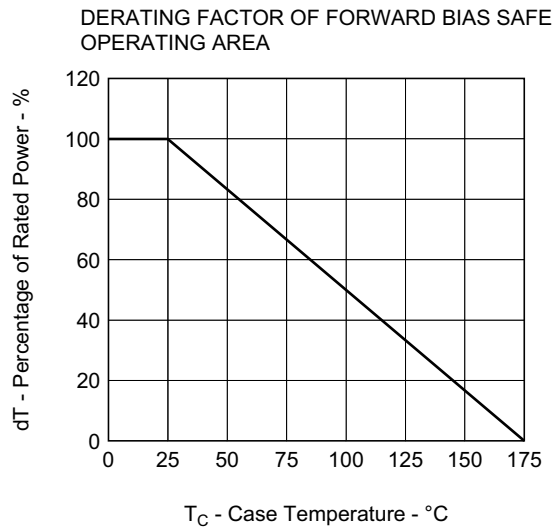
## TEST CIRCUIT 2 SWITCHING TIME



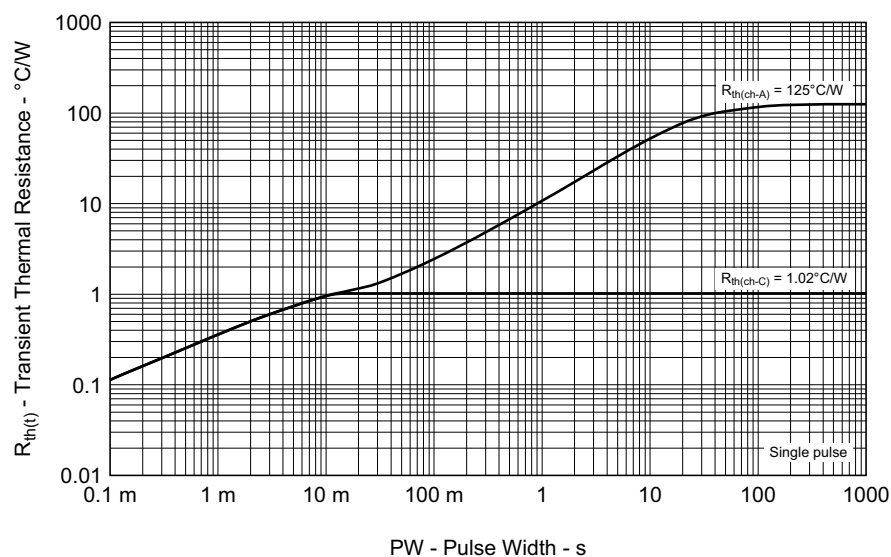
## TEST CIRCUIT 3 GATE CHARGE

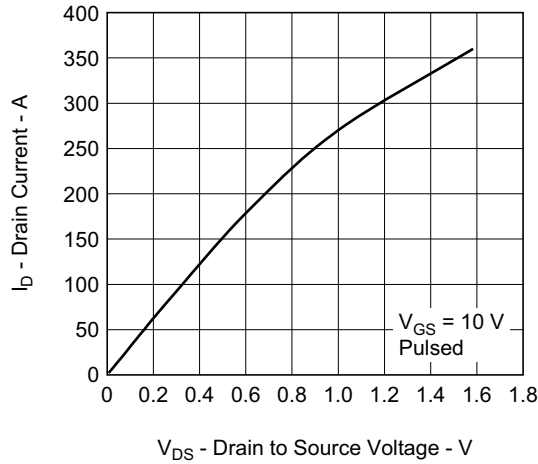


## Typical Characteristics ( $T_A = 25^\circ\text{C}$ )

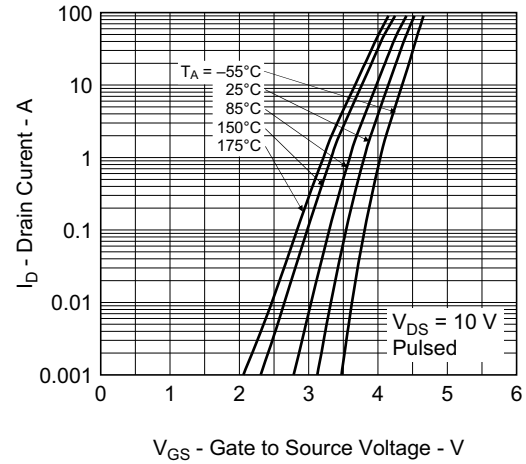
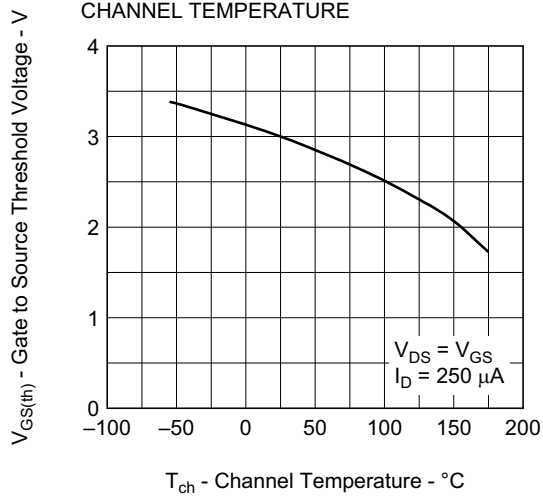
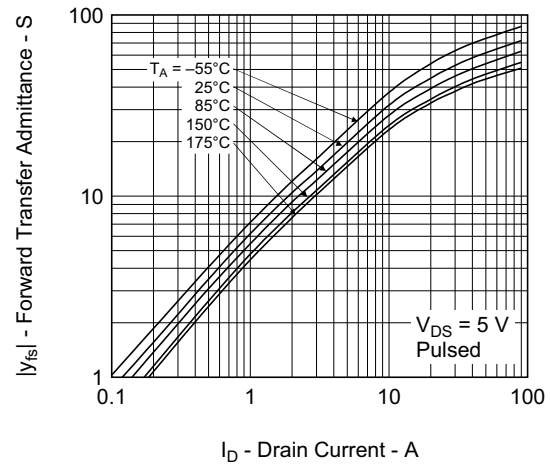
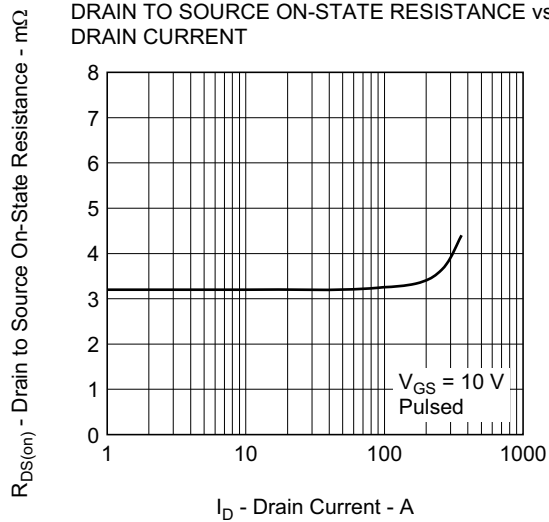
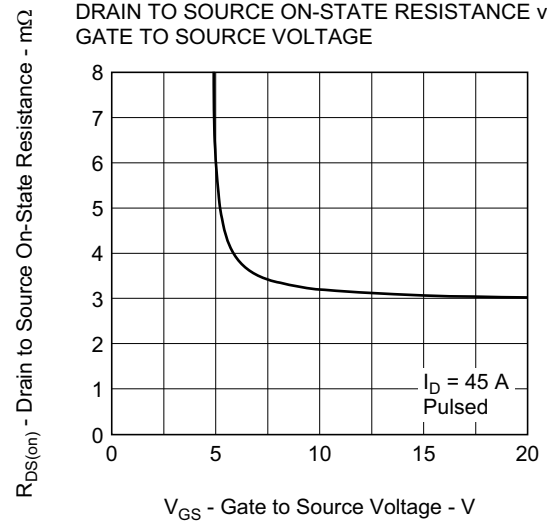


TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH

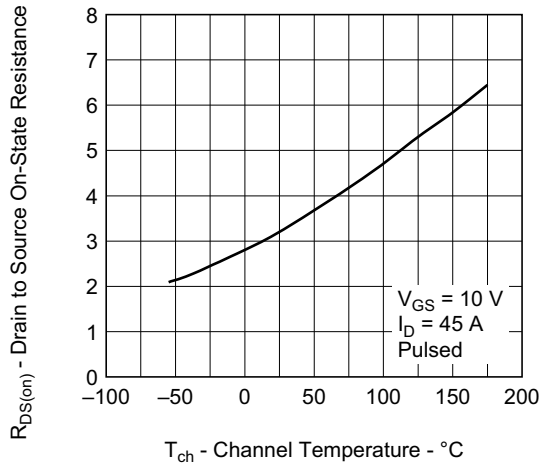


DRAIN CURRENT vs.  
DRAIN TO SOURCE VOLTAGE

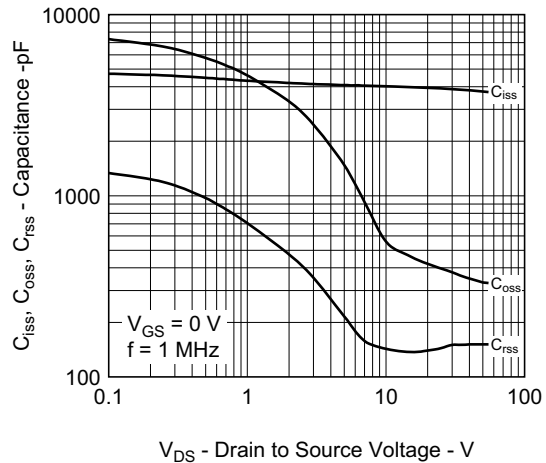
FORWARD TRANSFER CHARACTERISTICS

GATE TO SOURCE THRESHOLD VOLTAGE vs.  
CHANNEL TEMPERATUREFORWARD TRANSFER ADMITTANCE vs.  
DRAIN CURRENTDRAIN TO SOURCE ON-STATE RESISTANCE vs.  
DRAIN CURRENTDRAIN TO SOURCE ON-STATE RESISTANCE vs.  
GATE TO SOURCE VOLTAGE

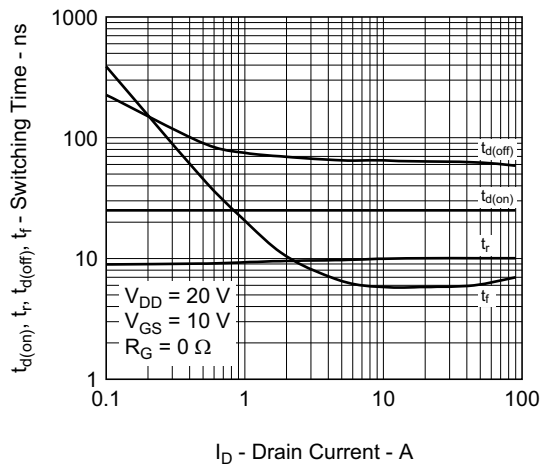
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



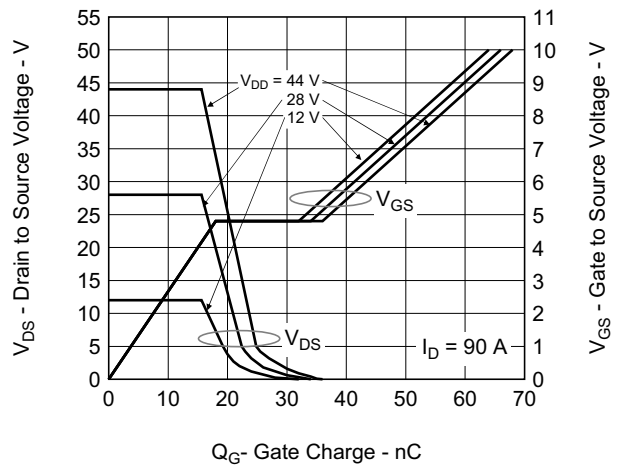
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



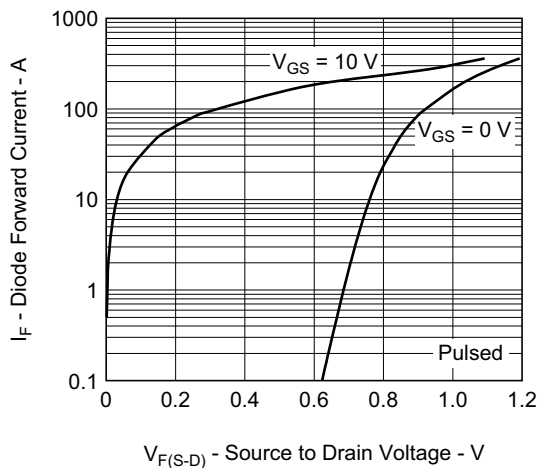
SWITCHING CHARACTERISTICS



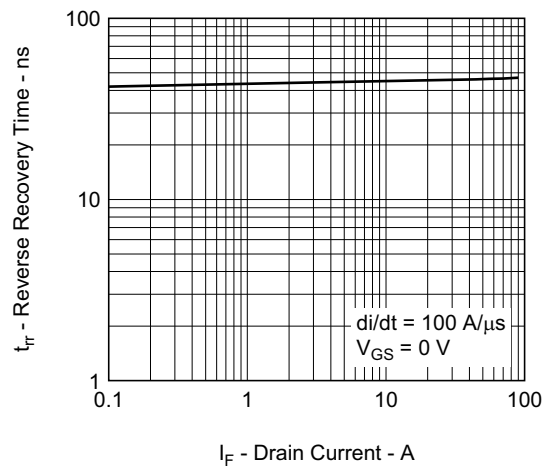
DYNAMIC INPUT/OUTPUT CHARACTERISTICS



SOURCE TO DRAIN DIODE FORWARD VOLTAGE



REVERSE RECOVERY TIME vs. DRAIN CURRENT





<b>Revision History</b>	<b>NP90N055VUK Data Sheet</b>
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Rev.	Date	Description	
		Page	Summary
1.00	Nov 29, 2011	—	First Edition Issued

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