

NP75P04YLG

MOS FIELD EFFECT TRANSISTOR

R07DS0183EJ0200 Rev.2.00 Mar 16, 2011

Description

The NP75P04YLG is P-channel MOS Field Effect Transistor designed for high current switching applications.

Features

- Low on-state resistance
 - --- $R_{DS(on)}$ = 9.7 mΩ MAX. (V_{GS} = -10 V, I_D = -37.5 A)
 - --- $R_{DS(on)}$ = 14 mΩ MAX. (V_{GS} = -5 V, I_D = -37.5 A)
- Logic level drive type
- Gate to Source ESD protection diode built in
- Designed for automotive application and AEC-Q101 qualified

Ordering Information

Part No.	LEAD PLATING	PACKING	Package
NP75P04YLG -E1-AY *1	Pure Sn (Tin)	Tape 2500 p/reel	8-pin HSON, Taping (E1 type)
NP75P04YLG -E2-AY *1			8-pin HSON, Taping (E2 type)

Note: *1. Pb-free (This product does not contain Pb in the external electrode.)

Absolute Maximum Ratings ($T_A = 25^{\circ}C$)

Item	Symbol	Ratings	Unit
Drain to Source Voltage (V _{GS} = 0 V)	V_{DSS}	-40	V
Gate to Source Voltage (V _{DS} = 0 V)	V_{GSS}	∓20	V
Drain Current (DC) (T _C = 25°C)	I _{D(DC)}	∓75	Α
Drain Current (pulse) *1	I _{D(pulse)}	∓225	Α
Total Power Dissipation (T _C = 25°C)	P _{T1}	138	W
Total Power Dissipation ($T_A = 25^{\circ}C$) *2	P _{T2}	1.0	W
Channel Temperature	T _{ch}	175	°C
Storage Temperature	T _{stg}	−55 to +175	°C
Single Avalanche Current *3	I _{AS}	35	Α
Single Avalanche Energy *3	E _{AS}	123	mJ

Thermal Resistance

Channel to Case Thermal Resistance $R_{th(ch-C)}$ 1.09 °C/W Channel to Ambient Thermal Resistance *2 $R_{th(ch-A)}$ 150 °C/W

Notes: *1. $T_C = 25^{\circ}C$, PW $\leq 10 \mu s$, Duty Cycle $\leq 1\%$

*2. Mounted on glass epoxy substrate of 40 mm x 40 mm x 0.8 mmt

*3. Starting T_{ch} = 25°C, V_{DD} = -20 V, R_G = 25 Ω , L = 100 μ H, V_{GS} = -20 \rightarrow 0 V

The mark <R> shows major revised points.

The revised points can be easily searched by copying an "<R>" in the PDF file and specifying it in the "Find what:" field.





Electrical Characteristics ($T_A = 25^{\circ}C$)

Item	Symbol	Min	Тур	Max	Unit	Test Conditions
Zero Gate Voltage Drain Current	I _{DSS}			-1	μΑ	$V_{DS} = -40 \text{ V}, V_{GS} = 0 \text{ V}$
Gate Leakage Current	I _{GSS}			∓10	μΑ	$V_{GS} = \mp 20 \text{ V}, V_{DS} = 0 \text{ V}$
Gate to Source Threshold Voltage	$V_{GS(th)}$	-1.0	-1.7	-2.5	V	$V_{DS} = V_{GS}, I_{D} = -250 \mu A$
Forward Transfer Admittance *1	y _{fs}	31	63		S	$V_{DS} = -5 \text{ V}, I_{D} = -37.5 \text{ A}$
Drain to Source On-state	R _{DS(on)1}		7.7	9.7	mΩ	$V_{GS} = -10 \text{ V}, I_D = -37.5 \text{ A}$
Resistance *1	R _{DS(on)2}		9.3	14	mΩ	$V_{GS} = -5 \text{ V}, I_{D} = -37.5 \text{ A}$
Input Capacitance	C _{iss}		3200	4800	pF	$V_{DS} = -25 \text{ V},$
Output Capacitance	Coss		460	600	pF	$V_{GS} = 0 V$,
Reverse Transfer Capacitance	C _{rss}		250	450	pF	f = 1 MHz
Turn-on Delay Time	t _{d(on)}		12	24	ns	$V_{DD} = -20 \text{ V}, I_D = -37.5 \text{ A},$
Rise Time	t _r		11	27	ns	$V_{GS} = -10 \text{ V},$
Turn-off Delay Time	t _{d(off)}		320	640	ns	$R_G = 0 \Omega$
Fall Time	t _f		180	440	ns	
Total Gate Charge	Q_{G}		91	140	nC	$V_{DD} = -32 \text{ V},$
Gate to Source Charge	Q_{GS}		14		nC	$V_{GS} = -10 \text{ V},$
Gate to Drain Charge	Q_{GD}		26		nC	I _D = -75 A
Body Diode Forward Voltage *1	$V_{F(S-D)}$		1.02	1.5	V	$I_F = -75 \text{ A}, V_{GS} = 0 \text{ V}$
Reverse Recovery Time	t _{rr}		43		ns	$I_F = -75 \text{ A}, V_{GS} = 0 \text{ V},$
Reverse Recovery Charge	Q _{rr}		57		nC	$di/dt = -100 A/\mu s$

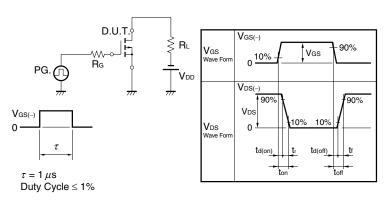
Note: *1. Pulsed

TEST CIRCUIT 1 AVALANCHE CAPABILITY

<u>B</u>V_{DSS}

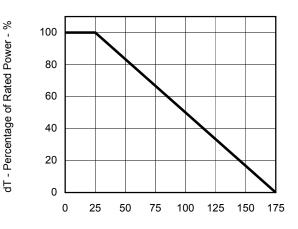


TEST CIRCUIT 2 SWITCHING TIME



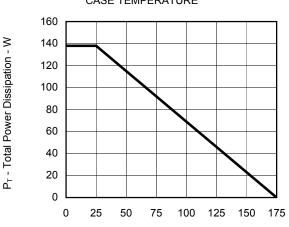
Typical Characteristics (T_A = 25°C)

DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



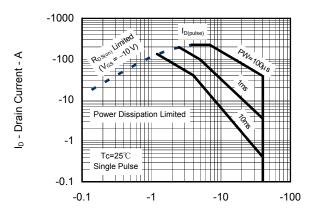
 T_{C} - Case Temperature - $^{\circ}\text{C}$

TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



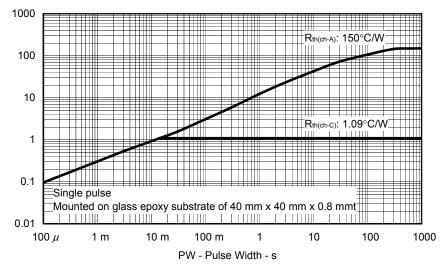
T_C - Case Temperature - °C

FORWARD BIAS SAFE OPERATING AREA



 $V_{\text{\scriptsize DS}}$ - Drain to Source Voltage - V

TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH

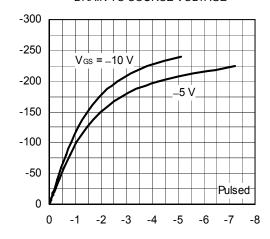


I_D - Drain Current - A

V_{GS(th)} - Gate to Source Threshold Voltage - V

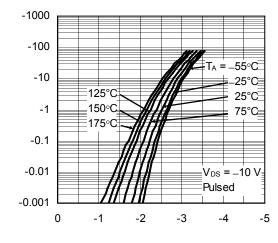
 $R_{\text{DS}(\text{on})}$ - Drain to Source On-state Resistance - $m\Omega$

DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



V_{DS} - Drain to Source Voltage - V

FORWARD TRANSFER CHARACTERISTICS

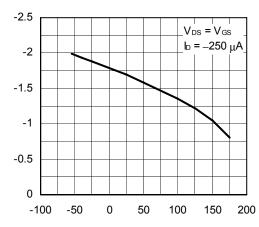


Ip - Drain Current - A

y_{fs} | - Forward Transfer Admittance - S

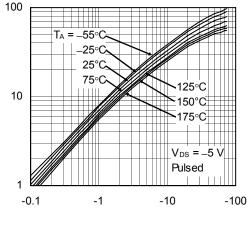
V_{GS} - Gate to Source Voltage - V

GATE TO SOURCE THRESHOLD VOLTAGE vs. CHANNEL TEMPERATURE



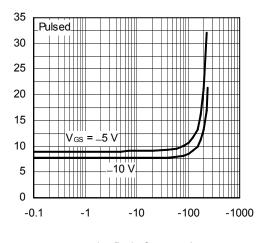
T_{ch} - Channel Temperature - °C

FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



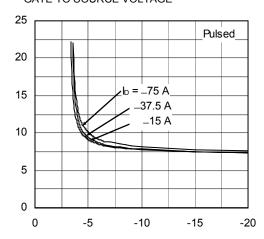
I_D - Drain Current - A

DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



 $\mbox{\rm I}_{\mbox{\scriptsize D}}$ - Drain Current - A

DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



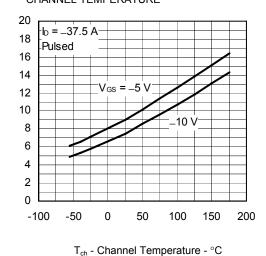
 V_{GS} - Gate to Source Voltage - V

 $R_{\text{DS}(\text{on})}$ - Drain to Source On-state Resistance - $m\Omega$

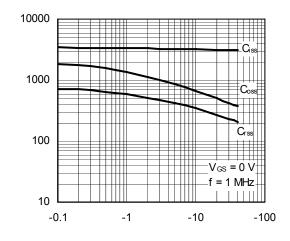
 $R_{\text{DS(on)}}$ - Drain to Source On-state Resistance - $m\Omega$

IF - Diode Forward Current - A

DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



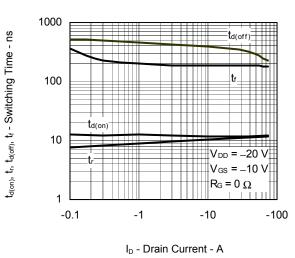
Ciss, Coss, Crss - Capacitance - pF

V_{DS} - Drain to Source Voltage - V

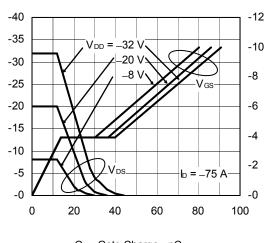
t_{rr} - Reverse Recovery Time - ns

V_{DS} - Drain to Source Voltage - V

SWITCHING CHARACTERISTICS

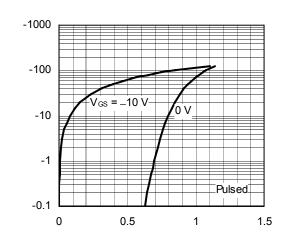


DYNAMIC INPUT/OUTPUT CHARACTERISTICS

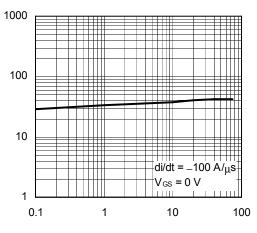


Q_G - Gate Charge - nC

SOURCE TO DRAIN DIODE FORWARD VOLTAGE



REVERSE RECOVERY TIME vs. DRAIN CURRENT

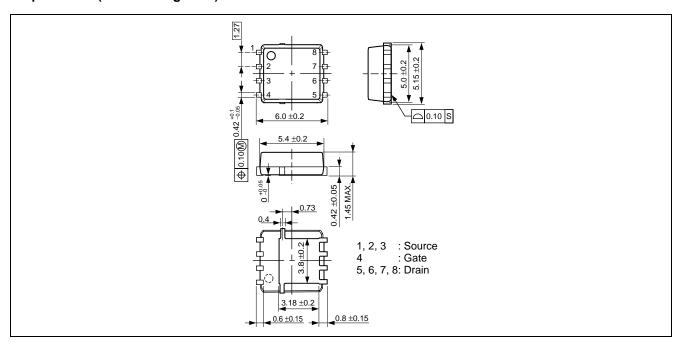


I_F - Drain Current - A

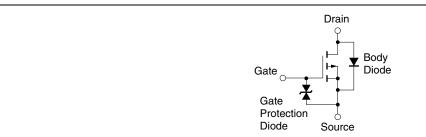
V_{GS} - Gate to Source Voltage - V

Package Drawings (Unit: mm)

8-pin HSON (Mass: 0.13 g TYP.)



Equivalent Circuit



Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

Revision History

NP75P04YLG Data Sheet

		Description		
Rev.	Date	Page	Summary	
1.00	Oct 22, 2010	-	First Edition Issued	
2.00	Mar 16, 2011	p.1	Repetitive Avalanche Current -> Single Avalanche Current	
			Repetitive Avalanche Energy -> Single Avalanche Energy	
			Modification of Note *3	

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