

N0400P

R07DS0500EJ0200 Rev.2.00 Aug 19, 2011

MOS FIELD EFFECT TRANSISTOR

Description

The N0400P is P-channel MOS Field Effect Transistor designed for high current and 2.5 V drive switching applications.

Features

- 2.5 V drive available
- Super low on-state resistance

 $R_{DS(on)1} = 40 \text{ m}\Omega \text{ MAX}. \text{ (Vgs} = -4.5 \text{ V}, I_D = -7.5 \text{ A)}$

 $R_{DS(on)2}$ = 73 m Ω MAX. (VGS = -2.5 V, ID = -3.8 A)

• Built-in gate protection diode

Ordering Information

PART NUMBER	LEAD PLATING	PACKING	PACKAGE	
N0400P-ZK-E1-AY Note	Duna Ca (Tin)	Tana 2500 m/mad	TO-252 (MP-3ZK)	
N0400P-ZK-E2-AY Note	Pure Sn (Tin)	Tape 2500 p/reel		

Note Pb-free (This product does not contain Pb in external electrode.)

Absolute Maximum Ratings (TA = 25°C)

Drain to Source Voltage (Ves = 0 V)	Voss	-40	٧
Gate to Source Voltage (V _{DS} = 0 V)	Vgss	∓12	٧
Drain Current (DC) (Tc = 25°C)	I _{D(DC)}	∓15	Α
Drain Current (pulse) Note1	D(pulse)	∓45	Α
Total Power Dissipation (Tc = 25°C)	P _{T1}	25	W
Total Power Dissipation (T _A = 25°C)	P _{T2}	1.0	W
Channel Temperature	Tch	150	°C
Storage Temperature	Tstg	-55 to +150	°C
Single Avalanche Current Note2	las	-16	Α
Single Avalanche Energy Note2	Eas	25	mJ

Notes 1. PW \leq 10 μ s, Duty Cycle \leq 1%

2. Starting T_{ch} = 25°C, V_{DD} = –20 V, R_G = 25 Ω , V_{GS} = –12 \rightarrow 0 V

Thermal Resistance

Channel to Case Thermal Resistance	Rth(ch-C)	5.0	°C/W
Channel to Ambient Thermal Resistance	Rth(ch-A)	125	°C/W

The mark <R> shows major revised points.

The revised points can be easily searched by copying an "<R>" in the PDF file and specifying it in the "Find what:" field.



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Electrical Characteristics (T_A = 25°C)

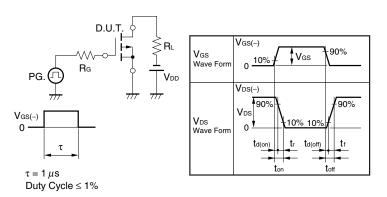
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	IDSS	V _{DS} = -40 V, V _{GS} = 0 V			-10	μΑ
Gate Leakage Current	Igss	V _{GS} = ∓12 V, V _{DS} = 0 V			∓10	μА
Gate to Source Cut-off Voltage	V _{GS(off)}	V _{DS} = -10 V, I _D = -1 mA	-0.5	-1.0	-1.5	V
Forward Transfer Admittance Note	y fs	V _{DS} = -10 V, I _D = -7.5 A	6.0			S
Drain to Source On-state Resistance Note	RDS(on)1	V _{GS} = -4.5 V, I _D = -7.5 A		31	40	mΩ
	RDS(on)2	V _{GS} = -2.5 V, I _D = -3.8 A		40	73	mΩ
Input Capacitance	Ciss	V _{DS} = -10 V,		1400		pF
Output Capacitance	Coss	V _{GS} = 0 V,		200		pF
Reverse Transfer Capacitance	Crss	f = 1 MHz		155		pF
Turn-on Delay Time	t _{d(on)}	V _{DD} = -20 V, I _D = -7.5 A,		11		ns
Rise Time	t r	V _{GS} = -4.5 V,		16		ns
Turn-off Delay Time	t _{d(off)}	R _G = 0 Ω		104		ns
Fall Time	tf			93		ns
Total Gate Charge	QG	$V_{DD} = -32 \text{ V},$		16		nC
Gate to Source Charge	Qgs	V _{GS} = -4.5 V,		3		nC
Gate to Drain Charge	Q _{GD}	I _D = -15 A		7		nC
Body Diode Forward Voltage Note	V _{F(S-D)}	I _F = -15 A, V _{GS} = 0 V		0.94	1.5	V
Reverse Recovery Time	trr	I _F = -15 A, V _{GS} = 0 V,		31		ns
Reverse Recovery Charge	Qrr	di/dt = -100 A/μs		33		nC

Note Pulsed: PW \leq 350 μ s, Duty Cycle \leq 2%

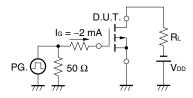
TEST CIRCUIT 1 AVALANCHE CAPABILITY

$V_{GS} = -12 \rightarrow 0 \text{ V}$ V_{DD} V_{DD}

TEST CIRCUIT 2 SWITCHING TIME

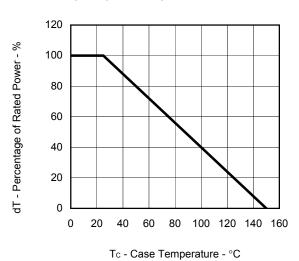


TEST CIRCUIT 3 GATE CHARGE

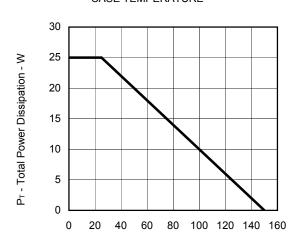


Typical Characteristics (T_A = 25°C)

DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA

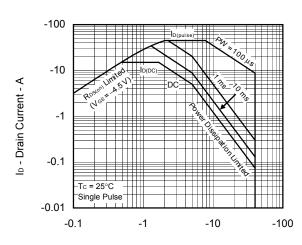


TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



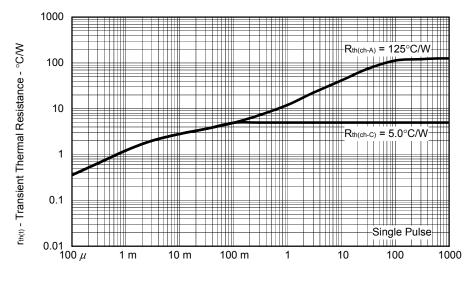
Tc - Case Temperature - °C

FORWARD BIAS SAFE OPERATING AREA



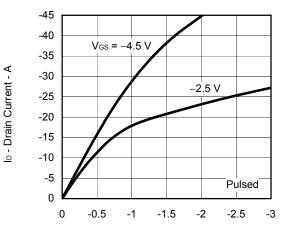
 $V_{\text{\scriptsize DS}}$ - Drain to Source Voltage - V

TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



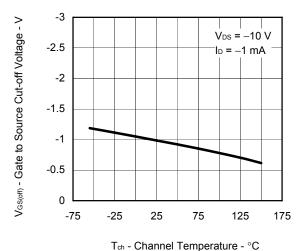
PW - Pulse Width - s

DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE

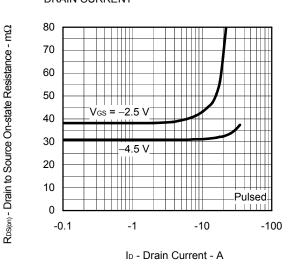


V_{DS} - Drain to Source Voltage - V

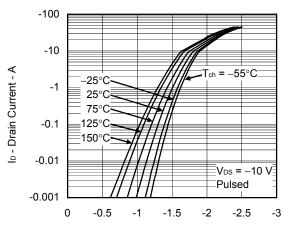
GATE TO SOURCE CUT-OFF VOLTAGE vs. CHANNEL TEMPERATURE



DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT

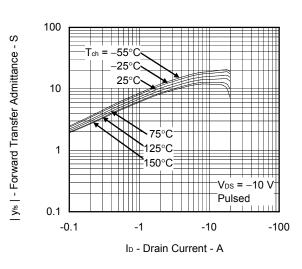


FORWARD TRANSFER CHARACTERISTICS

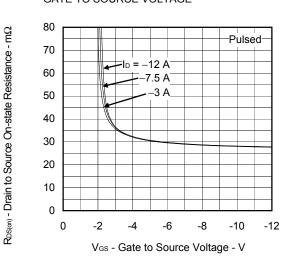


V_{GS} - Gate to Source Voltage - V

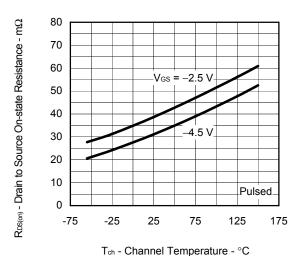
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



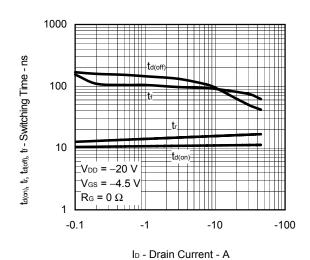
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



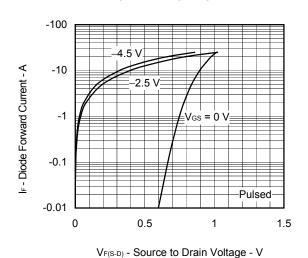
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



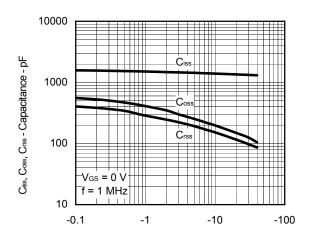
SWITCHING CHARACTERISTICS



SOURCE TO DRAIN DIODE FORWARD VOLTAGE

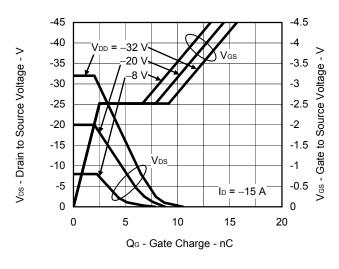


CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE

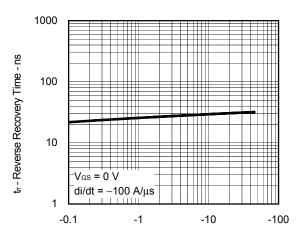


V_{DS} - Drain to Source Voltage - V

DYNAMIC INPUT/OUTPUT CHARACTERISTICS

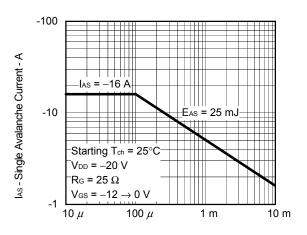


REVERSE RECOVERY TIME vs. DIODE FORWARD CURRENT



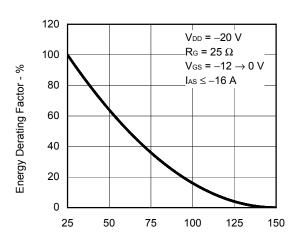
IF - Diode Forward Current - A

SINGLE AVALANCHE CURRENT vs. INDUCTIVE LOAD



L - Inductive Load - H

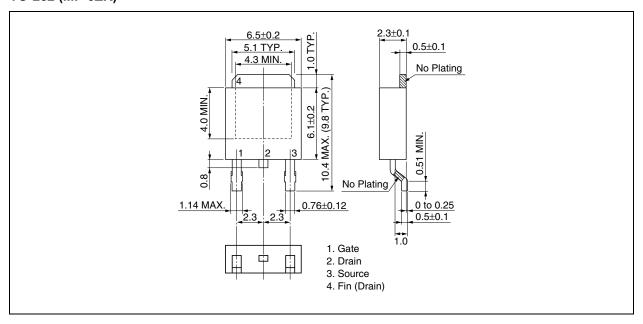
SINGLE AVALANCHE ENERGY DERATING FACTOR



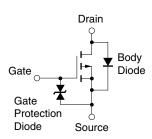
Starting T_{ch} - Starting Channel Temperature - $^{\circ}\text{C}$

Package Drawings (Unit: mm)

TO-252 (MP-3ZK)



Equivalent Circuit



Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

Revision History

N0400P Data Sheet

		Description		
Rev.	Date	Page	Summary	
_	Feb 2011	_	Previous No. : D19676EJ1V0DS00	
2.00	Aug 19, 2011	p.2	Modification of Electrical Characteristics	

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