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## Old Company Name in Catalogs and Other Documents

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April 1<sup>st</sup>, 2010  
Renesas Electronics Corporation

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# HD74HC195

## 4-bit Parallel-Access Shift Register

REJ03D0590-0200  
 (Previous ADE-205-467)  
 Rev.2.00  
 Jan 31, 2006

### Description

This shift register features parallel inputs, parallel outputs, J- $\bar{K}$  serial inputs, Shift/Load control input, and a direct overriding clear. This shift register can operate in two modes: Parallel load; shift from  $Q_A$  towards  $Q_D$ .

Parallel loading is accomplished by applying the four bits of data, and taking the Shift/Load control Input low. The data is loaded into the associated flip-flops and appears at the outputs after the positive transition of the clock input. During parallel loading, serial data flow is inhibited. Serial shifting occurs synchronously when the Shift/Load control input is high. Serial data for this mode is entered at the J- $\bar{K}$  inputs. These inputs allow the first stage to perform as a J- $\bar{K}$  or toggle flip-flop as shown in the function table.

### Features

- High Speed Operation:  $t_{pd}$  (Clock to Q) = 13 ns typ ( $C_L = 50$  pF)
- High Output Current: Fanout of 10 LSTTL Loads
- Wide Operating Voltage:  $V_{CC} = 2$  to 6 V
- Low Input Current: 1  $\mu$ A max
- Low Quiescent Supply Current:  $I_{CC}$  (static) = 4  $\mu$ A max ( $T_a = 25^\circ\text{C}$ )
- Ordering Information

Part Name	Package Type	Package Code (Previous Code)	Package Abbreviation	Taping Abbreviation (Quantity)
HD74HC195P	DILP-16 pin	PRDP0016AE-B (DP-16FV)	P	—

### Function Table

Inputs									Outputs				
Clear	Shift/Load	Clock	Serial		Parallel				$Q_A$	$Q_B$	$Q_C$	$Q_D$	$\bar{Q}_D$
			J	$\bar{K}$	A	B	C	D					
L	X	X	X	X	X	X	X	X	L	L	L	L	H
H	L	$\uparrow$	X	X	a	b	c	d	a	b	c	d	$\bar{d}$
H	H	L	X	X	X	X	X	X	$Q_{A0}$	$Q_{B0}$	$Q_{C0}$	$Q_{D0}$	$\bar{Q}_{D0}$
H	H	$\uparrow$	L	H	X	X	X	X	$Q_{A0}$	$Q_{A0}$	$Q_{Bn}$	$Q_{Cn}$	$\bar{Q}_{Cn}$
H	H	$\uparrow$	L	L	X	X	X	X	L	$Q_{An}$	$Q_{Bn}$	$Q_{Cn}$	$\bar{Q}_{Cn}$
H	H	$\uparrow$	H	H	X	X	X	X	H	$Q_{An}$	$Q_{Bn}$	$Q_{Cn}$	$\bar{Q}_{Cn}$
H	H	$\uparrow$	H	L	X	X	X	X	$Q_{An}$	$Q_{An}$	$Q_{Bn}$	$Q_{Cn}$	$\bar{Q}_{Cn}$

H : high level (steady state)

L : low level (steady state)

X : don't care

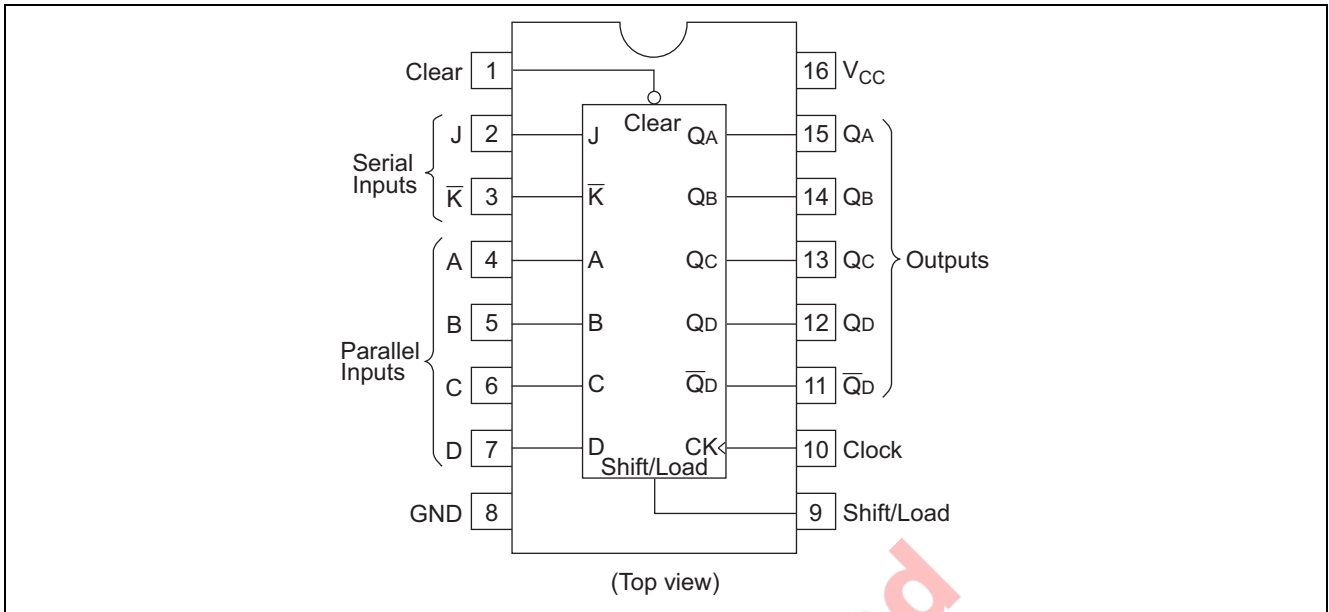
$\uparrow$  : transition from low to high level.

a, b, c, d : the level of steady-state input at inputs A, B, C or D respectively.

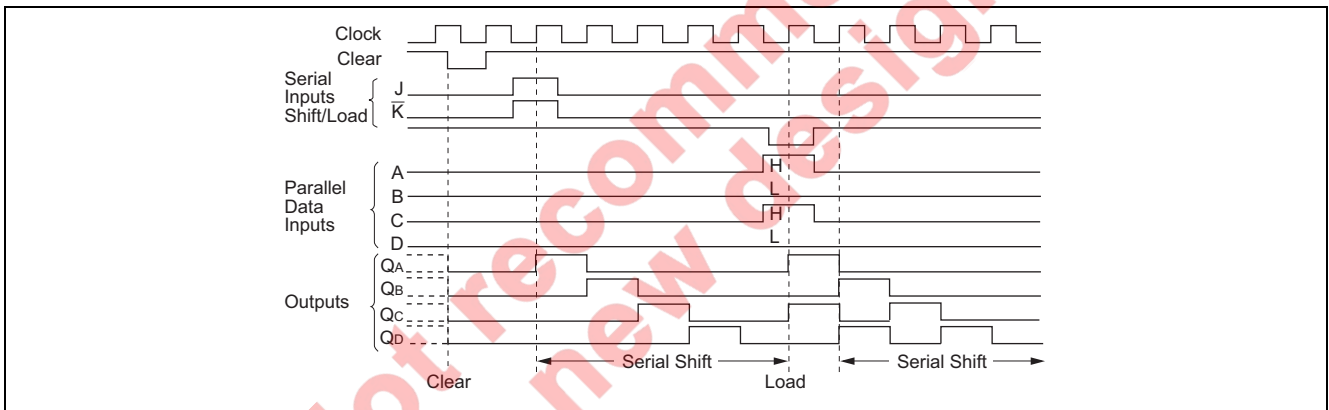
$Q_{A0}$ ,  $Q_{B0}$ ,  $Q_{C0}$ ,  $Q_{D0}$  : the level of  $Q_A$ ,  $Q_B$ ,  $Q_C$  or  $Q_D$  respectively, before the indicated steady-state input conditions were established.

$Q_{An}$ ,  $Q_{Bn}$ ,  $Q_{Cn}$ ,  $Q_{Dn}$  : the level of  $Q_A$ ,  $Q_B$ ,  $Q_C$  or  $Q_D$  respectively before the most recent  $\uparrow$  transition of the clock.

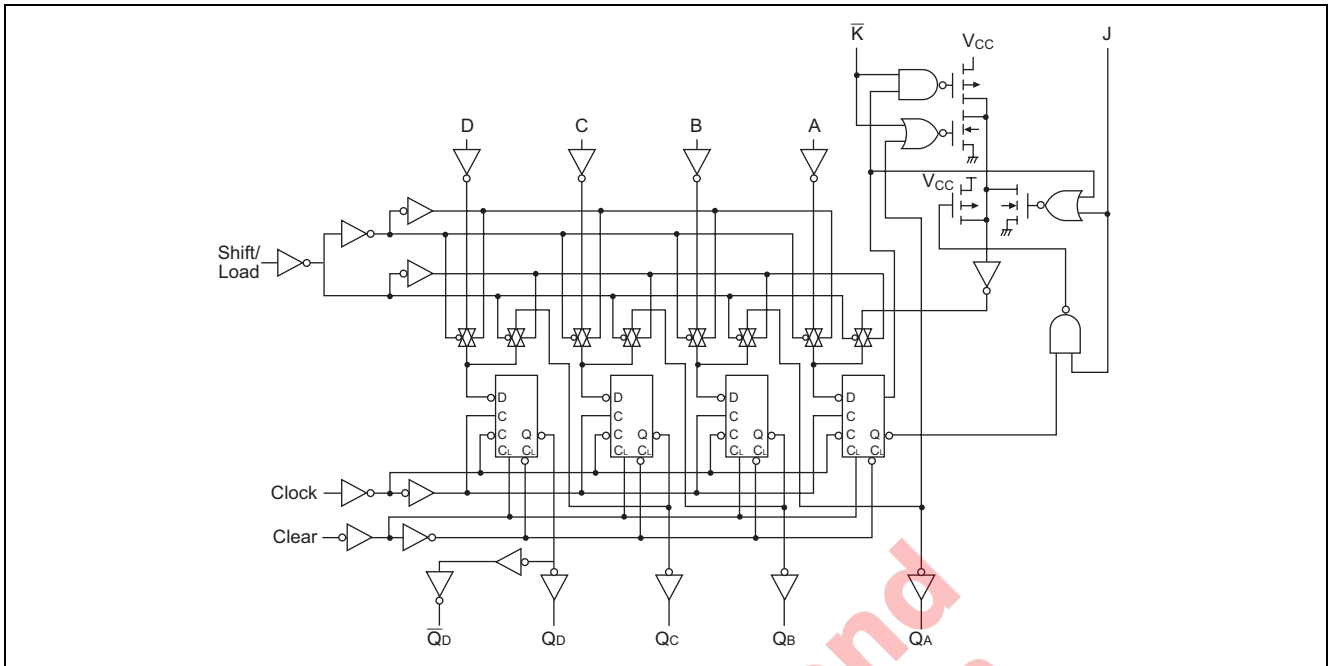
## Pin Arrangement



## Timing Diagram



Logic Diagram



Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Supply voltage range	$V_{CC}$	-0.5 to 7.0	V
Input / Output voltage	$V_{IN}, V_{OUT}$	-0.5 to $V_{CC} + 0.5$	V
Input / Output diode current	$I_{IK}, I_{OK}$	$\pm 20$	mA
Output current	$I_O$	$\pm 25$	mA
$V_{CC}, GND$ current	$I_{CC}$ or $I_{GND}$	$\pm 50$	mA
Power dissipation	$P_T$	500	mW
Storage temperature	$T_{stg}$	-65 to +150	$^{\circ}C$

Note: The absolute maximum ratings are values, which must not individually be exceeded, and furthermore, no two of which may be realized at the same time.

Recommended Operating Conditions

Item	Symbol	Ratings	Unit	Conditions
Supply voltage	$V_{CC}$	2 to 6	V	
Input / Output voltage	$V_{IN}, V_{OUT}$	0 to $V_{CC}$	V	
Operating temperature	$T_a$	-40 to 85	$^{\circ}C$	
Input rise / fall time <sup>*1</sup>	$t_r, t_f$	0 to 1000	ns	$V_{CC} = 2.0 V$
		0 to 500		$V_{CC} = 4.5 V$
		0 to 400		$V_{CC} = 6.0 V$

Notes: 1. This item guarantees maximum limit when one input switches.  
Waveform: Refer to test circuit of switching characteristics.

## Electrical Characteristics

Item	Symbol	V <sub>CC</sub> (V)	Ta = 25 °C			Ta = -40 to+85 °C		Unit	Test Conditions		
			Min	Typ	Max	Min	Max				
Input voltage	V <sub>IH</sub>	2.0	1.5	—	—	1.5	—	V			
		4.5	3.15	—	—	3.15	—				
		6.0	4.2	—	—	4.2	—				
	V <sub>IL</sub>	2.0	—	—	0.5	—	0.5	V			
		4.5	—	—	1.35	—	1.35				
		6.0	—	—	1.8	—	1.8				
Output voltage	V <sub>OH</sub>	2.0	1.9	2.0	—	1.9	—	V	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = -20 μA	
		4.5	4.4	4.5	—	4.4	—			I <sub>OH</sub> = -4 mA	
		6.0	5.9	6.0	—	5.9	—			I <sub>OH</sub> = -5.2 mA	
		4.5	4.18	—	—	4.13	—				
		6.0	5.68	—	—	5.63	—				
	V <sub>OL</sub>	2.0	—	0.0	0.1	—	0.1	V	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OL</sub> = 20 μA	
		4.5	—	0.0	0.1	—	0.1				
		6.0	—	0.0	0.1	—	0.1				
		4.5	—	—	0.26	—	0.33				I <sub>OL</sub> = 4 mA
		6.0	—	—	0.26	—	0.33				I <sub>OL</sub> = 5.2 mA
Input current	I <sub>in</sub>	6.0	—	—	±0.1	—	±1.0	μA	V <sub>in</sub> = V <sub>CC</sub> or GND		
Quiescent supply current	I <sub>CC</sub>	6.0	—	—	4.0	—	40	μA	V <sub>in</sub> = V <sub>CC</sub> or GND, I <sub>out</sub> = 0 μA		

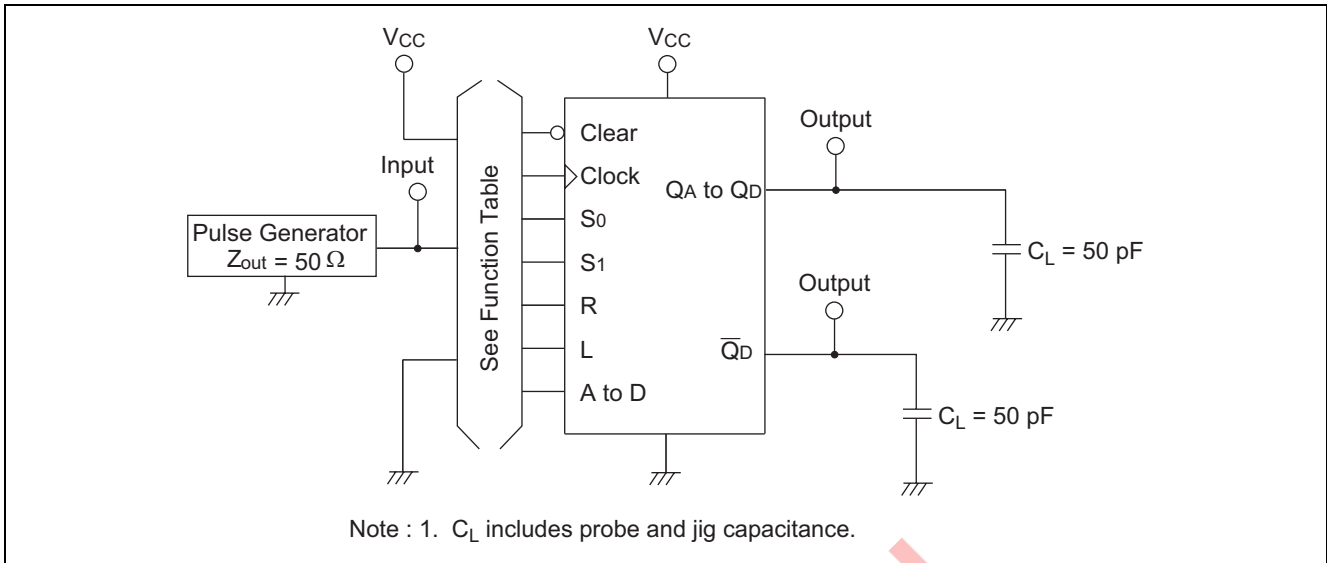
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## Switching Characteristics

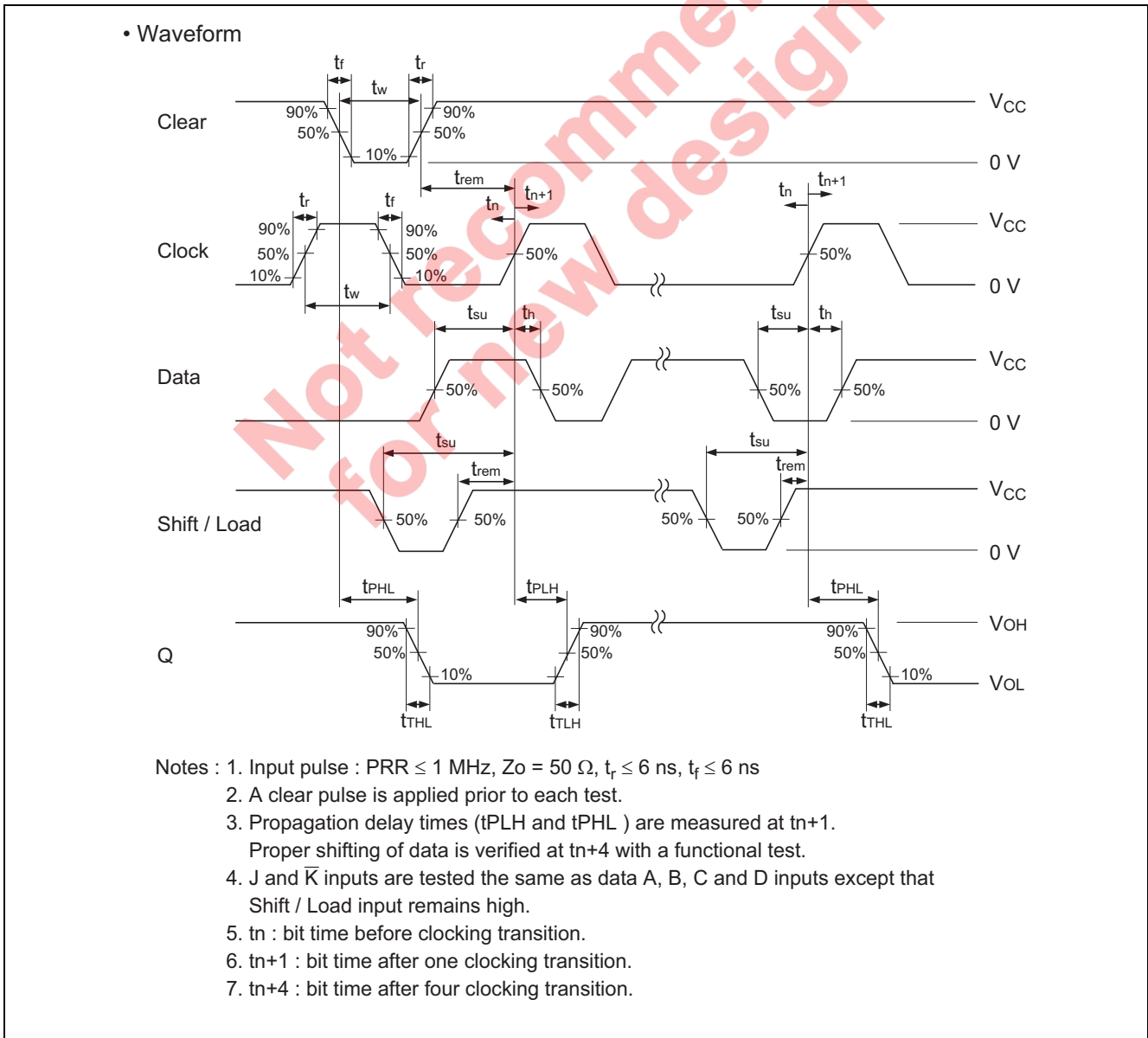
(C<sub>L</sub> = 50 pF, Input t<sub>r</sub> = t<sub>f</sub> = 6 ns)

Item	Symbol	V <sub>CC</sub> (V)	Ta = 25°C			Ta = -40 to +85°C		Unit	Test Conditions
			Min	Typ	Max	Min	Max		
Maximum clock frequency	f <sub>max</sub>	2.0	—	—	6	—	5	MHz	
		4.5	—	—	30	—	24		
		6.0	—	—	35	—	28		
Propagation delay time	t <sub>PHL</sub>	2.0	—	—	140	—	175	ns	Clock to Q
		4.5	—	13	28	—	35		
		6.0	—	—	24	—	30		
	t <sub>PLH</sub>	2.0	—	—	140	—	175	ns	
		4.5	—	13	28	—	35		
		6.0	—	—	24	—	30		
	t <sub>PHL</sub>	2.0	—	—	150	—	190	ns	Clear to Q
		4.5	—	15	30	—	38		
		6.0	—	—	26	—	33		
Pulse width	t <sub>w</sub>	2.0	80	—	—	100	—	ns	Clock to Clear
		4.5	16	7	—	20	—		
		6.0	14	—	—	17	—		
Setup time	t <sub>su</sub>	2.0	100	—	—	125	—	ns	A, B, C, D, J, $\bar{K}$ to Clock
		4.5	20	6	—	25	—		
		6.0	17	—	—	21	—		
	t <sub>sh</sub>	2.0	100	—	—	125	—	ns	Shift/Load to Clock
		4.5	20	13	—	25	—		
		6.0	17	—	—	21	—		
Hold time	t <sub>h</sub>	2.0	0	—	—	0	—	ns	Any input except Shift/Load
		4.5	0	-3	—	0	—		
		6.0	0	—	—	0	—		
Removal time	t <sub>rem</sub>	2.0	75	—	—	95	—	ns	Shift/Load to Clock
		4.5	15	8	—	19	—		
		6.0	13	—	—	16	—		
	t <sub>rem</sub>	2.0	25	—	—	31	—	ns	Clear inactive to Clock
		4.5	5	0	—	6	—		
		6.0	4	—	—	5	—		
Output rise/fall time	t <sub>TLH</sub>	2.0	—	—	75	—	95	ns	
	t <sub>THL</sub>	4.5	—	5	15	—	19		
	6.0	—	—	13	—	16			
Input capacitance	C <sub>in</sub>	—	—	5	10	—	10	pF	

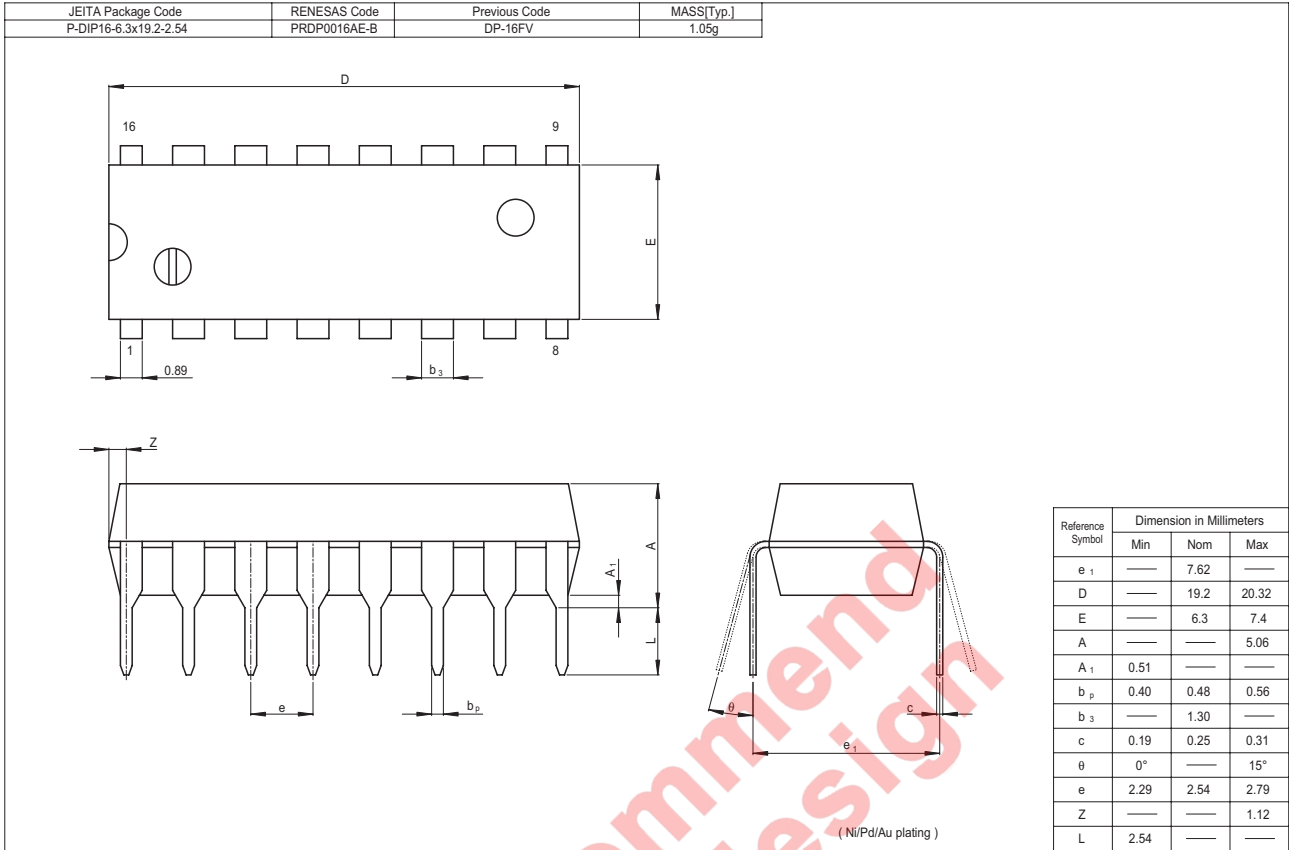
Test Circuit



Waveforms



Package Dimensions



Not recommended for new design

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