Freescale Semiconductor

Technical Data

MC14578 Rev 2, 05/2005

Archive Information

CMOS Micro-Power Comparator plus Voltage Follower

The MC14578 is an analog building block consisting of a very-high input impedance comparator. The voltage follower allows monitoring the noninverting input of the comparator without loading.

Four enhancement-mode MOSFETs are also included on chip. These FETs can be externally configured as open-drain or totem-pole outputs. The drains have on-chip static-protecting diodes. Therefore, the output voltage must be maintained between $V_{\rm SS}$ and $V_{\rm DD}$.

The chip requires one external component. A 3.9 M Ω ±10% resistor must be connected from the R_{bias} pin to V_{DD}. This circuit is designed to operate in smoke detector systems that comply with UL217 and UL268 specifications.

Features

Applications:

Pulse Shapers Line-Powered Smoke Detectors

Threshold Detectors Liquid/Moisture Sensors

Low-Battery Detectors CO Detector and Micro Interface

Operating Voltage Range: 3.5 to 14 V

Operating Temperature Range: -30° to 70°C

Input Current (IN + Pin): ±1 pA @ 25°C (DIP Only)

Quiescent Current: 10 μA @ 25°C

Electrostatic Discharge (ESD) Protection Circuitry on All Pins

ORDERING INFORMATION				
Device Temperature Range		Case No.	Package	
MC14578P	-30° to 70°C	648-08	Plastic Dip	

MC14578

CMOS
MICRO-POWER COMPARATOR
PLUS VOLTAGE FOLLOWER



P SUFFIX PLASTIC DIP CASE 648-08

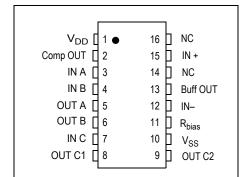


Figure 1. Pin Connections



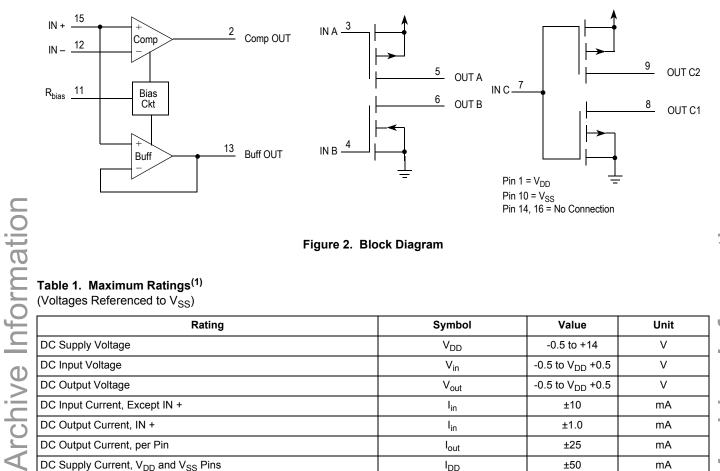


Figure 2. Block Diagram

Table 1. Maximum Ratings⁽¹⁾ (Voltages Referenced to V_{SS})

Symbol	Value	Unit
V_{DD}	-0.5 to +14	V
V _{in}	-0.5 to V _{DD} +0.5	V
V _{out}	-0.5 to V _{DD} +0.5	V
I _{in}	±10	mA
I _{in}	±1.0	mA
l _{out}	±25	mA
I _{DD}	±50	mA
P _D	500	mW
T _{stg}	-65 to + 150	°C
T _L	260	°C
	V _{DD} V _{in} V _{out} I _{in} I _{out} I _{DD} P _D T _{stg}	$\begin{array}{cccccccccccccccccccccccccccccccccccc$

^{1.} Maximum Ratings are those values beyond which damage to the device may occur. This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \le (V_{in} \text{ or } V_{out}) \le V_{DD}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left

Table 2. Electrical Characteristics

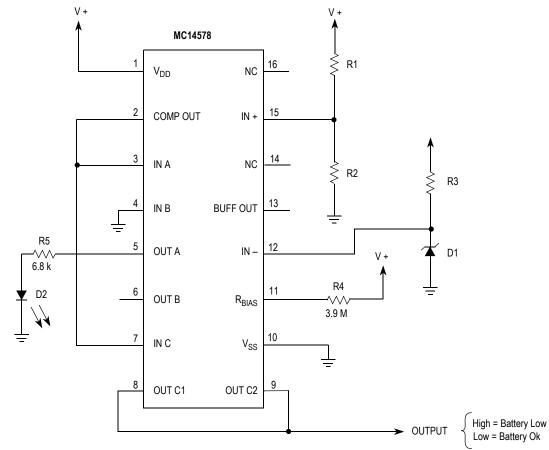
(Voltages Referenced to V_{SS}, R_{bias} = 3.9 M Ω to V_{DD}, T_A = -30 $^{\circ}$ to 70 $^{\circ}$ C Unless Otherwise Indicated)

Characteristic	Symbol	Test Condition	V _{DD} V _{DC}	Guaranteed Limit	Unit	
Power Supply Voltage Range	V_{DD}		_	3.5 to 14.0	V	
Maximum Low-Level Input Voltage, MOSFETs Wired as Inverters; i.e., IN A tied to IN B, OUT A to OUT B, OUT C1 to OUT C2	V _{IL}	V_{out} = 9.0 V, $II_{out}I$ <1 μ A	10.0	2.0	V	
Minimum High-Level Input voltage, MOSFETs Wired as Inverters; i.e., IN A tied to IN B, OUT A to OUT B, OUT C1 to OUT C2	V _{IH}	V _{out} = 1.0 V, II _{out} I <1 μA	10.0	8.0	V	
Comparator Input Offset Voltage	V _{IO}	T _A = 25°C, Over Common Mode Range	10.0	±50	mV	
		T _A = 0° to 50°C, Over Common Mode Range	3.5 to 14.0	±75		
Comparator Common Mode Voltage Range	V _{CM}		3.5 to 14.0	0.7 to V _{DD} – 1.5	V	
Maximum Low-Level Comparator Output Voltage	V _{OL}	$\begin{aligned} &\text{IN +: V}_{\text{in}} = \text{V}_{\text{SS}}, \text{IN -: V}_{\text{in}} = \text{V}_{\text{DD}}, \\ &\text{I}_{\text{out}} = 30 \mu\text{A} \end{aligned}$	10.0	0.5	V	
Minimum High-Level Comparator Output Voltage	V _{OH}	$\begin{aligned} &\text{IN +: V}_{in} = \text{V}_{DD}, \text{ IN -: V}_{in} = \text{V}_{SS}, \\ &\text{I}_{out} = -30 \mu\text{A} \end{aligned}$	10.0	9.5	V	
Buffer Amp Output Offset Voltage	V _{oo}	R_{load} = 10 M Ω to V_{DD} or V_{SS} , Over Common Mode Range	_	±100	mV	
Maximum Low-Level Input Voltage, MOSFETs	V _{OL}	OUT C1, OUT C2, I _{out} = 1.1 mA	10.0	0.5	V	
Wired as Inverters; i.e., IN A tied to IN B, OUT A to OUT B, OUT C1 to OUT C2		OUT A, OUT B, I _{out} = 270 μA	10.0	0.5	V	
Minimum High-Level Input Voltage, MOSFETs	V _{OH}	OUT C1, OUT C2, I _{out} = -1.1 mA	10.0	9.5	V	
Wired as Inverters; i.e., IN A tied to IN B, OUT A to OUT B, OUT C1 to OUT C2		OUT A, OUT B, I _{out} = 270 μA	10.0	9.5	V	
Maximum Input Leakage IN + (DIP Only) Current	I _{in}	T _A = 25°C, 40% R.H., V _{in} = V _{SS} or V _{DD}	10.0	±1.0	рA	
IN + (DIP Only)		$T_A = 50$ °C, $V_{in} = V_{SS}$ or V_{DD}	10.0	±6.0		
IN + (SOG), IN A, IN B, IN C, IN –		$V_{in} = V_{SS}$ or V_{DD}	10.0	±40	nA	
Maximum Off-State MOSFET Leakage Current	I _{OZ}	IN A, IN C: V _{in} = V _{DD} , OUT A, OUT C2: V _{out} = V _{SS} or V _{DD}	10.0	±100	nA	
		IN B, IN C: V _{in} = V _{SS} , OUT B, OUT C1: V _{out} = V _{SS} or V _{DD}	10.0	±100		
Maximum Quiescent Current	I _{DD}	$\begin{split} T_A &= 25^{\circ}C\\ \text{IN A, IN B, IN C: V}_{\text{in}} &= \text{V}_{\text{SS}} \text{ or V}_{\text{DD}},\\ \text{IV}_{\text{IN}} &+ -\text{V}_{\text{IN}} - \text{I} = 100 \text{ mV}\\ \text{I}_{\text{out}} &= 0 \mu\text{A} \end{split}$	10.0	10	μА	
Maximum Input Capacitance IN + Other Inputs	C _{in}	f = 1 kHz	_	5.0 15	pF	

Low-battery

Indicator

APPLICATIONS INFORMATION



NOTE: IN + and IN - have very high input impedance. Interconnect to these pins should be as short as possible.

Figure 3. Low-Battery Detector

EXAMPLE VALUES

Near the switchpoint, the comparator output in the circuit of Figure 3. may chatter or oscillate. This oscillation appears on the signal labelled OUTPUT. In some cases, the oscillation in the transition region will not cause problems. For example, an MPU reading OUTPUT could sample the signal two or three times to ensure a solid level is attained. But, in a low battery detector, this probably is not necessary.

To eliminate comparator chatter, hysteresis can be added as shown in Figure 4. The circuit of Figure 4. requires slightly more operating current than the Figure 3. arrangement.

R1	R2	R3	Nominal Tip Point
470 kΩ	1.3 MΩ	20 kΩ	4.08 V
820 kΩ	1.2 MΩ	39 kΩ	5.05 V
1.2 MΩ	1.2 MΩ	62 kΩ	6.00 V

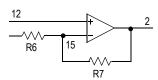
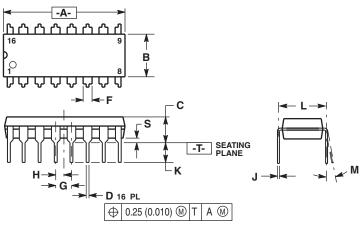


Figure 4. Adding Hysteresis

Archive Information

PACKAGE DIMENSIONS



STYLE 1:		STYLE 2:	
PIN 1.	CATHODE	PIN 1.	COMMON DF
2.	CATHODE	2.	COMMON DF
3.	CATHODE	3.	COMMON DF
	CATHODE		COMMON DF
	ANODE		GATE
	ANODE		SOURCE
	ANODE		GATE
	ANODE		SOURCE
	ANODE		GATE
	ANODE		SOURCE
	ANODE		GATE
16	ANODE	16	SOURCE

CASE 648-08 ISSUE R 16-LEAD PLASTIC DIP

- DIMENSIONING AND TOLERANCING PER ANSI DIMENSIONING AND TOLEHANGING PEH AN Y14.5M, 1982. CONTROLLING DIMENSION: INCH. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
- 4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
 5. ROUNDED CORNERS OPTIONAL.

	INC	HES	MILLIM	ETERS	
DIM	MIN	MAX	MIN	MAX	
Α	0.740	0.770	18.80	19.55	
В	0.250	0.270	6.35	6.85	
С	0.145	0.175	3.69	4.44	
D	0.015	0.021	0.39	0.53	
F	0.040	0.70	1.02	1.77	
G	0.100	BSC	2.54 BSC		
Н	0.050	BSC	1.27	BSC	
J	0.008	0.015	0.21	0.38	
K	0.110	0.130	2.80	3.30	
L	0.295	0.305	7.50	7.74	
M	0	10	0	10	
S	0.020	0.040	0.51	1.01	

NOTES

NOTES

How to Reach Us:

Home Page:

www.freescale.com

support@freescale.com

USA/Europe or Locations Not Listed:

Freescale Semiconductor Technical Information Center, CH370 1300 N. Alma School Road Chandler, Arizona 85224 +1-800-521-6274 or +1-480-768-2130 support@freescale.com

Europe, Middle East, and Africa: Freescale Halbleiter Deutschland GmbH **Technical Information Center** Schatzbogen 7 81829 Muenchen, Germany +44 1296 380 456 (English) +46 8 52200080 (English) +49 89 92103 559 (German) +33 1 69 35 48 48 (French) support@freescale.com

Freescale Semiconductor Japan Ltd. Headquarters ARCO Tower 15F 1-8-1, Shimo-Meguro, Meguro-ku, Tokyo 153-0064 Japan 0120 191014 or +81 3 5437 9125 support.japan@freescale.com

Asia/Pacific:

Freescale Semiconductor Hong Kong Ltd. **Technical Information Center** 2 Dai King Street
Tai Po Industrial Estate Tai Po, N.T., Hong Kong +800 2666 8080 support.asia@freescale.com

For Literature Requests Only:

Freescale Semiconductor Literature Distribution Center P.O. Box 5405 Denver, Colorado 80217 1-800-441-2447 or 303-675-2140 Fax: 303-675-2150 LDCForFreescaleSemiconductor@hibbertgroup.com

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