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April 1st, 2010
Renesas Electronics Corporation

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HA16129AFPJ

Single Watchdog Timer

REJ03F0143-0100
(Previous: ADE-204-067)
Rev.1.00
Jun 15, 2005

Description

The HA16129AFPJ is a watchdog timer IC that monitors a microprocessor for runaway. In addition to the watchdog timer function, the HA16129AFPJ also provides a function for supplying a high-precision stabilized power supply to the microprocessor, a power on reset function, a power supply voltage monitoring function, and a fail-safe function that masks the microprocessor outputs if a runaway is detected.

Functions

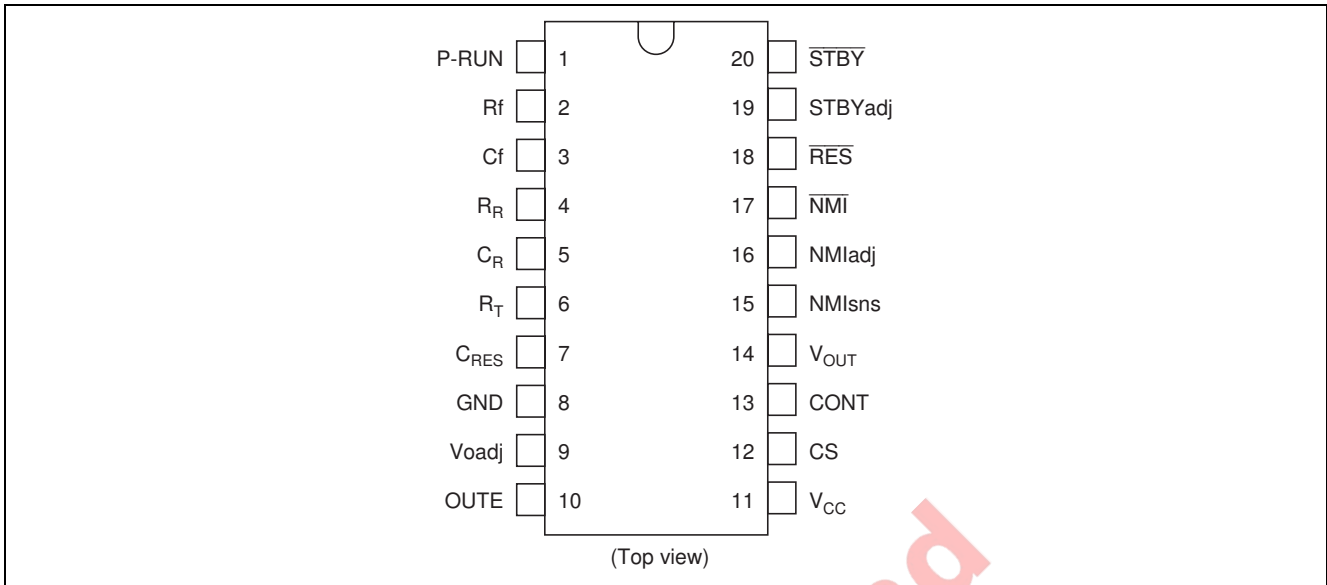
- Watchdog timer (WDT) function
Monitors the P-RUN signal output by the microprocessor, and issues an auto-reset (RES) signal if a microprocessor runaway is detected.
- Stabilized power supply
Provides power to the microprocessor.
- Power on and clock off functions
The power on function outputs a low level signal to the microprocessor for a fixed period when power is first applied.
The clock off function outputs a $\overline{\text{RES}}$ signal to the microprocessor a fixed period after a runaway occurs.
- Power supply monitoring function
When the reference voltage (V_{out}) falls and becomes lower than the $\overline{\text{NMI}}$ detection voltage (4.63 V, Typ) or the $\overline{\text{STBY}}$ detection voltage (3.0 V Typ), this function outputs either an $\overline{\text{NMI}}$ signal or an $\overline{\text{STBY}}$ signal, respectively. Note that NMI detection can be set to monitor either V_{CC} or V_{out} .
- OUTE function*¹ (fail-safe function)
Outputs a signal used to mask microprocessor outputs when a microprocessor runaway has been detected.
- $\overline{\text{RES}}$ delay function
Sets the delay between the time the $\overline{\text{NMI}}$ signal is output and the time the $\overline{\text{RES}}$ signal is output.
- Protection functions
- The HA16129AFPJ incorporates both V_{out} overvoltage prevention and short detection functions.

Note: 1. OUTE function: OUTE is an abbreviation for output enable.

Features

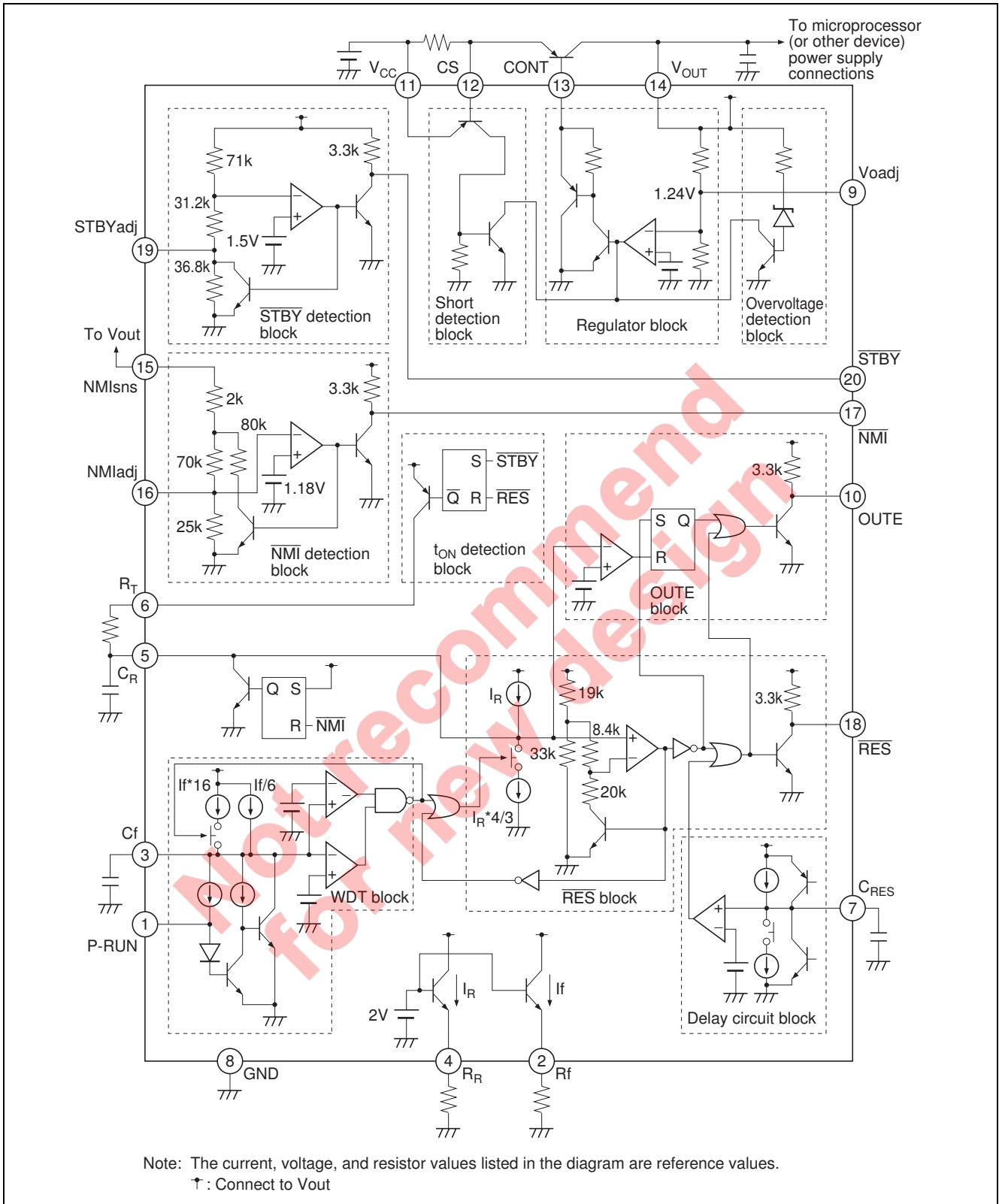
- High-precision output voltage: 5.0 V \pm 1.5%
- The WDT supports both frequency and duty detection schemes.
- High-precision power supply monitoring function: 4.625 V \pm 0.125 V
- Built-in OUTE function
- All functions can be adjusted with external resistors and/or capacitors.

Pin Arrangement



Not recommended for new design

Block Diagram



Pin Function

Related Function	Pin No.	Symbol	Function
WDT.	1	P-RUN	Watchdog timer pulse input. The auto-reset function is controlled by the duty cycle or frequency of this input pulse signal.
	2	Rf	The resistor connected to this pin determines the current that flows in the Cf pin capacitor. Use the resistor value from 100 kΩ to 500 kΩ
	3	Cf	The current determined by the Rf pin charges the Cf capacitor and the potential on this pin determines the watchdog timer frequency band.
t_{RH} , t_{RL} , t_{OFF}	4	R _R	The resistor connected to this pin determines the current that flows in the C _R pin capacitor. Use the resistor value from 100 kΩ to 500 kΩ
	5	C _R	The current determined by the R _R pin charges the capacitor C _R and the potential on this pin controls the \overline{RES} function (t_{off} , t_{RH} , and t_{RL}).
t_{ON}	6	R _T	The resistor R _T , which determines only the time t_{ON} for the \overline{RES} function is connected to this pin. This resistor determines the current that charges the capacitor C _R for the time t_{ON} . Use the resistor value from 100 kΩ to 500 kΩ
t_r , t_{RES}	7	C _{RES}	The current determined by the Rf pin charges the capacitor C _{RES} , and the \overline{RES} delay times (T_r and T_{RES}) are determined by the potential of this capacitor.
–	8	GND	Ground
Vout	9	Voadj	Insert the resistor Roadj if fine adjustment of the regulator output voltage Vout is required. Leave this pin open if Vout does not need to be changed.
Output	10	OUTE	Output for the OUTE function
Power supply	11	V _{CC}	Power supply
Short detection	12	CS	Connect the overcurrent detection resistor between the CS pin and the V _{CC} pin. If this function is not used, short this pin to V _{CC} . Also, connect this pin to the emitter of the external transistor.
Vout	13	CONT	Connect this pin to the base of the external transistor.
	14	V _{OUT}	Provides the regulator output voltage and the IC internal power supply. Connect this pin to the collector of the external transistor.
\overline{NMI}	15	NMI _{sns}	This pin senses the \overline{NMI} detection voltage. If V _{CC} is to be detected, connect this pin to the V _{CC} pin (however, note that an external resistor is required), and if Vout is to be detected, connect this pin to the V _{OUT} pin.
	16	NMI _{adj}	Insert a resistor if fine adjustment of the \overline{NMI} detection voltage is required. Leave this pin open if fine adjustment is not required.
Output	17	\overline{NMI}	\overline{NMI} output
Output	18	\overline{RES}	\overline{RES} output
\overline{STBY}	19	STBY _{adj}	Insert a resistor if fine adjustment of the \overline{STBY} detection voltage is required. Leave this pin open if fine adjustment is not required.
Output	20	\overline{STBY}	\overline{STBY} output

Functional Description

This section describes the functions provided by the HA16129FPJ. See the section on formulas for details on adjustment methods.

Regulator Block

- Vout Voltage

This IC provides a stabilized 5 V power supply by controlling the base current of an external transistor. The largest current (the maximum CONT pin current) that can be drawn by the base of this external transistor is 20 mA. Also note that the Vout output is also used for the power supply for this IC's internal circuits.

Short Detection Block

When a current detection resistor (R_{CS}) is connected between the V_{CC} pin and the CS pin, and the voltage between these pins exceeds the V_{CS} voltage (700 mV Typ), the CONT pin function turns off and the output voltage supply is stopped.

Output Voltage (Vout) Adjustment

The output voltage can be adjusted by connecting an external resistor at the output voltage adjustment pin (Voadj). However, if for some reason the voltage on this Vout line increases and exceeds the voltage adjustment range (7 V Max), the CONT pin function turns off and the output voltage supply is stopped.

Refer to the timing charts in conjunction with the following items.

LVI (Low Voltage Inhibit)

- \overline{NMI} Detection Voltage

This function monitors for drops in the power-supply voltage. This function can be set up to monitor either V_{CC} or Vout. When Vout is monitored, a low level is output from the \overline{NMI} pin if that voltage falls under the detection voltage (4.63 V Typ). Then, when the power-supply voltage that fell rises again, the \overline{NMI} pin will output a high level. Note that this function has a fixed hysteresis of 50 mV (Typ). The monitored power supply is selected by connecting the \overline{NMI} pin either to the V_{CC} pin or to the V_{OUT} pin. When detecting V_{CC} , an external adjustment resistor is required.)

The detection voltage can also be adjusted with the \overline{NMI} adj pin.

- \overline{STBY} Detection Voltage

This function monitors for drops in the Vout voltage. It monitors the Vout voltage, and outputs a low level from the \overline{STBY} pin if that voltage drops below the detection voltage (3.0 V Typ). Then, when the power-supply voltage that fell rises again, the \overline{STBY} pin will output a high level. Note that this function has a fixed hysteresis of 1.35 V (Typ). The detection voltage can also be adjusted with the \overline{STBY} adj pin.

Function Start Voltage

This is the minimum required Vout voltage for the \overline{RES} , \overline{NMI} , \overline{STBY} , and OUTE output pin functions to start operating. It is stipulated as the voltage that Vout must reach after power is first applied for these pins to output a low level.

Hysteresis

This is the difference between the LVI function detection voltage when the power-supply voltage drops, and the clear (reset) voltage when the power-supply voltage rises.

$$(V_{HYSN} = V_{\overline{NMI}'} - V_{\overline{NMI}}; V_{HYSS} = V_{\overline{STBY}'} - V_{\overline{STBY}})$$

OUTE Function

When a microprocessor is in the runaway state, its outputs are undefined, and thus it is possible that the outputs may be driven by incorrect signals. This function is used to mask such incorrect microprocessor outputs. When the WDT function recognizes normal operation (when the $\overline{\text{RES}}$ output is high), the OUTE output will be held high. When the WDT function recognizes an abnormal state and an auto-reset pulse is output from the $\overline{\text{RES}}$ pin, the OUTE output will be held low. Thus microprocessor outputs during microprocessor runaway can be masked by taking the AND of those outputs and this signal using external AND gates.

The OUTE output will go high when the C_R pin voltage exceeds V_{thHcr2} , and will go low when that voltage falls below V_{thLcr} .

There are limitation that apply when the OUTE function is used. Refer to the calculation formulas item for details.

RES Function

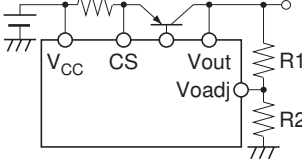
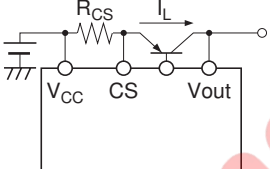
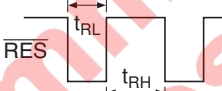
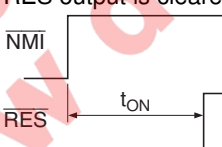
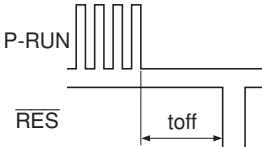
- t_{RH}
This period is the length of the high-level output period of the $\overline{\text{RES}}$ pulse when the P-RUN signal from the microprocessor stops. This is the time required for the C_R potential to reach V_{thLcr} from V_{thHcr1} .
- t_{RL}
This period is the length of the low-level output period of the $\overline{\text{RES}}$ pulse when the P-RUN signal from the microprocessor stops. This is the time required for the C_R potential to reach V_{thHcr1} from V_{thLcr} .
- t_{OFF}
This is the time from the point the P-RUN signal from the microprocessor stops to the point a low level is output from the $\overline{\text{RES}}$ pin. During normal microprocessor operation, the potential on the C_R pin will be about $V_{out} - 0.2 \text{ V}$ (although this value may change with the P-RUN signal input conditions, so it should be verified in the actual application circuit) and t_{OFF} is the time for the C_R pin potential to reach V_{thLcr} from that potential.
- t_{ON}
 t_{ON} is the time from the point the $\overline{\text{NMI}}$ output goes high when power is first applied to the point the $\overline{\text{RES}}$ output goes low. t_{ON} is the time for the potential of the C_R pin to reach V_{thHcr1} from 0 V.
- t_r
The time t_r is the fixed delay time between the point the $\overline{\text{NMI}}$ output goes from low to high after the power-supply voltage comes up to the point $\overline{\text{RES}}$ goes from low to high. The time t_r is the time for the C_{RES} pin potential to fall from the high voltage (about 1.9 V) to V_{thres} .
- t_{RES}
The time t_{RES} is the fixed delay time between the point the $\overline{\text{NMI}}$ output goes from high to low when the power-supply voltage falls to the point $\overline{\text{RES}}$ goes from high to low. The time t_{RES} is the time for the C_{RES} pin potential to rise from 0 V to V_{thres} .

WDT Function

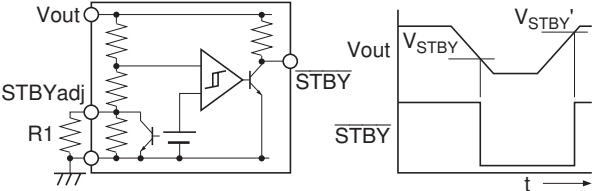
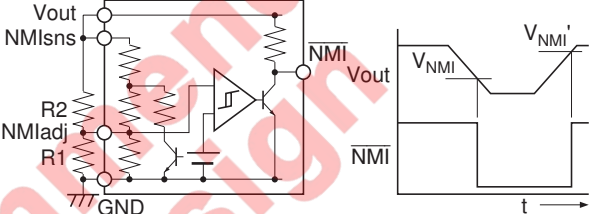
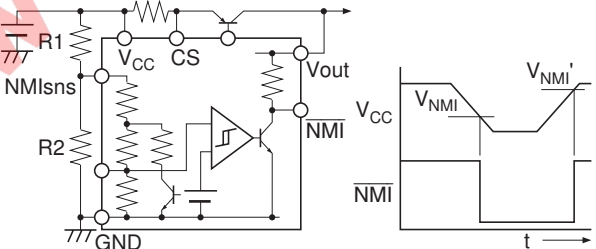
This function determines whether the microprocessor is operating normally or has entered a runaway state by monitoring the duty or frequency of the P-RUN signal. When this function recognizes a runaway state, it outputs a reset pulse from the $\overline{\text{RES}}$ pin and sets the OUTE pin to low from high. It holds the $\overline{\text{RES}}$ and OUTE pins fixed at high as long as it recognizes normal microprocessor operation.

In this function, the potential of the C_f capacitor is controlled by the P-RUN signal. This C_f pin potential charges the capacitor C_R that controls the reset pulse to be between V_{thLcf} and V_{thHcf} . The judgment as to whether or not the microprocessor is operating normally, is determined by the balance between the charge and discharge voltage on the capacitor C_R at this time.

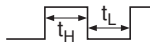
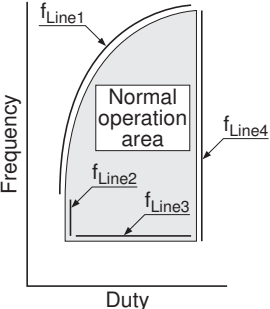
Calculation Formulas

Item	Formula	Notes
Reference voltage	$V_{out} = 1.225 \left(1 + \frac{37 \parallel R1}{12 \parallel R2} \right)$ R1, R2; kΩ	While the Vout voltage will be 5 V ±1.5% when the Voadj pin is open, the circuit shown here should be used to change the Vout voltage externally. 
Short detection voltage	$V_{CS} (700 \text{ mV Typ}) < I_L \cdot R_{CS}$	When this function operates, the base current to the external transistor connected to the CS pin stops and the Vout output is lowered. 
OVP	-	This function prevents the microprocessor from being damaged if the Vout voltage is inadvertently increased to too high a level. The OVP detection voltage is fixed.
t _{RH} , t _{RL}	$t_{RH} = 3.3 \times C_R \cdot R_R$ $t_{RL} = 1.1 \times C_R \cdot R_R$	These determine the reset pulse frequency and duty. 
t _{ON}	$t_{ON} = 1.1 \times C_R \cdot R_T$	Sets the time from the rise of the NMI signal to the point the RES output is cleared. 
t _{OFF}	$t_{OFF} = 6.5 \times C_R \cdot R_R$	Sets the time from the point the P-RUN pulse stops to the point a reset pulse is output. 

Calculation Formulas (cont.)

Item	Formula	Notes
V_{STBY}	$V_{STBY} = 1.48 \times \left(\frac{67.6}{29.5 + 36.2 // R1} + 1 \right)$	<p>The voltage at which the \overline{STBY} signal is output when V_{out} falls. The \overline{STBY} detection voltage can be adjusted by connecting a resistor between the $STBY_{adj}$ pin and ground (R3). However, the \overline{STBY} recovery voltage cannot be adjusted.</p> 
V_{NMI} (V_{out} detection)	$V_{NMI} = 1.2 \times \left(1 + \frac{R1 // 73}{R2 // 25} \right)$ <p>R1, R2; kΩ</p>	<p>The voltage at which the \overline{NMI} signal is output when V_{out} falls. (When NMI_{sns} is connected to V_{out}.)</p> <p>The \overline{NMI} detection voltage can be adjusted by connecting resistors between the NMI_{adj} pin and V_{out} (R1), and between the NMI_{adj} pin and ground (R2).</p> 
V_{NMI} (V_{CC} detection)	$V_{NMI} = 4.62 \times \left(\frac{R1}{R2 // 97.1} + 1 \right)$ <p>Recovery voltage</p> $V_{NMI} = 4.68 \times \left(\frac{R1}{R2 // 45.5} + 1 \right)$ <p>R1, R2; kΩ</p>	<p>The voltage at which the \overline{NMI} signal is output when V_{CC} falls. (When NMI_{sns} is connected to V_{CC}.)</p> <p>The \overline{NMI} detection voltage can be adjusted by connecting resistors between the NMI_{sns} pin and V_{CC} (R1), and between the NMI_{sns} pin and ground (R2).</p> 
$OUTE$	$C_R \times R_R > 19.3 \times C_f \times R_f$	<p>If the $OUTE$ function is used, the relationship shown at the left must be fulfilled to assure that pulses are not incorrectly generated in this output when a microprocessor runaway state is detected.</p>

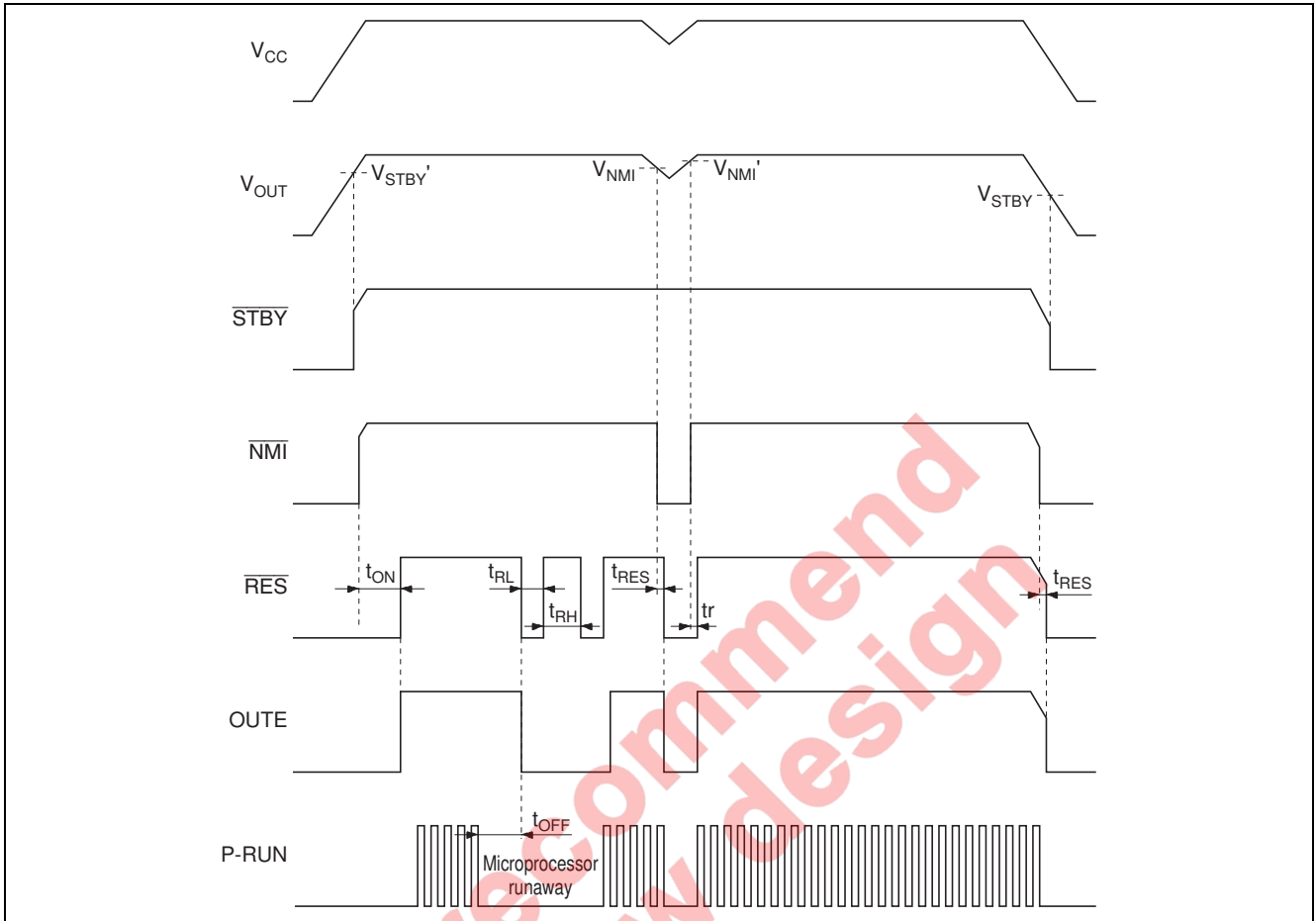
Calculation Formulas (cont.)

Item	Formula	Notes
WDT.	$f_{Line1} = \frac{0.31 \times (Du - 24)}{Cf \cdot Rf}$ $f_{Line2} = 24\% \text{ (fixed)}$ $f_{Line3} = \frac{0.024}{Cf \cdot Rf}$ $f_{Line4} = 99\%$ <p>The relationship between f_{Line1} and f_{Line3}</p> $f_{Line1} = f_{Line3} \times 12.9 (Du - 24)$ <p>Du: The P-RUN signal duty cycle</p>  $Du = \frac{t_H}{t_H + t_L} \times 100$	<p>The WDT function judges whether the P-RUN pulse signal is normal or not. If the WDT function judges the P-RUN pulse signal to be abnormal, it outputs a reset signal. The normal range is the area enclosed by f_{Line1} to f_{Line4} in the figure.</p> 

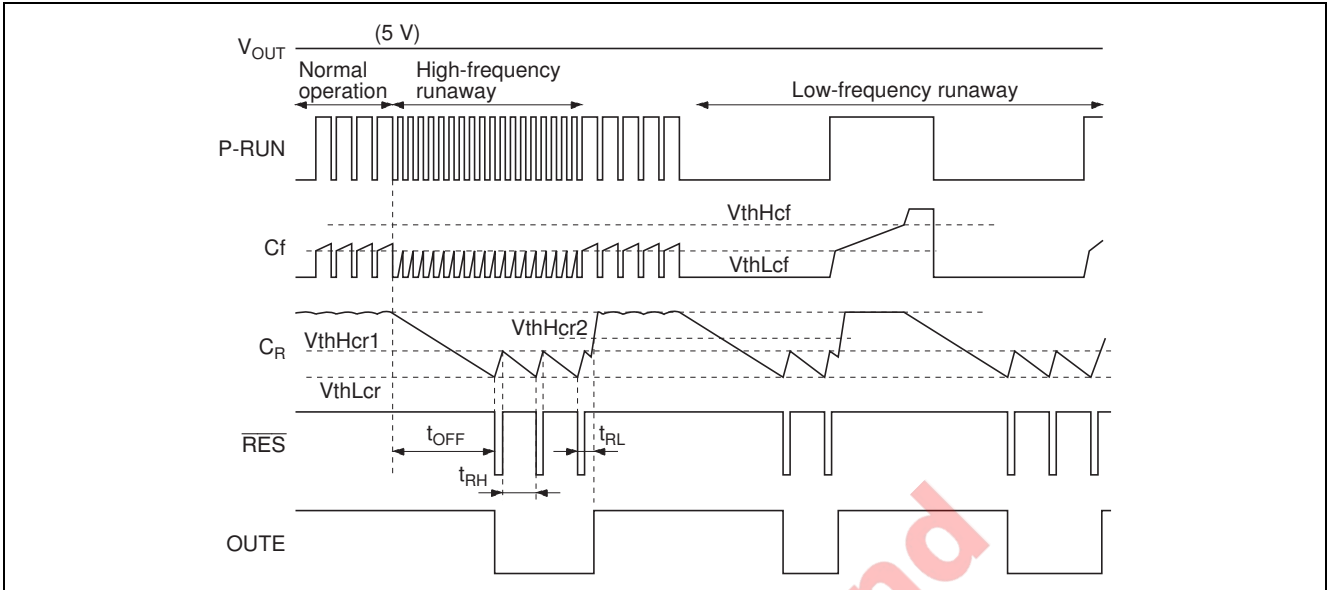
Not recommend
for new design

Timing Charts

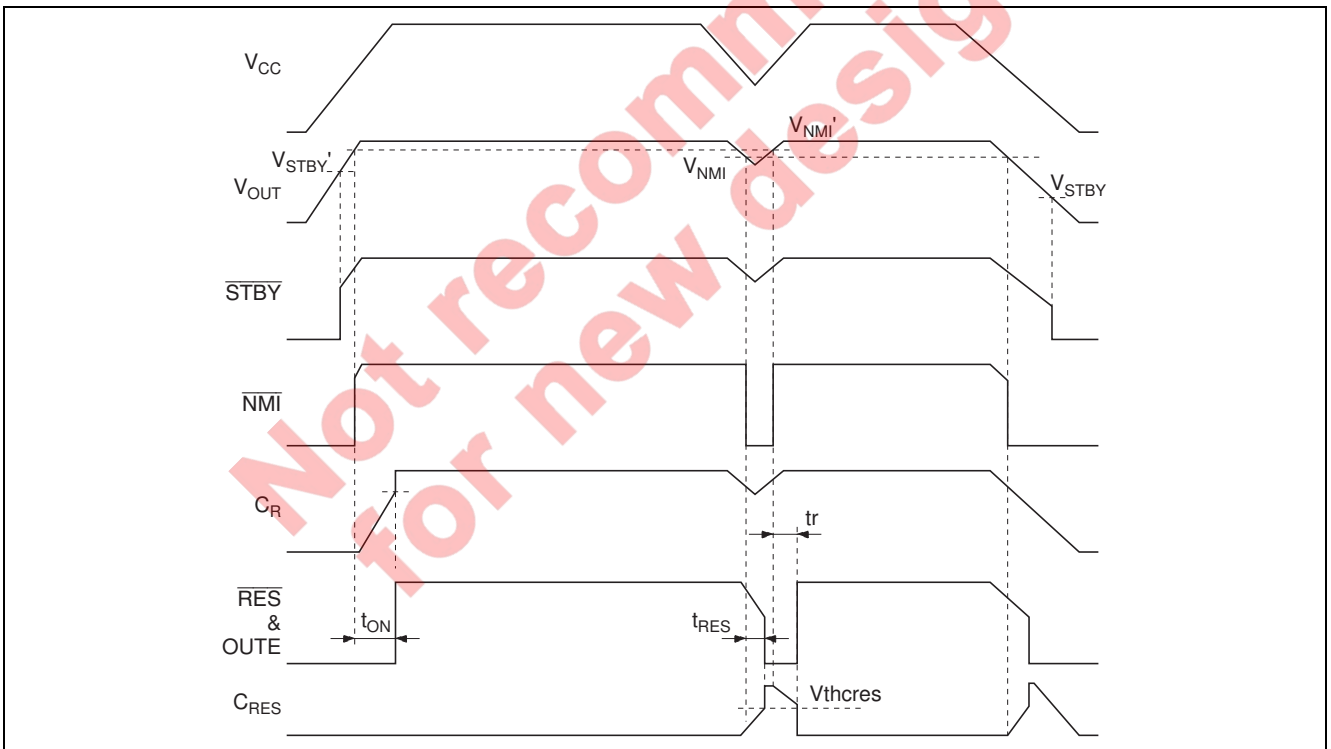
Whole system timing chart



WDT. timing chart



LVI timing chart

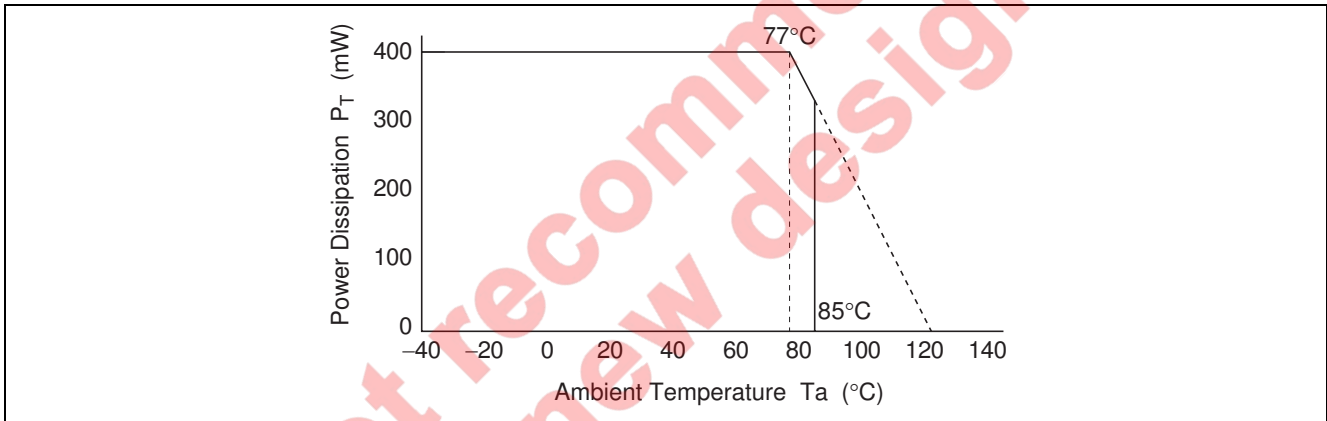


Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Rating	Unit
Power supply voltage	V _{CC}	40	V
CS pin voltage	V _{CS}	V _{CC}	V
CONT pin current	I _{cont}	20	mA
CONT pin voltage	V _{cont}	V _{CC}	V
Vout pin voltage	V _{out}	12	V
P-RUN pin voltage	V _{PRUN}	V _{out}	V
NMIsns pin voltage	V _{NMIsns}	V _{CC}	V
NMI pin voltage	V _{NMI}	V _{out}	V
STBY pin voltage	V _{STBY}	V _{out}	V
RES pin voltage	V _{RES}	V _{out}	V
OUTE pin voltage	V _{OUTE}	V _{out}	V
Power dissipation ^{*1}	P _T	400	mW
Operating temperature	T _{opr}	-40 to +85	°C
Storage temperature	T _{stg}	-50 to +125	°C

Note: 1. This is the allowable value when mounted on a 40 × 40 × 1.6 mm glass-epoxy printed circuit board with a mounting density of 10% at ambient temperatures up to Ta = 77°C. This value must be derated by 8.3 mW/°C above that temperature.



Electrical Characteristics

($T_a = 25^\circ\text{C}$, $V_{CC} = 12\text{V}$, $V_{out} = 5.0\text{V}$, $R_f = R_R = 180\text{k}\Omega$, $C_f = 3300\text{pF}$, $C_R = 0.1\mu\text{F}$, $R_T = 390\text{k}\Omega$, $C_{RES} = 1500\text{pF}$, $R_{CS} = 0.2\Omega$)

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Power supply current		I_{CC}	–	10	15	mA	
Short detection voltage		V_{CS}	400	700	900	mV	$V_{CS} = (V_{CC} \text{ pin voltage} - \text{CS pin voltage})$
Regulator block	Output voltage	V_{out}	4.925	5.00	5.075	V	$V_{CC} = 12\text{V}$, $I_{cont} = 5\text{mA}$
	Input voltage stabilization	V_{olin}	–30	–	30	mV	$V_{CC} = 6 \text{ to } 17.5\text{V}$, $I_{cont} = 10\text{mA}$
	Load current stabilization	V_{oload}	–30	–	30	mV	$I_{cont} = 0.1 \text{ to } 15\text{mA}$
	Ripple exclusion ratio	R_{REJ}	(45)	75	–	dB	$V_i = 0.5V_{rms}$, $f_i = 1\text{kHz}$
	Output voltage temperature coefficient	$ \delta V_{out}/\delta T $	–	40	(200)	ppm/ $^\circ\text{C}$	$I_{cont} = 5\text{mA}$
	Output voltage adjustment range	V_{oMAX}	–	–	7.0	V	
P-RUN input block	Input high-level voltage	V_{IH}	2.0	–	–	V	
	Input low-level voltage	V_{IL}	–	–	0.8	V	
	Input high-level current	I_{IH}	–	300	500	μA	$V_{IH} = 5.0\text{V}$
	Input low-level current	I_{IL}	–5	0	5	μA	$V_{IL} = 0.0\text{V}$
NMI output block	High level	V_{OHN}	$V_{out} - 0.2$	V_{out}	$V_{out} + 0.2$	V	$I_{OHN} = 0\text{mA}$
	Low level	V_{OLN}	–	–	0.4	V	$I_{OLN} = 2.0\text{mA}$
	Function start voltage	V_{STN}	–	0.7	1.4	V	
STBY output block	High level	V_{OHS}	$V_{out} - 0.2$	V_{out}	$V_{out} + 0.2$	V	$I_{OHS} = 0\text{mA}$
	Low level	V_{OLS}	–	–	0.4	V	$I_{OLS} = 2.0\text{mA}$
	Function start voltage	V_{STS}	–	0.7	1.4	V	

Note: Values in parentheses are design reference values.

Electrical Characteristics (cont.)

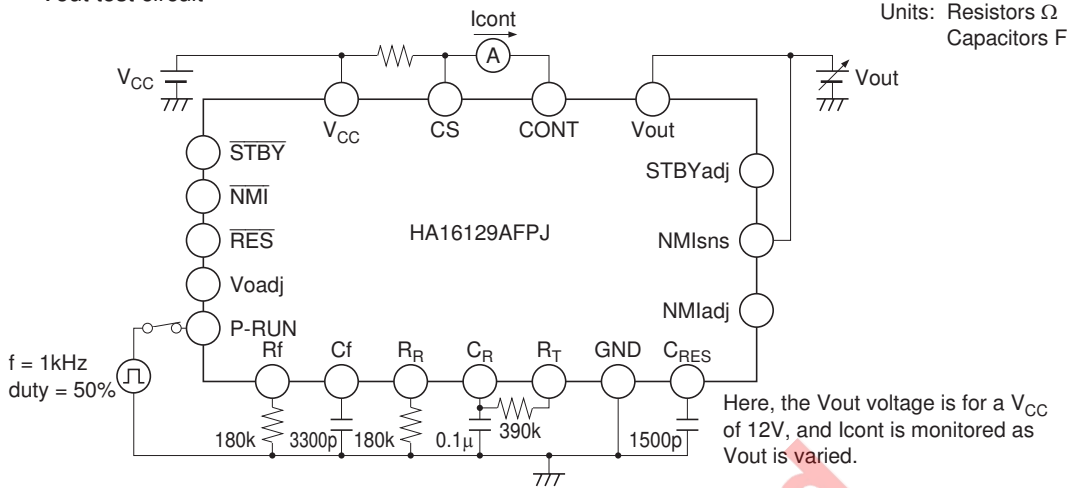
($T_a = 25^\circ\text{C}$, $V_{CC} = 12\text{V}$, $V_{out} = 5.0\text{V}$, $R_f = R_R = 180\text{k}\Omega$, $C_f = 3300\text{pF}$, $C_R = 0.1\mu\text{F}$, $R_T = 390\text{k}\Omega$, $C_{RES} = 1500\text{pF}$, $R_{CS} = 0.2\Omega$)

Item		Symbol	Min	Typ	Max	Unit	Test Conditions	
RES output block	High level	V_{OHR}	$V_{out} - 0.2$	V_{out}	$V_{out} + 0.2$	V	$I_{OHR} = 0\text{mA}$	
	Low level	V_{OLR}	–	–	0.4	V	$I_{OLR} = 2.0\text{mA}$	
	Function start voltage	V_{STR}	–	0.7	1.4	V		
OUTE output block	High level	V_{OHE}	$V_{out} - 0.2$	V_{out}	$V_{out} + 0.2$	V	$I_{OHE} = 0\text{mA}$	
	Low level	V_{OLE}	–	–	0.4	V	$I_{OLE} = 2.0\text{mA}$	
	Function start voltage	V_{STE}	–	0.7	1.4	V		
RES function	Power on time	t_{on}	25	40	60	ms		
	Clock off time	t_{off}	80	130	190	ms		
	Reset pulse high time	t_{RH}	40	60	90	ms		
	Reset pulse low time	t_{RL}	15	20	30	ms		
LVI function	NMI function (V_{out} detection)	Detection voltage 1	V_{NMI1}	4.5	4.63	4.75	V	
		Hysteresis 1	V_{HYSN1}	–	50	100	mV	
		Temperature coefficient	$ \delta V_{NMI}/\delta T $	–	100	(400)	ppm/ $^\circ\text{C}$	
	NMI function (V_{CC} detection)	Detection voltage 2	V_{NMI2}	5.0	5.4	5.7	V	$R1 = 13\text{k}\Omega$, $R2 = 390\text{k}\Omega$
		Hysteresis 2	V_{HYSN2}	0.5	0.8	1.3	V	$R1 = 13\text{k}\Omega$, $R2 = 390\text{k}\Omega$
	STBY function	Detection voltage	V_{STBY}	2.70	3.00	3.30	V	
		Hysteresis	V_{HYSS}	1.20	1.35	1.50	V	
		Temperature coefficient	$ \delta V_{STBY}/\delta T $	–	100	(400)	ppm/ $^\circ\text{C}$	
	RES delay time	Disable time	t_{RES}	(100)	200	(300)	μs	
Recovery time		t_r	(100)	200	(300)	μs		

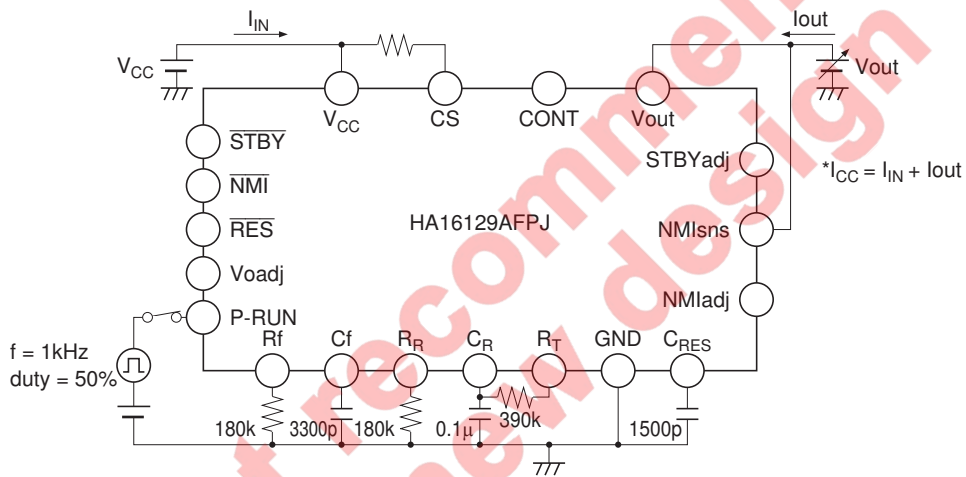
Note: Values in parentheses are design reference values.

Test Circuits

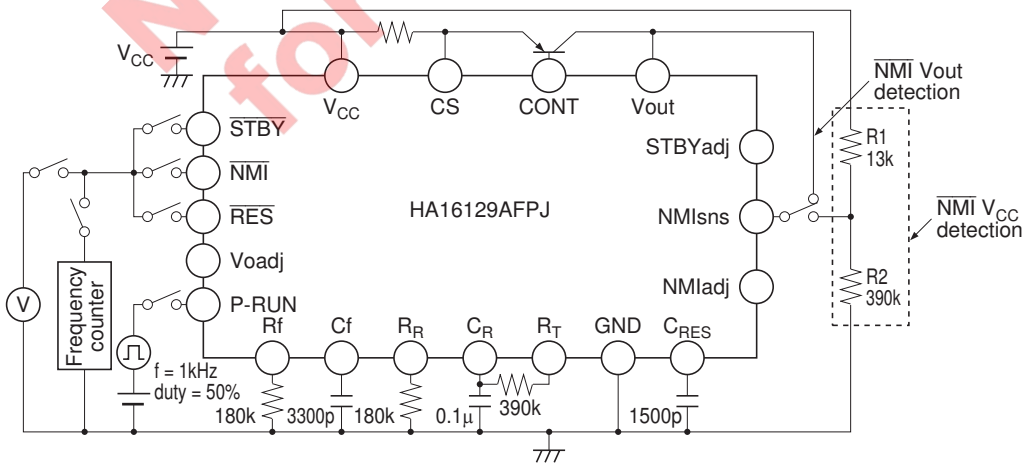
• Vout test circuit



• ICC test circuit

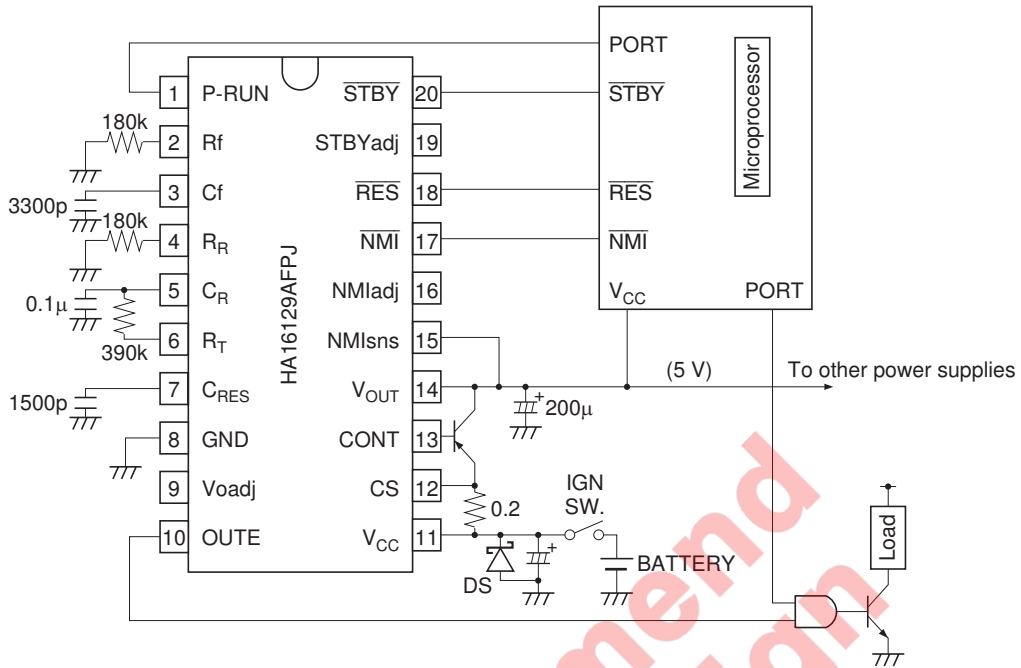


• Test circuit for other parameters

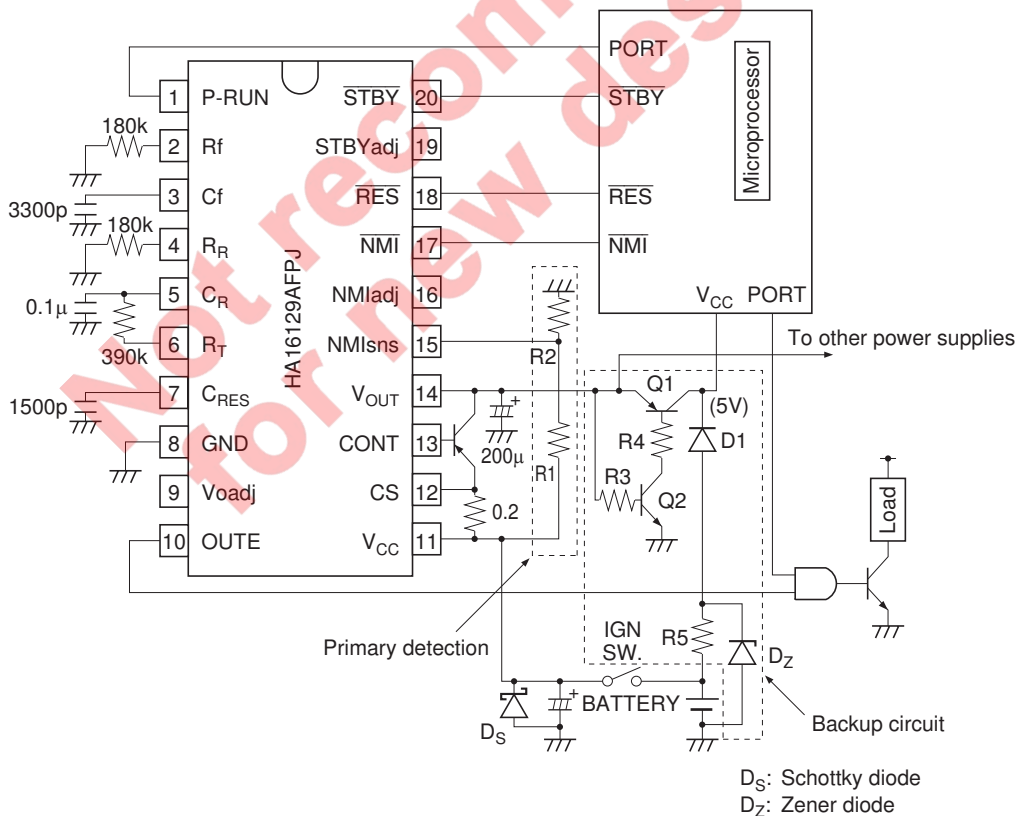


System Circuit Examples

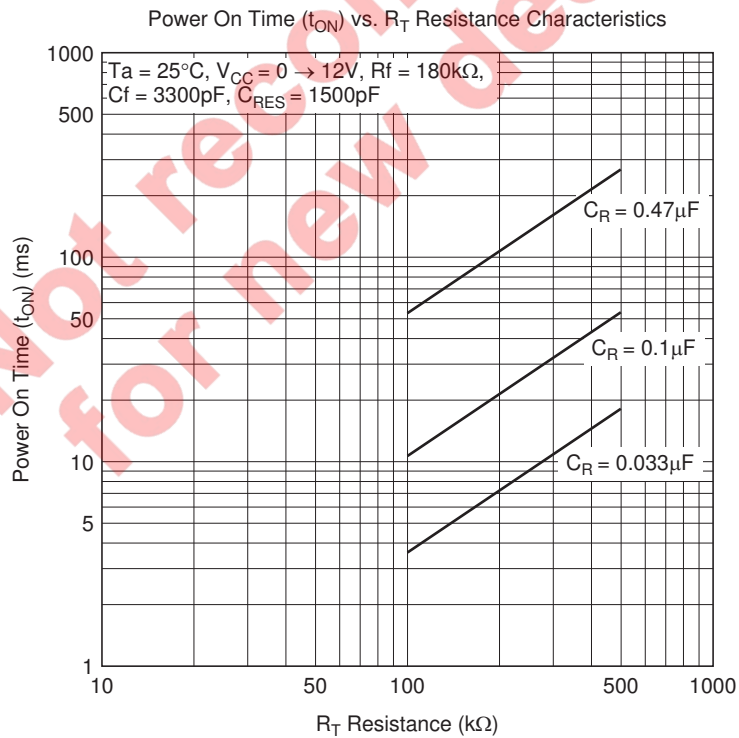
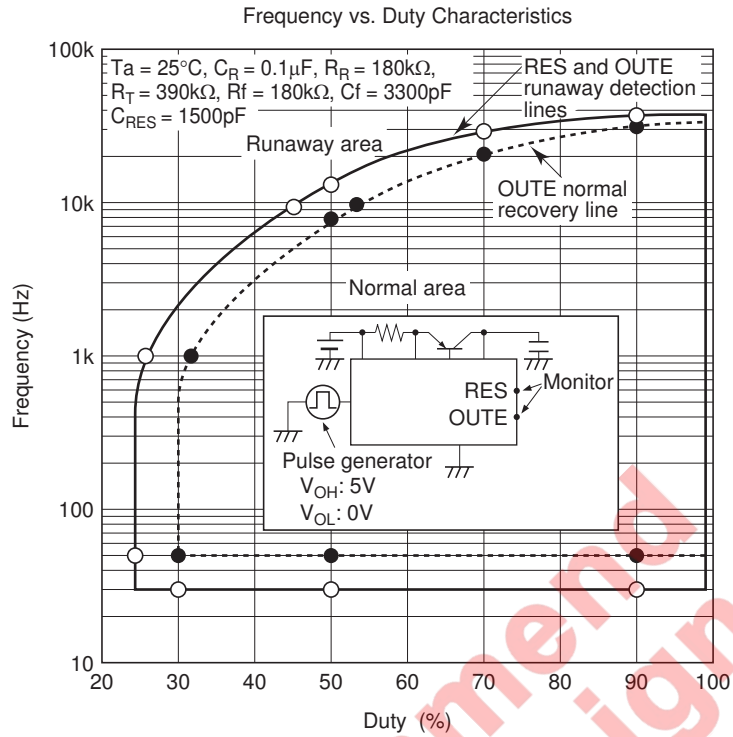
- Example of a basic system

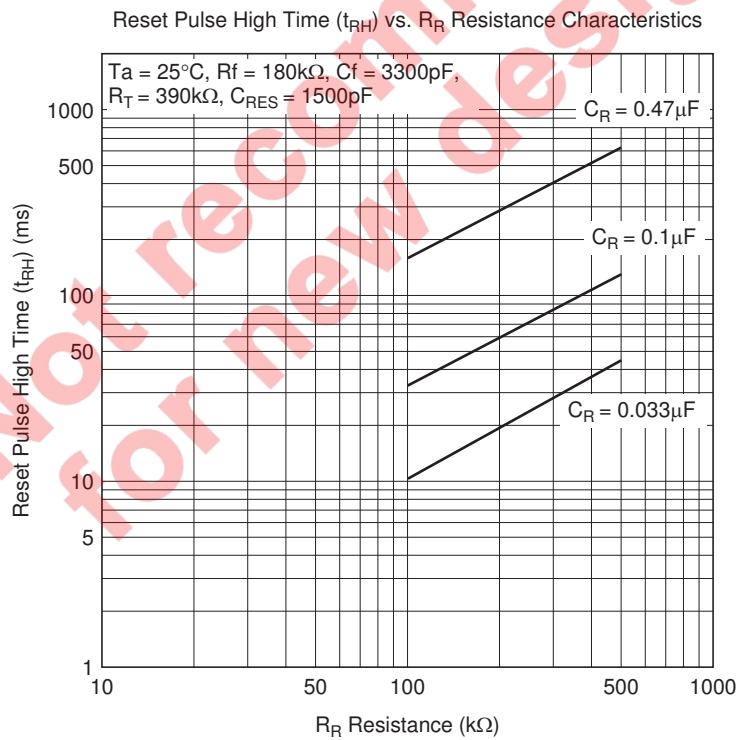
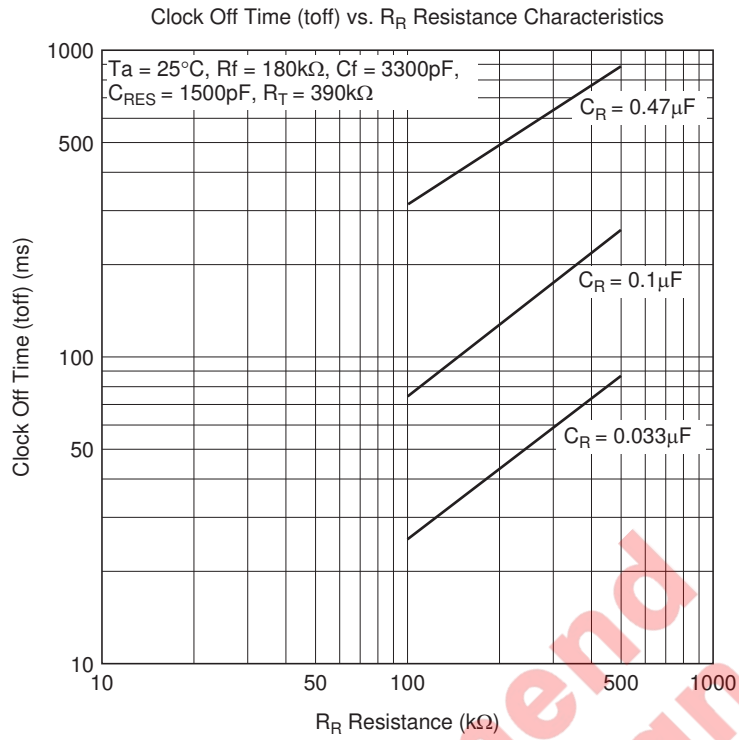


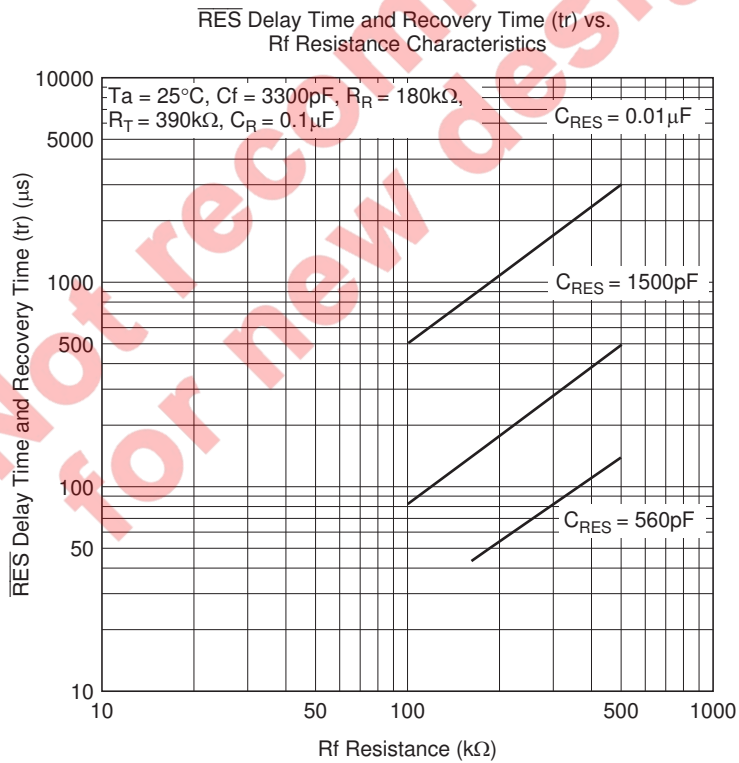
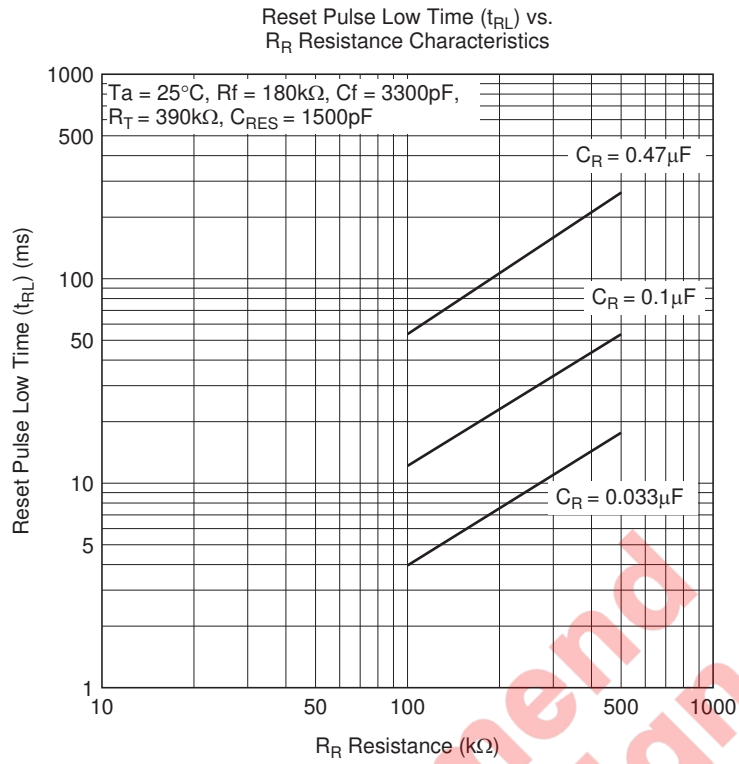
- Example of a system using a backup circuit and a primary voltage monitoring circuit



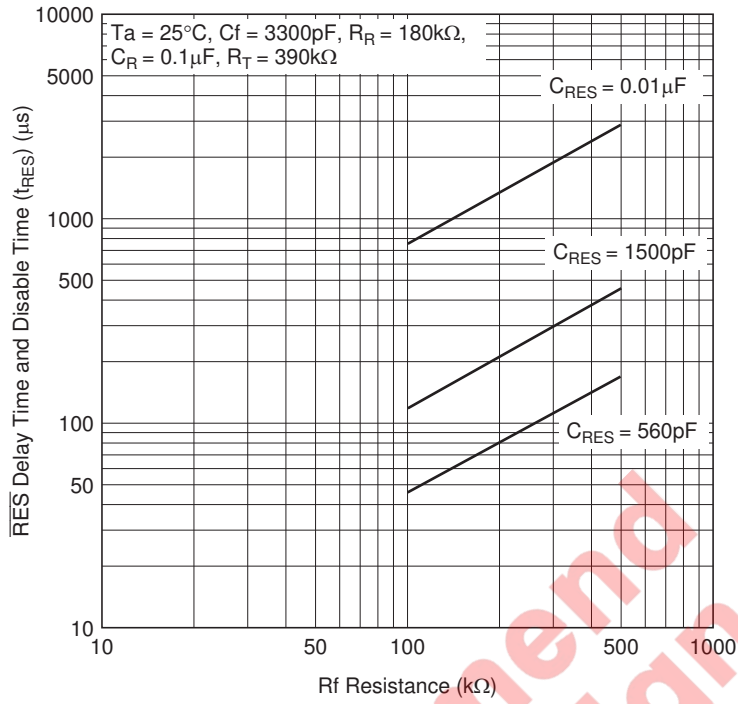
Operating Waveforms



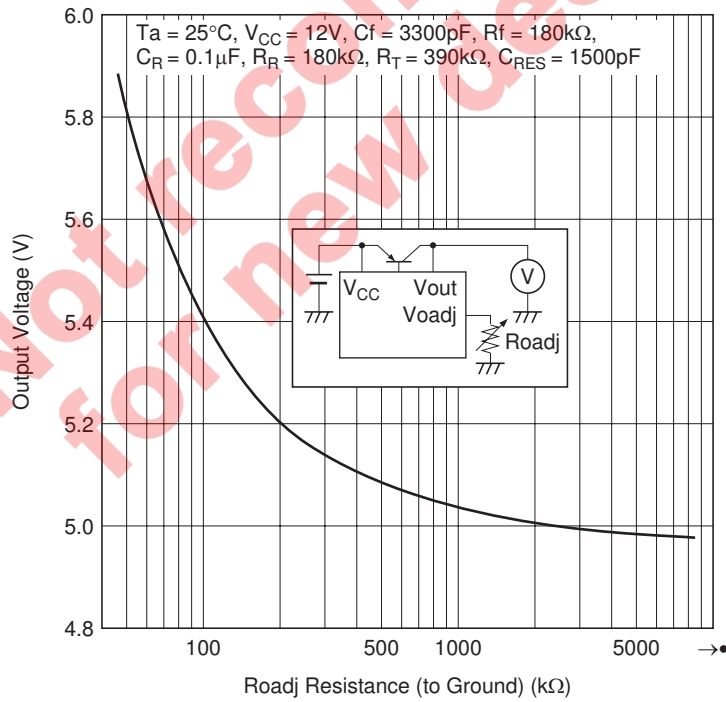


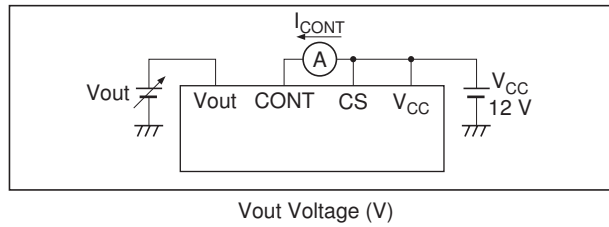
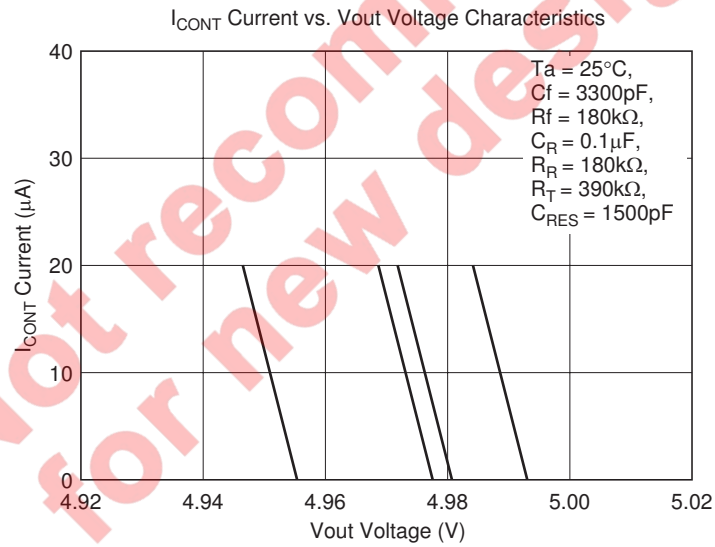
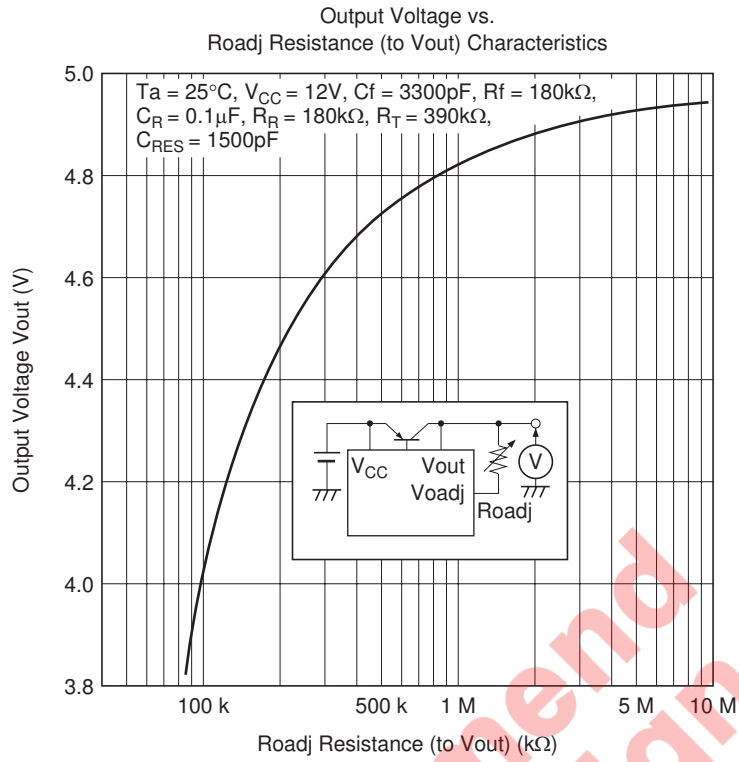


RES Delay Time and Disable Time (t_{RES}) vs. Rf Resistance Characteristics

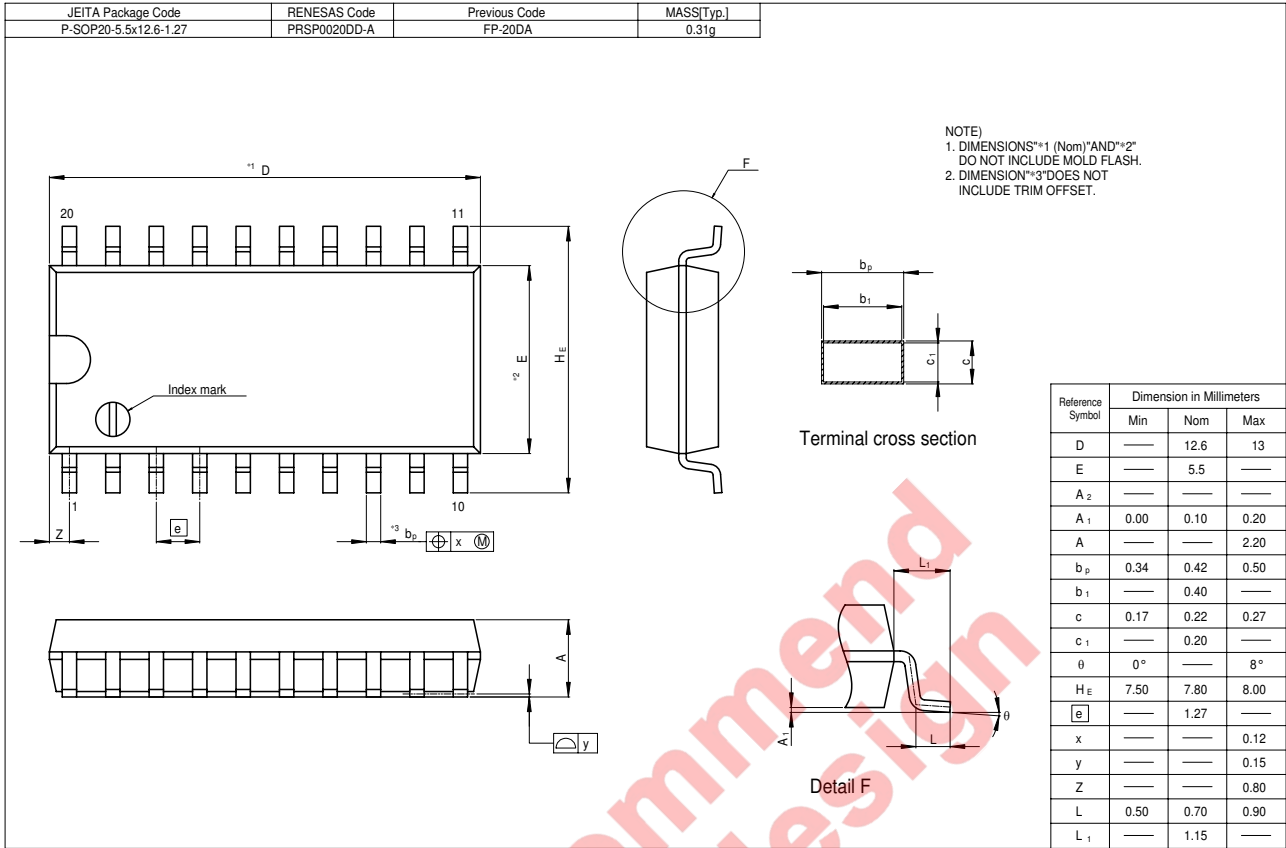


Output Voltage vs. Roadj Resistance (to Ground) Characteristics





Package Dimensions



Not recommended for new design

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