

To our customers,

Old Company Name in Catalogs and Other Documents

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Renesas Electronics website: <http://www.renesas.com>

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (<http://www.renesas.com>)

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MOS FIELD EFFECT TRANSISTOR

2SK4080

SWITCHING

N-CHANNEL POWER MOS FET

DESCRIPTION

The 2SK4080 is N-channel MOS FET device that features a low on-state resistance and excellent switching characteristics, and designed for low voltage high current applications such as DC/DC converter with synchronous rectifier.

FEATURES

- Low on-state resistance
 $R_{DS(on)1} = 9.0 \text{ m}\Omega \text{ MAX. (} V_{GS} = 10 \text{ V, } I_D = 24 \text{ A)}$
- Low Q_{GD} : $Q_{GD} = 6.3 \text{ nC TYP.}$
- 4.5 V drive available

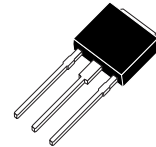
ORDERING INFORMATION

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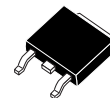
PART NUMBER	PACKAGE
2SK4080(1)-S27-AY ^{Note}	TO-251 (MP-3-b)
2SK4080-ZK-E1-AY ^{Note}	TO-252 (MP-3ZK)
2SK4080-ZK-E2-AY ^{Note}	TO-252 (MP-3ZK)

Note Pb-free (This product does not contain Pb in external electrode.)

(TO-251)



(TO-252)



ABSOLUTE MAXIMUM RATINGS (T_A = 25°C)

Drain to Source Voltage (V _{GS} = 0 V)	V _{DSS}	30	V
Gate to Source Voltage (V _{DS} = 0 V)	V _{GSS}	±20	V
Drain Current (DC) (T _C = 25°C)	I _{D(DC)}	±48	A
Drain Current (pulse) ^{Note1}	I _{D(pulse)}	±144	A
Total Power Dissipation (T _C = 25°C)	P _{T1}	29	W
Total Power Dissipation	P _{T2}	1.0	W
Channel Temperature	T _{ch}	150	°C
Storage Temperature	T _{stg}	−55 to +150	°C
Single Avalanche Current ^{Note2}	I _{AS}	21	A
Single Avalanche Energy ^{Note2}	E _{AS}	44.1	mJ

Notes 1. PW ≤ 10 μs, Duty Cycle ≤ 1%

2. Starting T_{ch} = 25°C, V_{DD} = 15 V, R_G = 25 Ω, V_{GS} = 20 → 0 V, L = 100 μH

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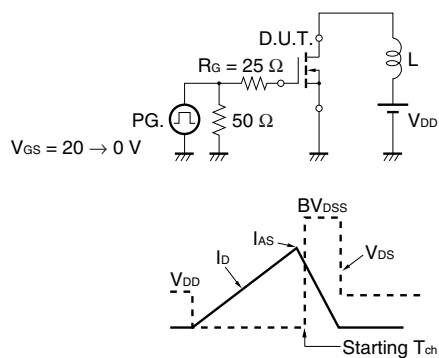
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ELECTRICAL CHARACTERISTICS (T_A = 25°C)

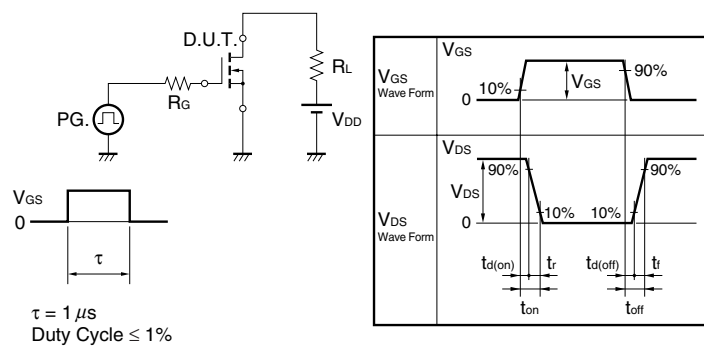
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 30 V, V _{GS} = 0 V			10	μA
Gate Leakage Current	I _{GSS}	V _{GS} = ±20 V, V _{DS} = 0 V			±100	nA
Gate Cut-off Voltage	V _{GS(off)}	V _{DS} = 10 V, I _D = 1 mA	1.5	2.0	2.5	V
Forward Transfer Admittance ^{Note}	y _{fs}	V _{DS} = 10 V, I _D = 12 A	7	14		S
Drain to Source On-state Resistance ^{Note}	R _{DS(on)1}	V _{GS} = 10 V, I _D = 24 A		7.0	9.0	mΩ
	R _{DS(on)2}	V _{GS} = 4.5 V, I _D = 24 A		10.2	15	mΩ
Input Capacitance	C _{iss}	V _{DS} = 10 V		1670		pF
Output Capacitance	C _{oss}	V _{GS} = 0 V		290		pF
Reverse Transfer Capacitance	C _{rss}	f = 1 MHz		150		pF
Turn-on Delay Time	t _{d(on)}	V _{DD} = 15 V		10		ns
Rise Time	t _r	I _D = 30 A		5.3		ns
Turn-off Delay Time	t _{d(off)}	V _{GS} = 12 V		42		ns
Fall Time	t _f	R _G = 3 Ω		6.1		ns
Total Gate Charge	Q _{G1}	V _{DD} = 15 V, V _{GS} = 12 V, I _D = 30 A		32		nC
	Q _{G2}	V _{DD} = 15 V, V _{GS} = 4.5 V, I _D = 30 A		13		nC
Gate to Source Charge	Q _{GS}	V _{DD} = 15 V		4.6		nC
Gate to Drain Charge	Q _{GD}	I _D = 30 A		6.3		nC
Gate Resistance	R _G			2.4		Ω
Body Diode Forward Voltage ^{Note}	V _{F(S-D)}	I _F = 30 A, V _{GS} = 0 V		0.94	1.5	V
Reverse Recovery Time	t _{rr}	I _F = 30 A, V _{GS} = 0 V		29		ns
Reverse Recovery Charge	Q _{rr}	di/dt = 100 A/μs		23		nC

Note Pulsed

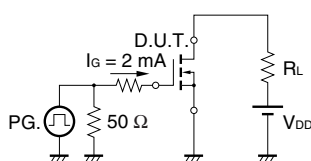
TEST CIRCUIT 1 AVALANCHE CAPABILITY



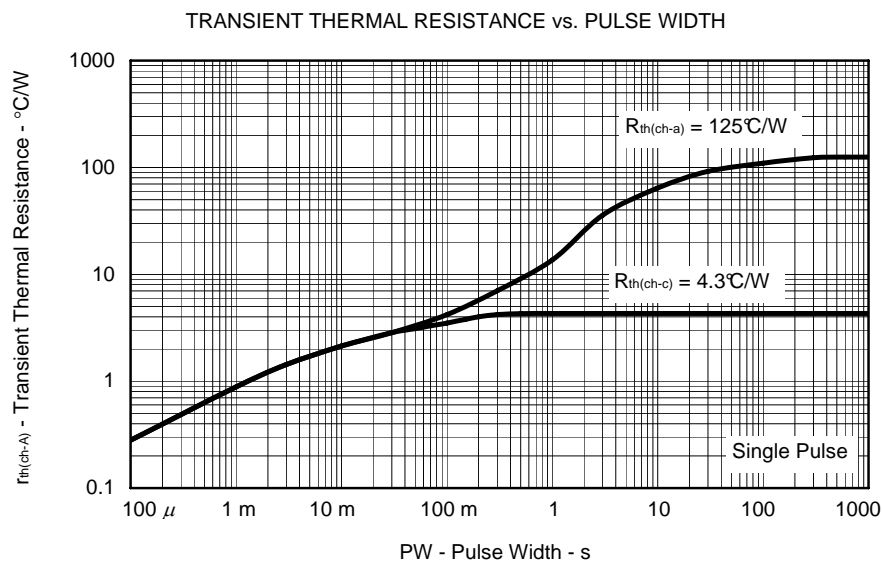
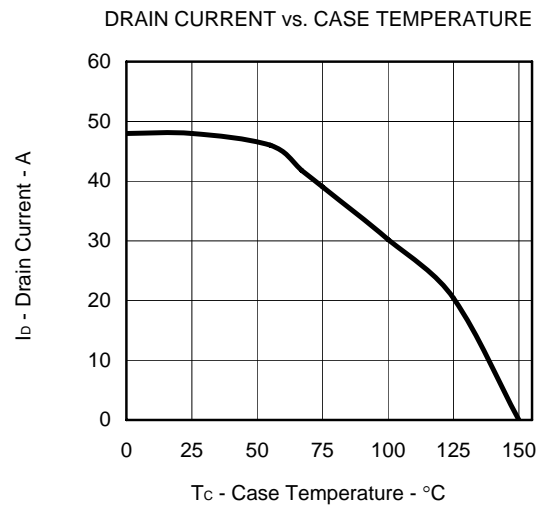
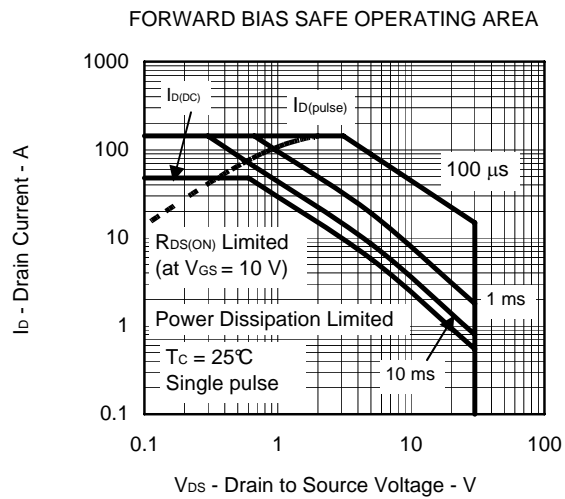
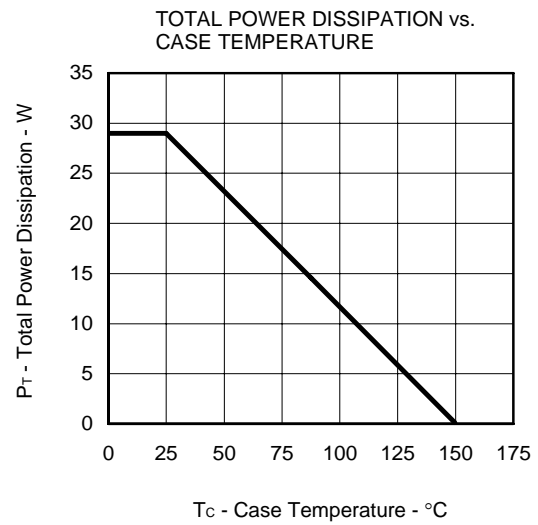
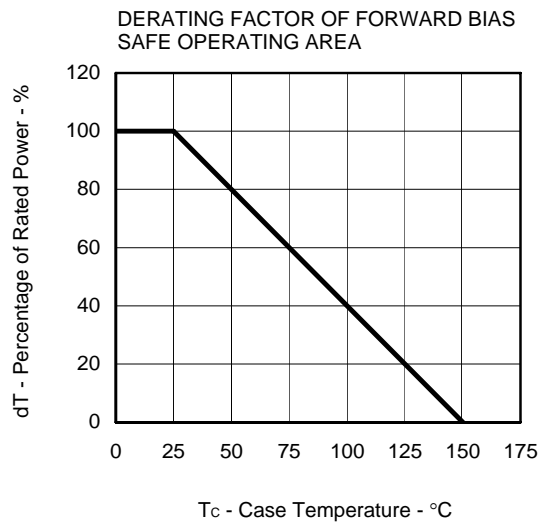
TEST CIRCUIT 2 SWITCHING TIME



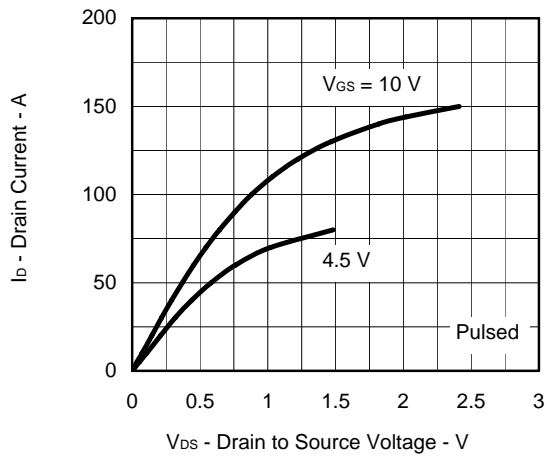
TEST CIRCUIT 3 GATE CHARGE



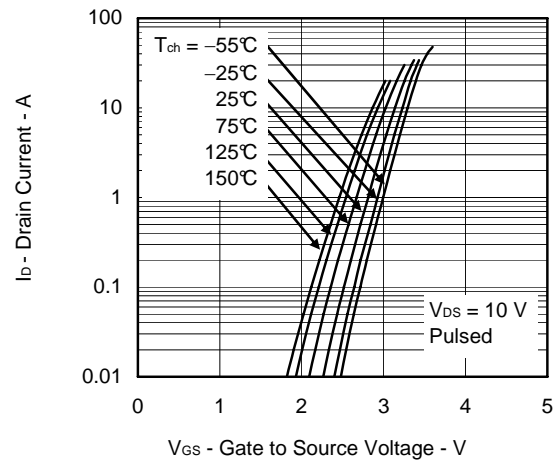
TYPICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$)



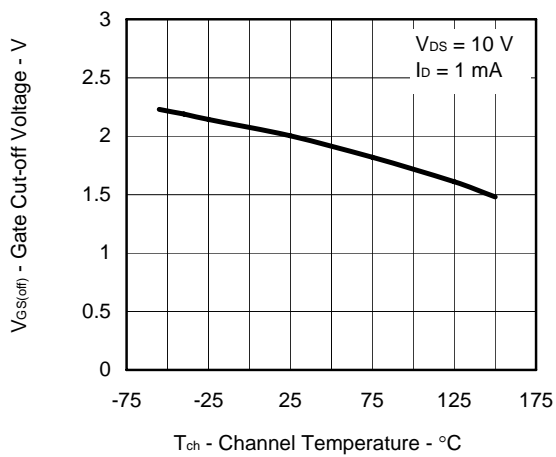
DRAIN CURRENT vs.
DRAIN TO SOURCE VOLTAGE



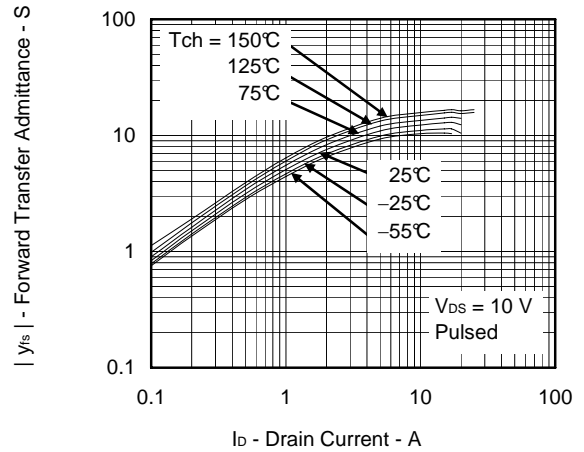
FORWARD TRANSFER CHARACTERISTICS



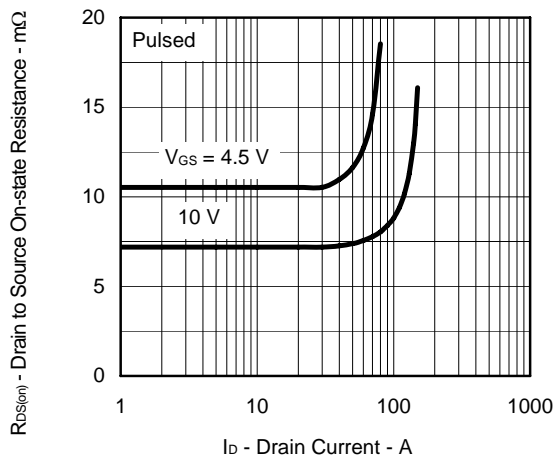
GATE CUT-OFF VOLTAGE vs.
CHANNEL TEMPERATURE



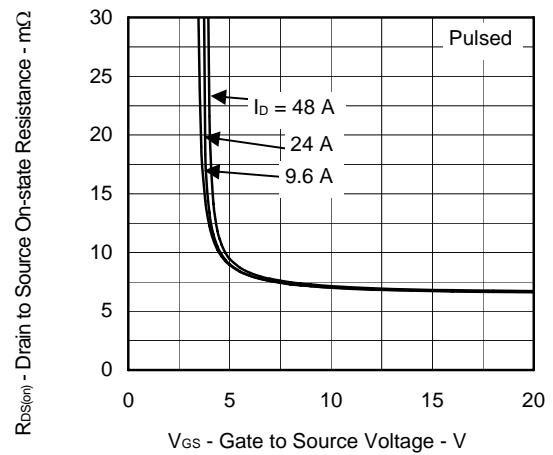
FORWARD TRANSFER ADMITTANCE vs.
DRAIN CURRENT

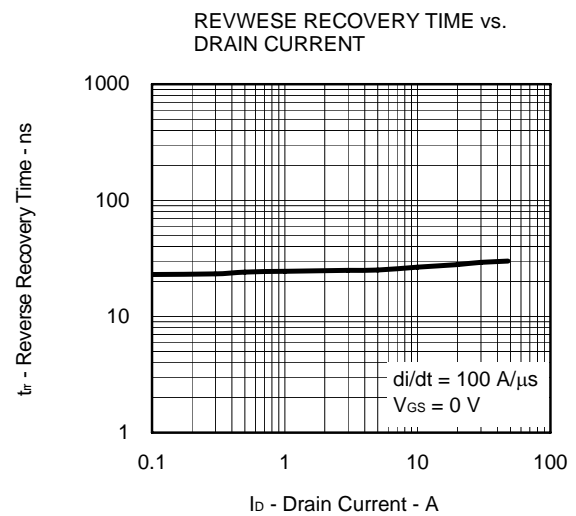
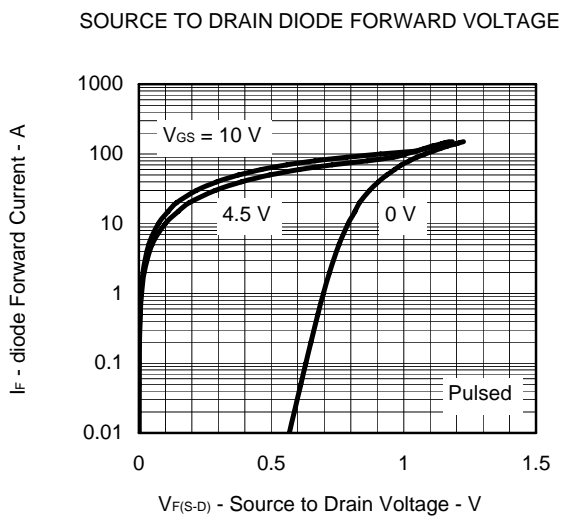
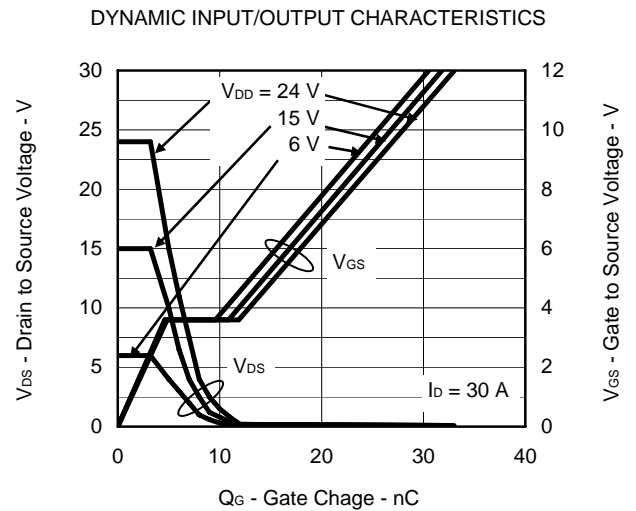
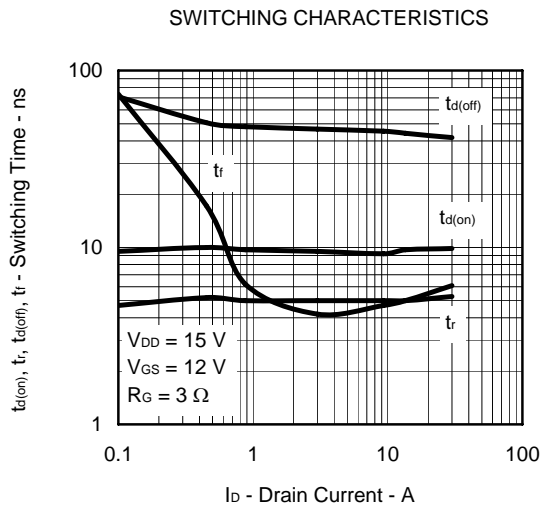
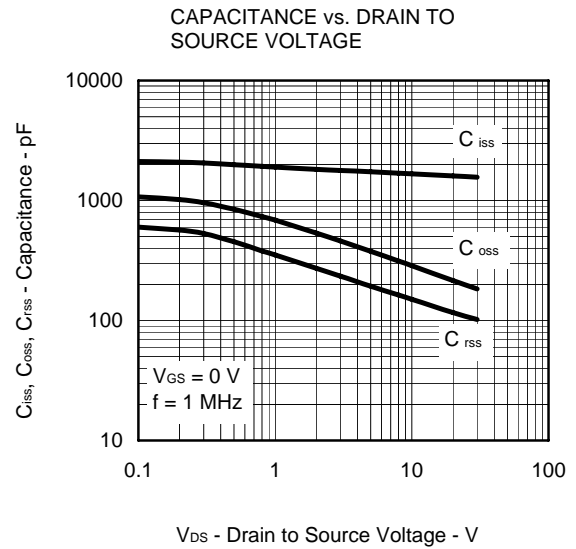
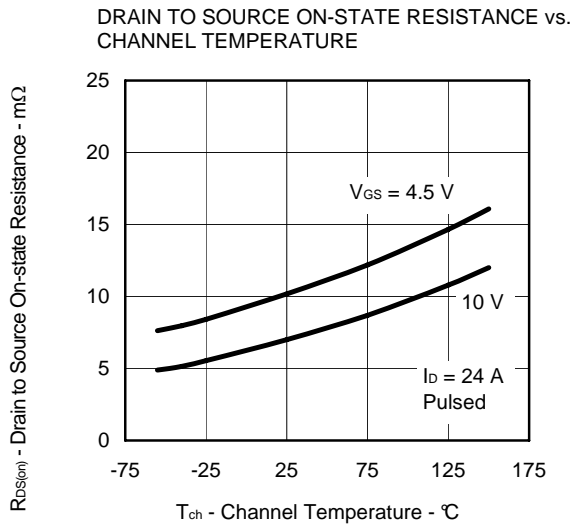


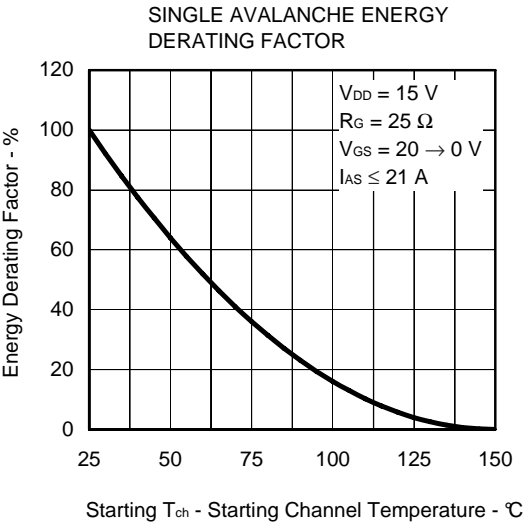
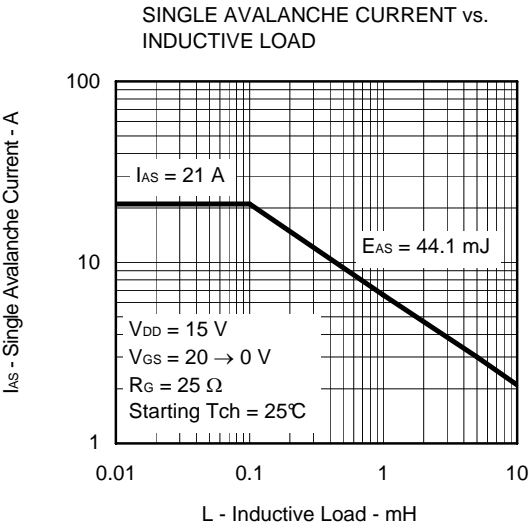
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
DRAIN CURRENT



DRAIN TO SOURCE ON-STATE RESISTANCE vs.
GATE TO SOURCE VOLTAGE



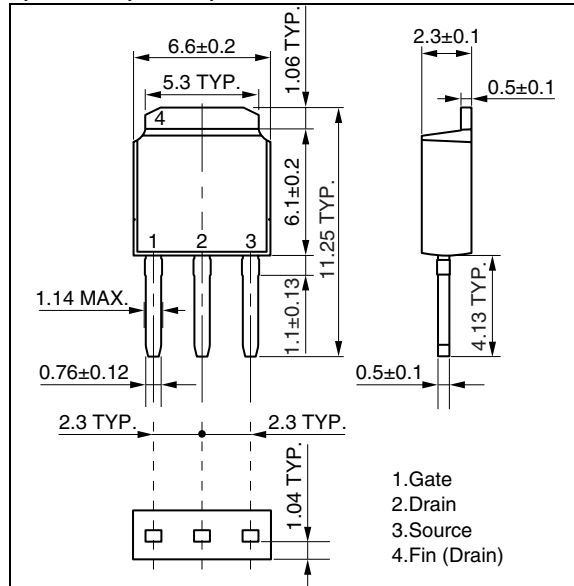




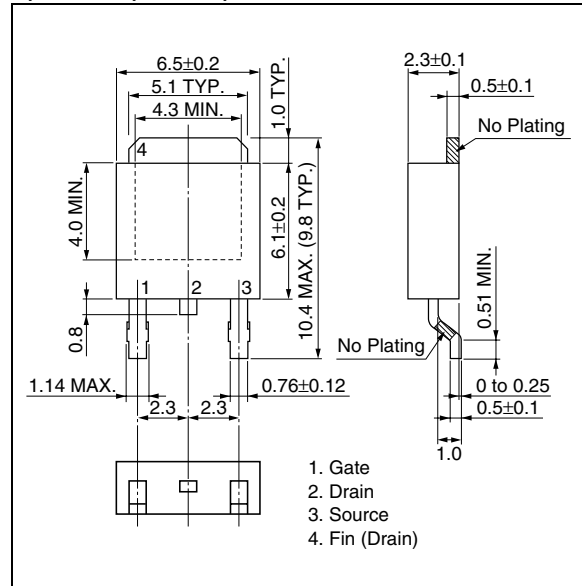
PACKAGE DRAWINGS (Unit: mm)

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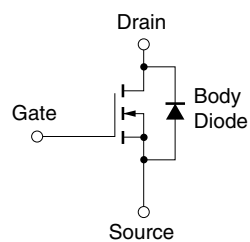
1) TO-251 (MP-3-b)



2) TO-252 (MP-3ZK)



EQUIVALENT CIRCUIT



Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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