

To our customers,

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## Old Company Name in Catalogs and Other Documents

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April 1<sup>st</sup>, 2010  
Renesas Electronics Corporation

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# 2SJ505(L), 2SJ505(S)

Silicon P Channel MOS FET

REJ03G0872-0500  
Rev.5.00  
Jun 05, 2006

## Description

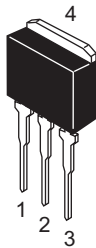
High speed power switching

## Features

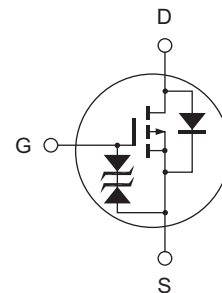
- Low on-resistance  
 $R_{DS(on)} = 0.017 \Omega$  typ.
- Low drive current.
- 4 V gate drive devices.
- High speed switching.

## Outline

RENESAS Package code: PRSS0004AE-A  
(Package name: LDPAK (L) )



RENESAS Package code: PRSS0004AE-B  
(Package name: LDPAK (S)-(1) )



1. Gate
2. Drain
3. Source
4. Drain

## Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Value	Unit
Drain to source voltage	V <sub>DSS</sub>	-60	V
Gate to source voltage	V <sub>GSS</sub>	±20	V
Drain current	I <sub>D</sub>	-50	A
Drain peak current	I <sub>D (pulse)</sub> <sup>Note 1</sup>	-200	A
Body to drain diode reverse drain current	I <sub>DR</sub>	-50	A
Avalanche current	I <sub>AP</sub> <sup>Note 3</sup>	-50	A
Avalanche energy	E <sub>AR</sub> <sup>Note 3</sup>	214	mJ
Channel dissipation	P <sub>ch</sub> <sup>Note 2</sup>	75	W
Channel temperature	T <sub>ch</sub>	150	°C
Storage temperature	T <sub>stg</sub>	-55 to +150	°C

- Notes: 1. PW ≤ 10 μs, duty cycle ≤ 1%  
 2. Value at T<sub>c</sub> = 25°C  
 3. Value at Ta = 25°C, R<sub>g</sub> ≥ 50 Ω

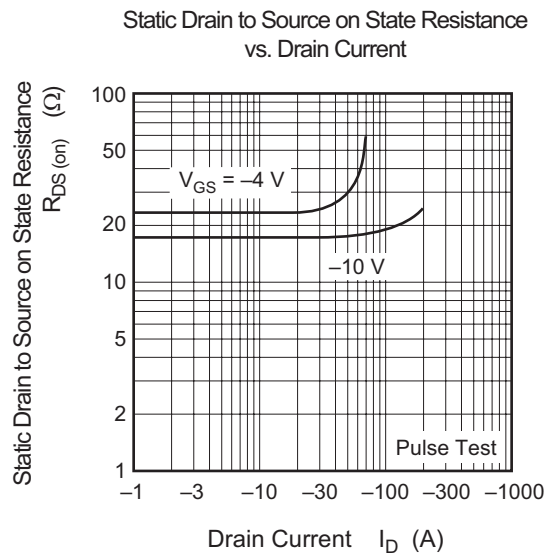
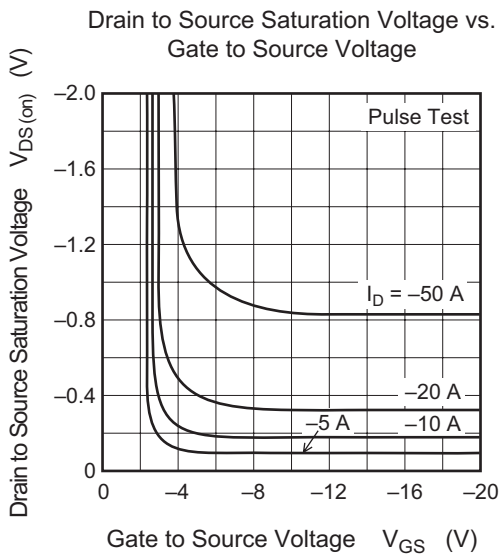
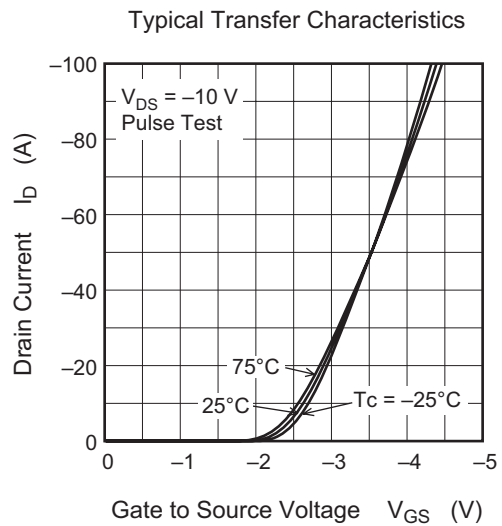
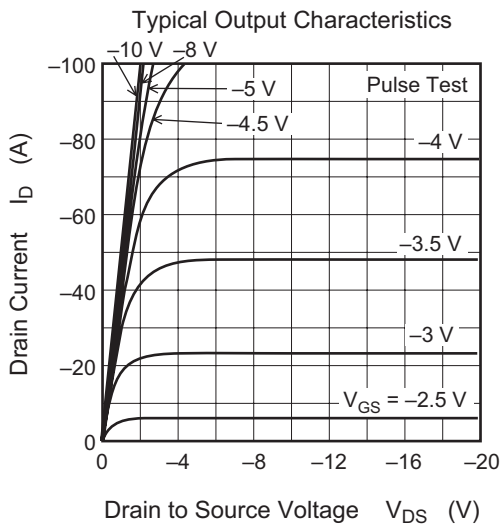
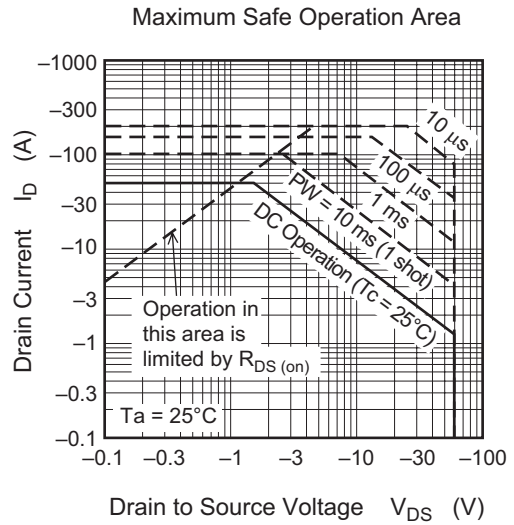
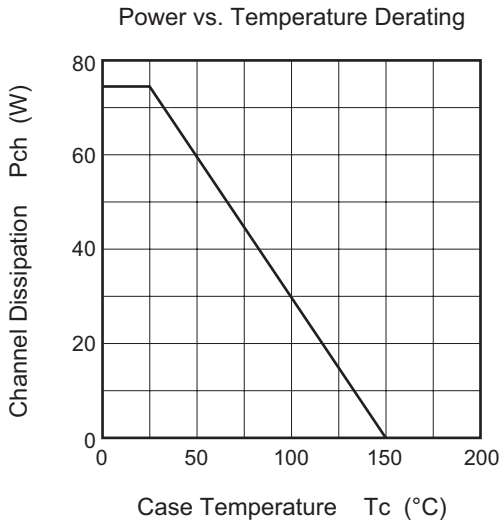
## Electrical Characteristics

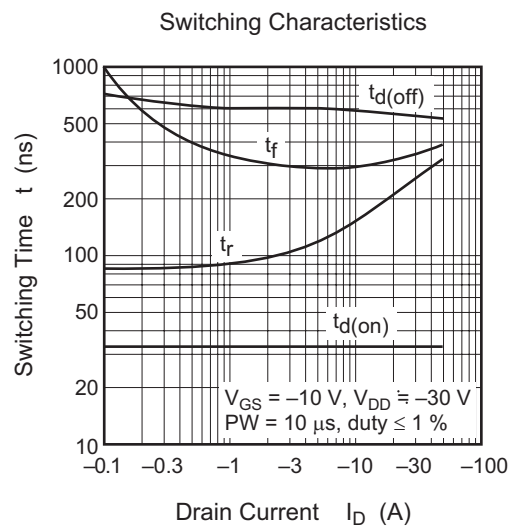
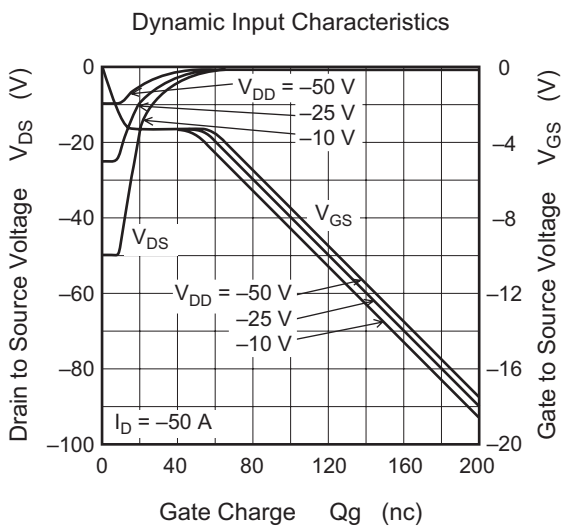
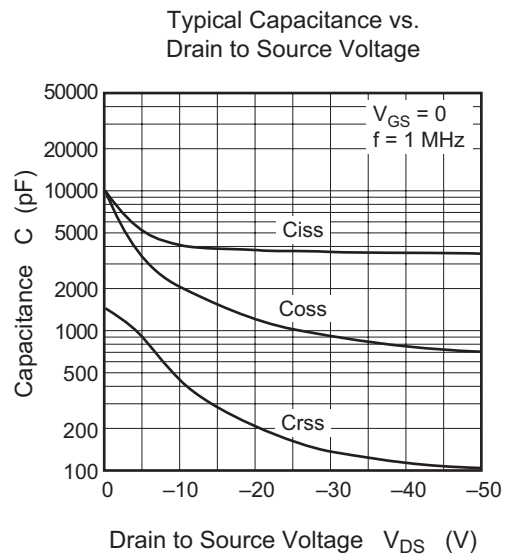
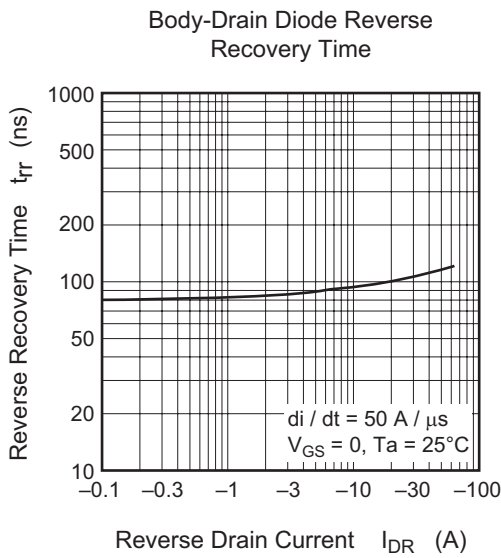
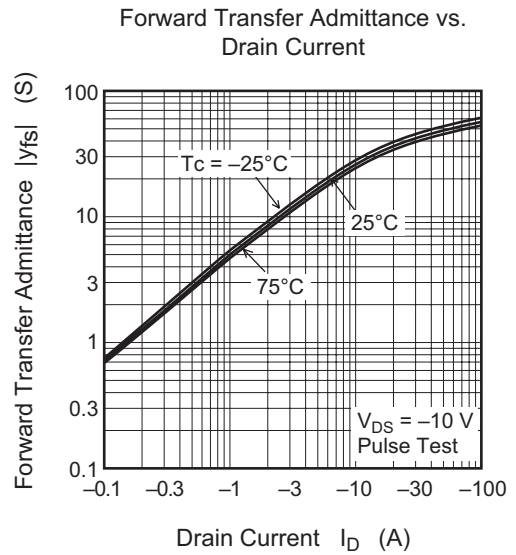
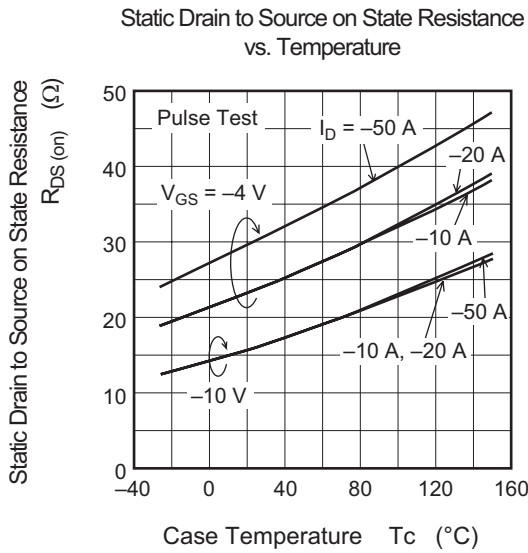
(Ta = 25°C)

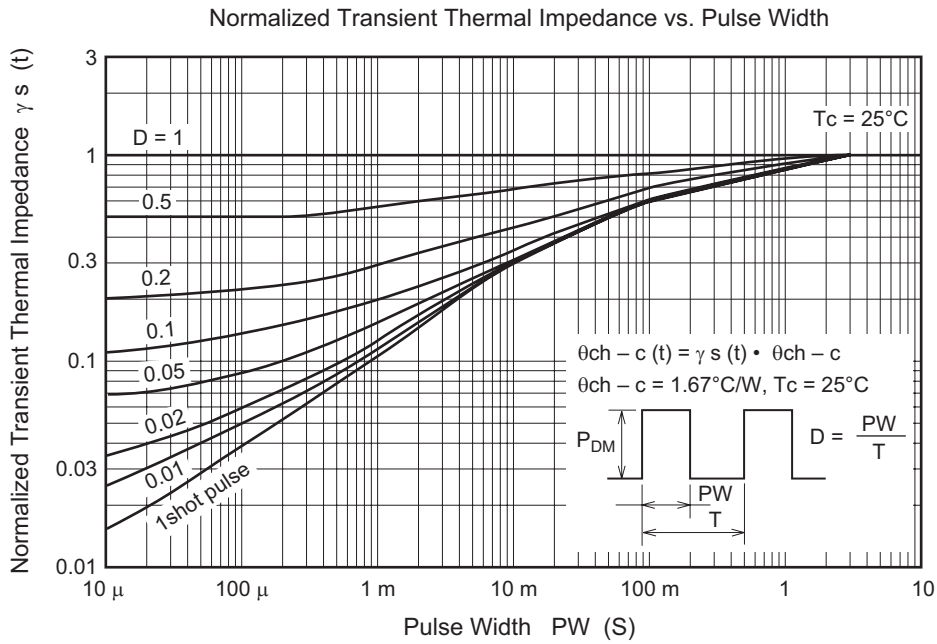
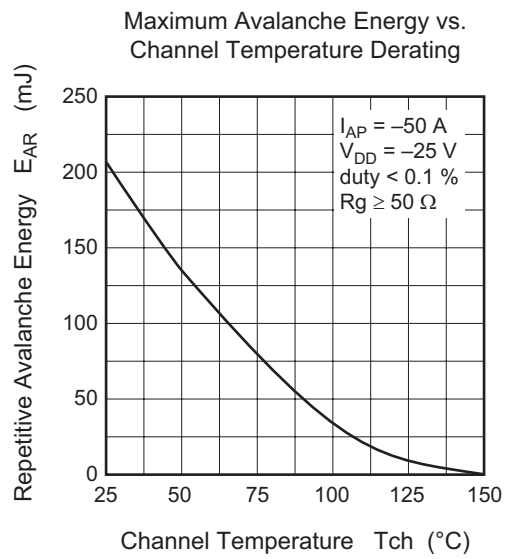
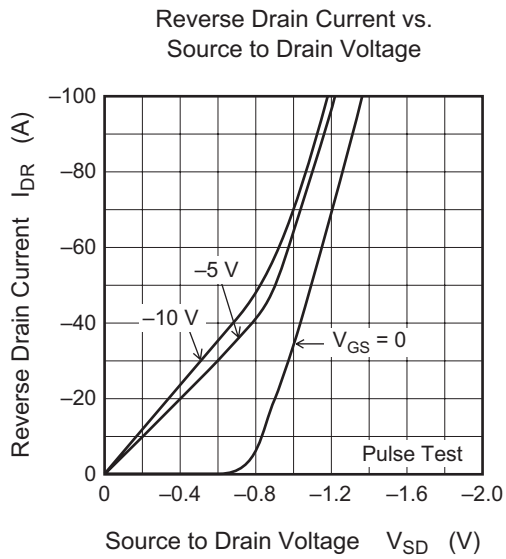
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	V <sub>(BR) DSS</sub>	-60	—	—	V	I <sub>D</sub> = -10 mA, V <sub>GS</sub> = 0
Gate to source breakdown voltage	V <sub>(BR) GSS</sub>	±20	—	—	V	I <sub>G</sub> = ±100 μA, V <sub>DS</sub> = 0
Zero gate voltage drain current	I <sub>DSS</sub>	—	—	-10	μA	V <sub>DS</sub> = -60 V, V <sub>GS</sub> = 0
Gate to source leak current	I <sub>GSS</sub>	—	—	±10	μA	V <sub>GS</sub> = ±16 V, V <sub>DS</sub> = 0
Gate to source cutoff voltage	V <sub>GS (off)</sub>	-1.0	—	-2.0	V	I <sub>D</sub> = -1 mA, V <sub>DS</sub> = -10 V
Static drain to source on state resistance	R <sub>DS (on)</sub>	—	0.017	0.022	Ω	I <sub>D</sub> = -25 A, V <sub>GS</sub> = -10 V <sup>Note 4</sup>
	R <sub>DS (on)</sub>	—	0.024	0.036	Ω	I <sub>D</sub> = -25 A, V <sub>GS</sub> = -4 V <sup>Note 4</sup>
Forward transfer admittance	y <sub>fs</sub>	27	39	—	S	I <sub>D</sub> = 25 A, V <sub>DS</sub> = 10 V <sup>Note 4</sup>
Input capacitance	C <sub>iss</sub>	—	4100	—	pF	V <sub>DS</sub> = -10 V
Output capacitance	C <sub>oss</sub>	—	2100	—	pF	V <sub>GS</sub> = 0
Reverse transfer capacitance	C <sub>rss</sub>	—	450	—	pF	f = 1 MHz
Turn-on delay time	t <sub>d (on)</sub>	—	32	—	ns	V <sub>GS</sub> = -10 V
Rise time	t <sub>r</sub>	—	225	—	ns	I <sub>D</sub> = -25 A
Turn-off delay time	t <sub>d (off)</sub>	—	530	—	ns	R <sub>L</sub> = 1.2 Ω
Fall time	t <sub>f</sub>	—	330	—	ns	
Body to drain diode forward voltage	V <sub>DF</sub>	—	-1.1	—	V	I <sub>F</sub> = -50 A, V <sub>GS</sub> = 0
Body to drain diode reverse recovery time	t <sub>rr</sub>	—	110	—	ns	I <sub>F</sub> = -50 A, V <sub>GS</sub> = 0 di <sub>F</sub> /dt = 50 A/μs

- Note: 4. Pulse test

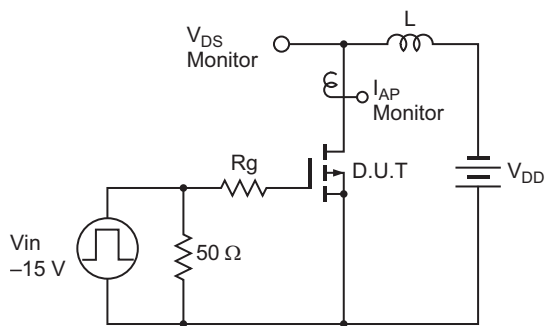
Main Characteristics



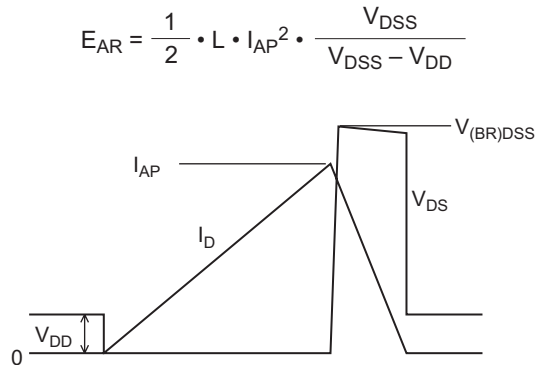




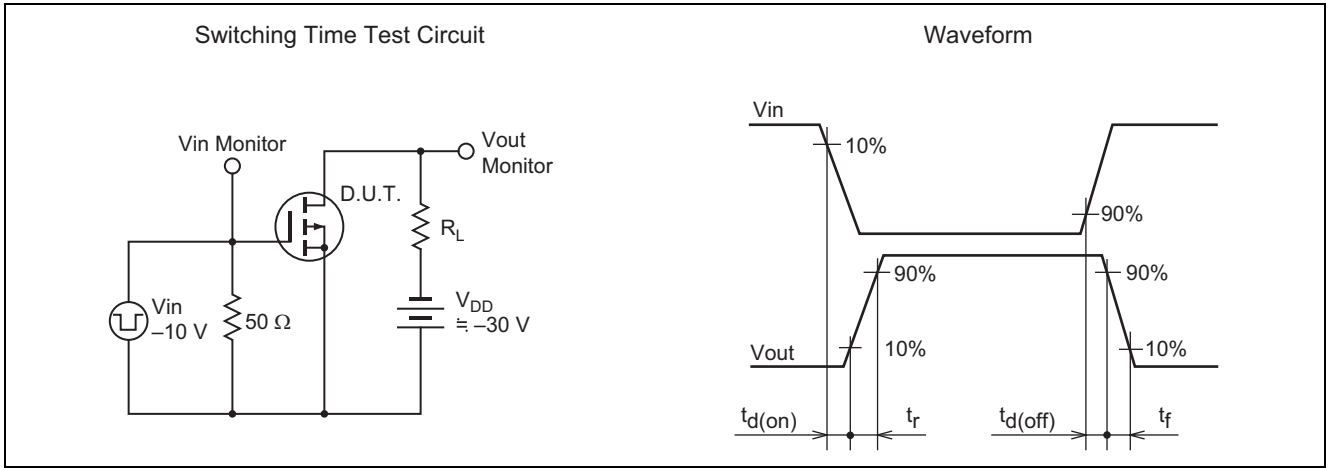
Avalanche Test Circuit



Avalanche Waveform



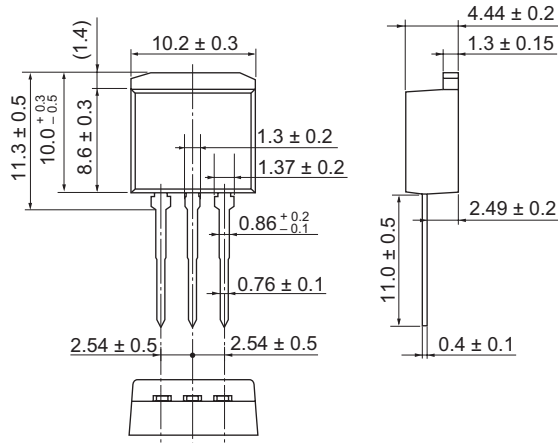
$$E_{AR} = \frac{1}{2} \cdot L \cdot I_{AP}^2 \cdot \frac{V_{DSS}}{V_{DSS} - V_{DD}}$$



Package Dimensions

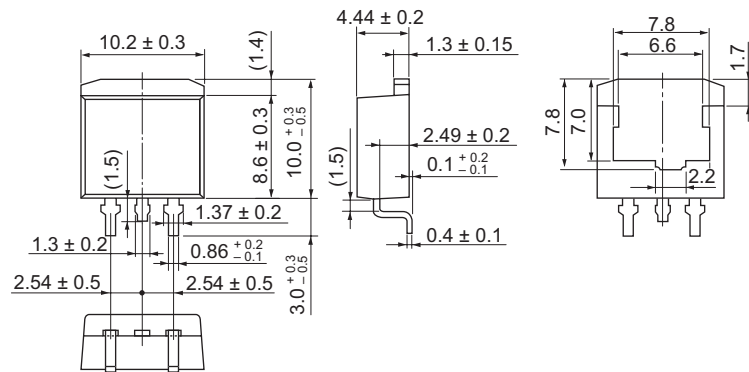
Package Name	JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
LDBPAK(L)	—	PRSS0004AE-A	LDBPAK(L) / LDBPAK(L)V	1.40g

Unit: mm



Package Name	JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
LDBPAK(S)-(1)	SC-83	PRSS0004AE-B	LDBPAK(S)-(1) / LDBPAK(S)-(1)V	1.30g

Unit: mm



### Ordering Information

Part Name	Quantity	Shipping Container
2SJ505L-E	500 pcs	Box (Sack)
2SJ505STL-E	1000 pcs	Taping

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