To our customers,

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April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

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RENESAS

# MOS FIELD EFFECT TRANSISTOR

Phase-out/Discontinued

# 2SJ492

## SWITCHING
## P-CHANNEL POWER MOS FET

### DESCRIPTION

This product is P-Channel MOS Field Effect Transistor designed for DC/DC converters and motor/lamp driver circuits.

### FEATURES

- Low on-state resistance
  $R_{DS(on)1}$ = 100 mΩ MAX. ($V_{GS}$ = –10 V, $I_D$ = –10 A)
  $R_{DS(on)2}$ = 185 mΩ MAX. ($V_{GS}$ = –4 V, $I_D$ = –10 A)
- Low input capacitance
  $C_{iss}$ = 1210 pF TYP.
- Built-in gate protection diode

### ORDERING INFORMATION

| PART NUMBER | PACKAGE |
|---|---|
| 2SJ492 | TO-220AB (MP-25) |
| 2SJ492-S | TO-262 (MP-25 Fin Cut) |
| 2SJ492-ZJ | TO-220SMD (MP-25ZJ) |

### ABSOLUTE MAXIMUM RATINGS ($T_A$ = 25°C)

| | | | |
|---|---|---|---|
| Drain to Source Voltage ($V_{GS}$ = 0 V) | $V_{DSS}$ | –60 | V |
| Gate to Source Voltage ($V_{DS}$ = 0 V) | $V_{GSS(AC)}$ | ∓20 | V |
| Gate to Source Voltage ($V_{DS}$ = 0 V) Note1 | $V_{GSS(DC)}$ | –20, 0 | V |
| Drain Current (DC) | $I_{D(DC)}$ | ∓20 | A |
| Drain Current (pulse) Note2 | $I_{D(pulse)}$ | ∓80 | A |
| Total Power Dissipation ($T_C$ = 25°C) | $P_{T1}$ | 70 | W |
| Total Power Dissipation ($T_A$ = 25°C) | $P_{T2}$ | 1.5 | W |
| Channel Temperature | $T_{ch}$ | 150 | °C |
| Storage Temperature | $T_{stg}$ | –55 to +150 | °C |
| Single Avalanche Current Note3 | $I_{AS}$ | –20 | A |
| Single Avalanche Energy Note3 | $E_{AS}$ | 40 | mJ |

**Notes 1.** f = 20 kHz, Duty Cycle ≤ 10% (+Side)

**2.** PW ≤ 10 μs, Duty Cycle ≤ 1 %

**3.** Starting $T_{ch}$ = 25°C, $V_{DD}$ = –30 V, $R_G$ = 25 Ω, $V_{GS}$ = –20 → 0 V

### THERMAL RESISTANCE

| | | | |
|---|---|---|---|
| Channel to Case Thermal Resistance | $R_{th(ch-C)}$ | 1.79 | °C/W |
| Channel to Ambient Thermal Resistance | $R_{th(ch-A)}$ | 83.3 | °C/W |



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Printed in Japan

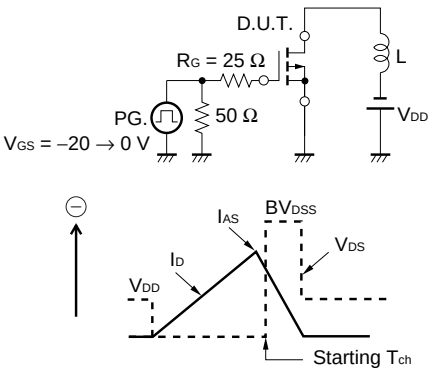


**The mark <R> shows major revised points.**
**The revised points can be easily searched by copying an "<R>" in the PDF file and specifying it in the "Find what:" field.**

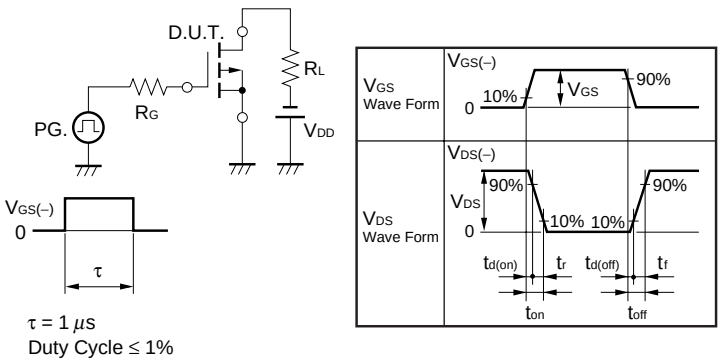
## ELECTRICAL CHARACTERISTICS ($T_A$ = 25°C)

| CHARACTERISTICS | SYMBOL | TEST CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| Drain Leakage Current | $I_{DSS}$ | $V_{DS}$ = –60 V, $V_{GS}$ = 0 V | | | –10 | μA |
| Gate to Source Leakage Current | $I_{GSS}$ | $V_{GS}$ = ∓20 V, $V_{DS}$ = 0 V | | | ∓10 | μA |
| Gate to Source Cut-off Voltage | $V_{GS(off)}$ | $V_{DS}$ = –10 V, $I_D$ = –1 mA | –1.0 | –1.5 | –2.0 | V |
| Forward Transfer Admittance | $\|y_{fs}\|$ | $V_{DS}$ = –10 V, $I_D$ = –10 A | 5.0 | 12 | | S |
| Drain to Source On-state Resistance | $R_{DS(on)1}$ | $V_{GS}$ = –10 V, $I_D$ = –10 A | | 70 | 100 | mΩ |
| | $R_{DS(on)2}$ | $V_{GS}$ = –4 V, $I_D$ = –10 A | | 120 | 185 | mΩ |
| Input Capacitance | $C_{iss}$ | $V_{DS}$ = –10 V, | | 1210 | | pF |
| Output Capacitance | $C_{oss}$ | $V_{GS}$ = 0 V, | | 520 | | pF |
| Reverse Transfer Capacitance | $C_{rss}$ | f = 1 MHz | | 180 | | pF |
| Turn-on Delay Time | $t_{d(on)}$ | $I_D$ = –10 A, | | 16 | | ns |
| Rise Time | $t_r$ | $V_{GS}$ = –10 V, | | 140 | | ns |
| Turn-off Delay Time | $t_{d(off)}$ | $V_{DD}$ = –30 V, | | 90 | | ns |
| Fall Time | $t_f$ | $R_G$ = 10 Ω | | 80 | | ns |
| Total Gate Charge | $Q_G$ | $I_D$ = –20 A, | | 42 | | nC |
| Gate to Source Charge | $Q_{GS}$ | $V_{DD}$ = –48 V, | | 8.0 | | nC |
| Gate to Drain Charge | $Q_{GD}$ | $V_{GS}$ = –10 V | | 10 | | nC |
| Body Diode Forward Voltage | $V_{F(S-D)}$ | $I_F$ = –20 A, $V_{GS}$ = 0 V | | 1.0 | | V |
| Reverse Recovery Time | $t_{rr}$ | $I_F$ = –20 A, $V_{GS}$ = 0 V, | | 125 | | ns |
| Reverse Recovery Charge | $Q_{rr}$ | di/dt = 50 A/μs | | 280 | | nC |

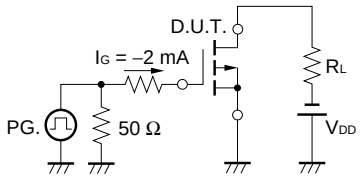
### TEST CIRCUIT 1 AVALANCHE CAPABILITY




### TEST CIRCUIT 2 SWITCHING TIME

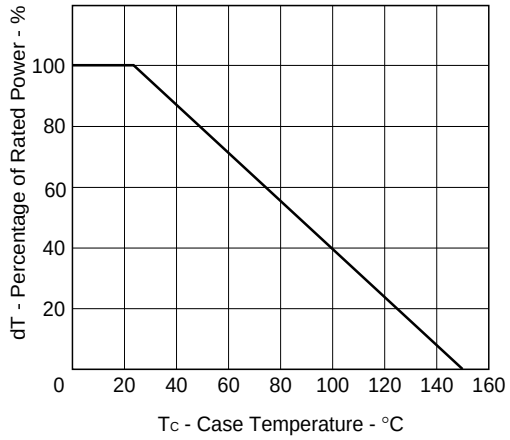



### TEST CIRCUIT 3 GATE CHARGE

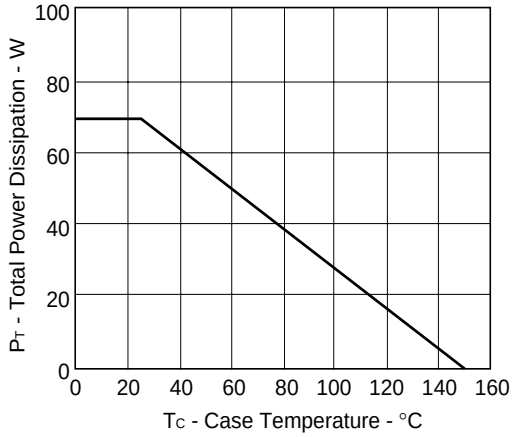


## TYPICAL CHARACTERISTICS ($T_A$ = 25°C)

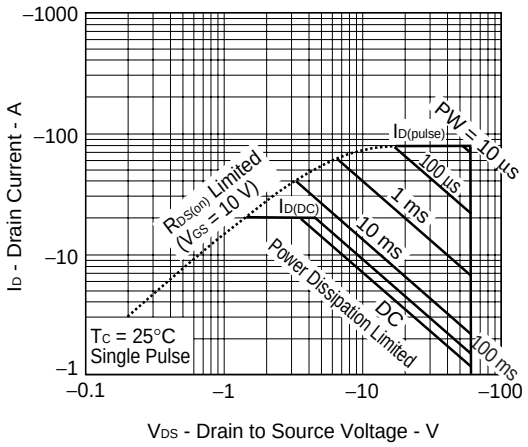
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



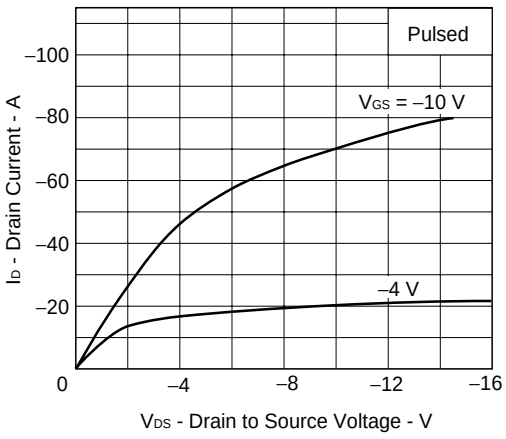

<R> TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



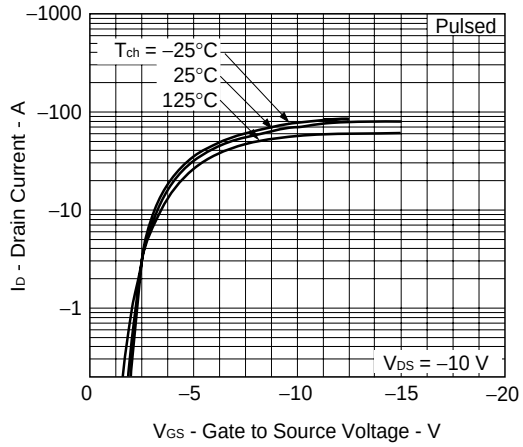

FORWARD BIAS SAFE OPERATING AREA



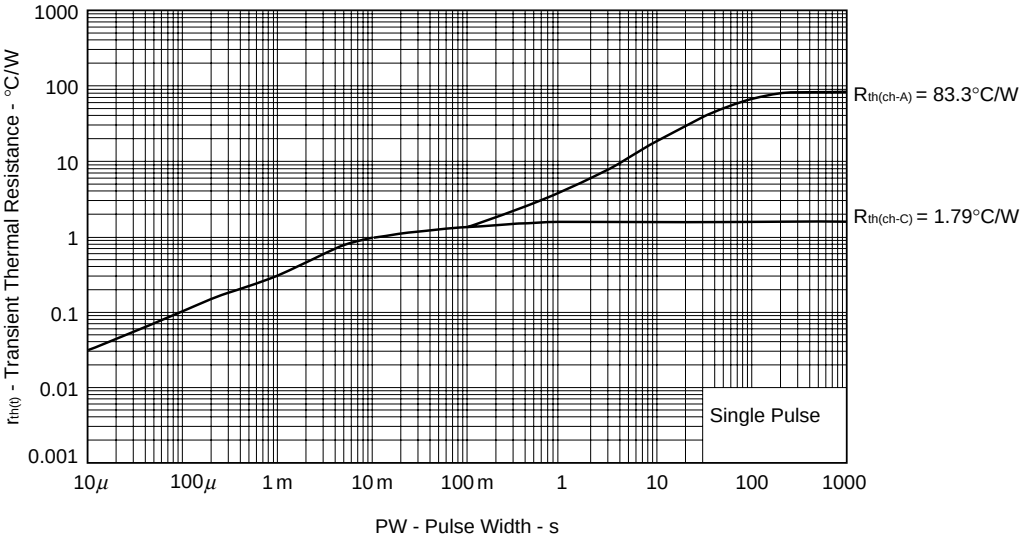

DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



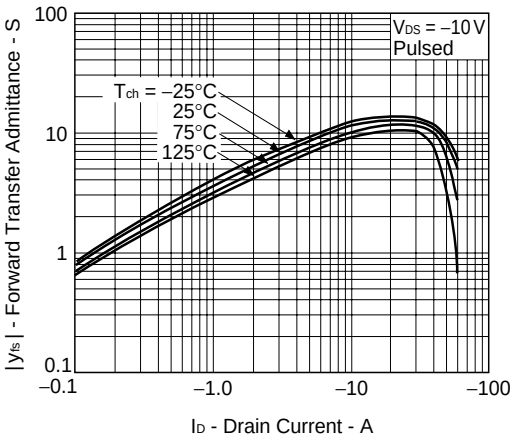

FORWARD TRANSFER CHARACTERISTICS



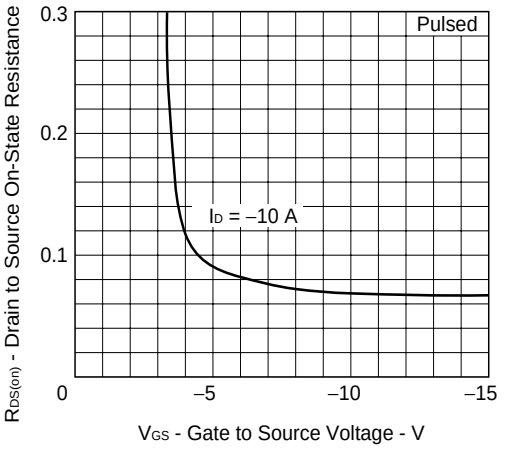
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



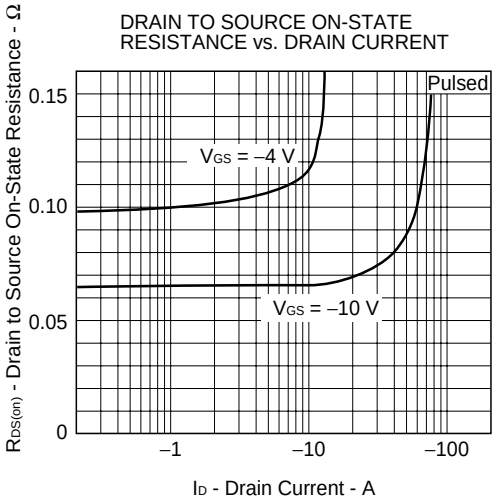

FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



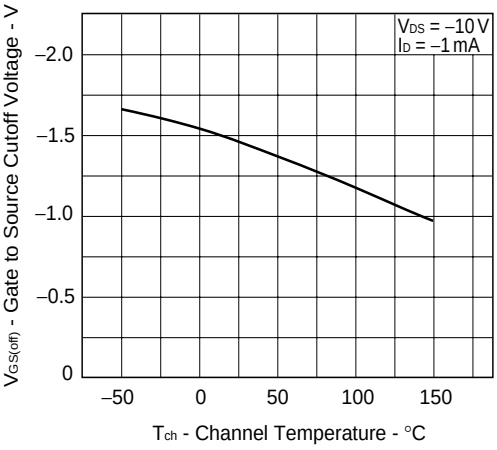

DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



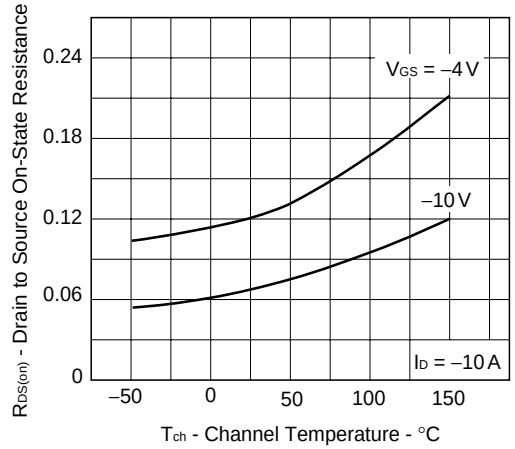

DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



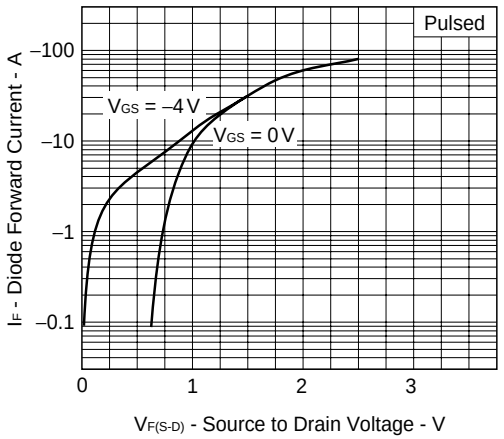

GATE TO SOURCE CUTOFF VOLTAGE vs. CHANNEL TEMPERATURE



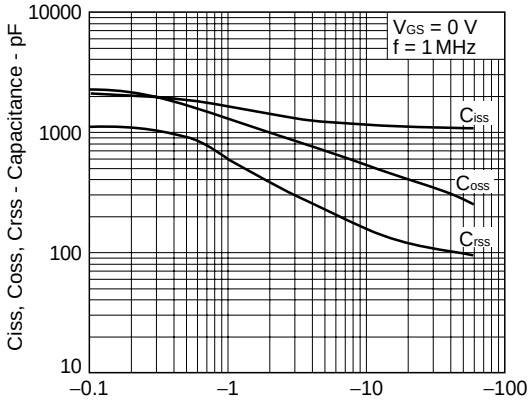
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



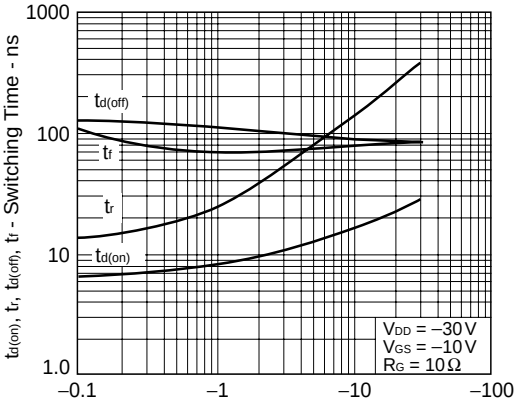

SOURCE TO DRAIN DIODE FORWARD VOLTAGE



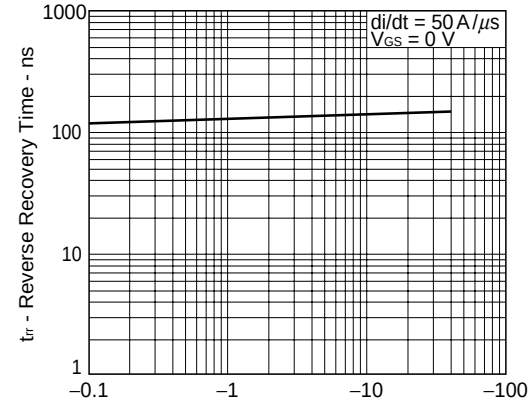

CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



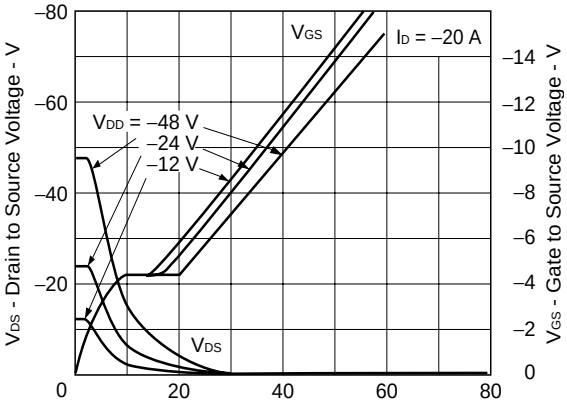

SWITCHING CHARACTERISTICS



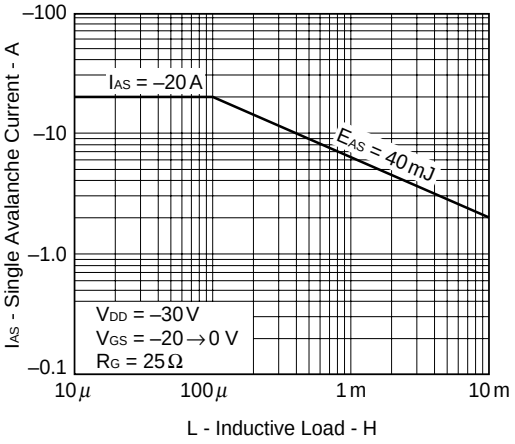

REVERSE RECOVERY TIME vs. DIODE FORWARD CURRENT



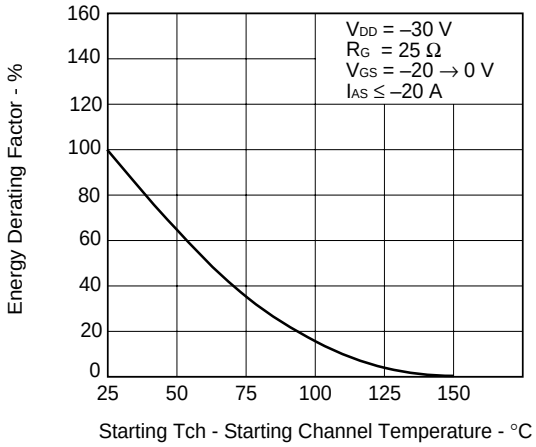

DYNAMIC INPUT/OUTPUT CHARACTERISTICS



SINGLE AVALANCHE CURRENT vs.
INDUCTIVE LOAD

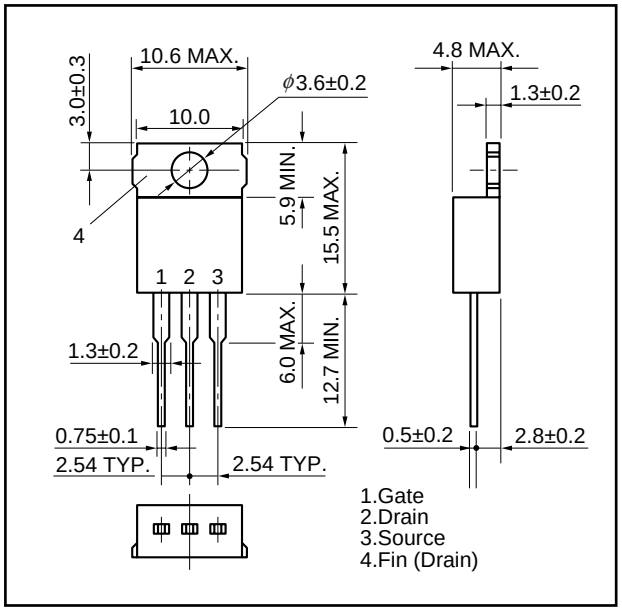



SINGLE AVALANCHE ENERGY
DERATING FACTOR

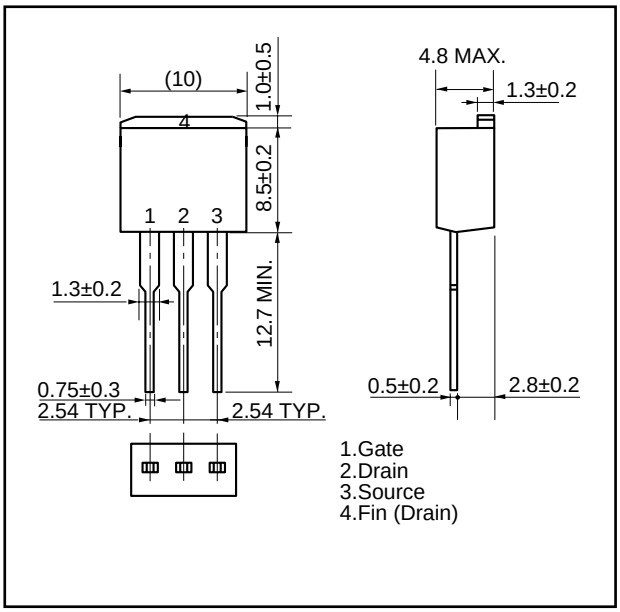


**PACKAGE DRAWING (Unit: mm)**

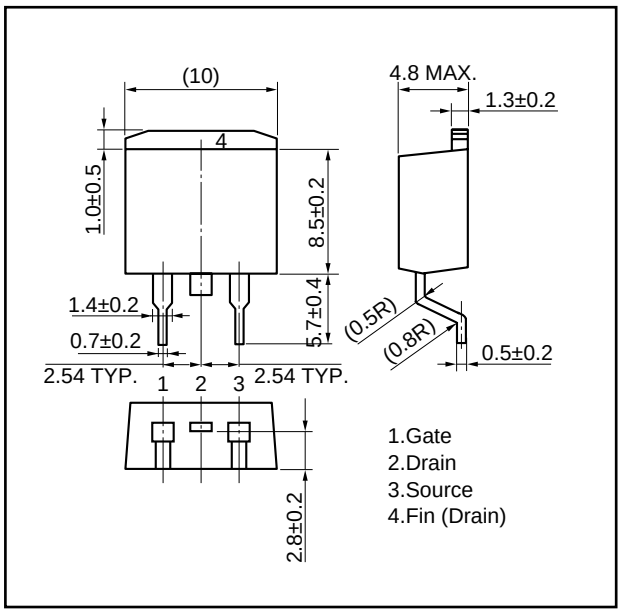
**1) TO-220AB (MP-25)**



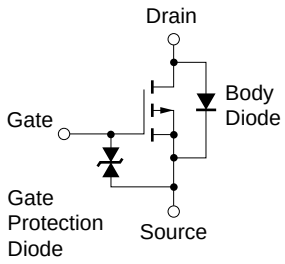

**2) TO-262 (MP-25 Fin Cut)**




**3) TO-263 (JEDEC TYPE: MP-25ZJ)**




**EQUIVALENT CIRCUIT**




**Remark** The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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