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DATA SHEET

RENESAS

MOS INTEGRATED CIRCUIT

μPD70F3178(A)

V850E/CG3™ CarGate+
32-Bit Flash Microcontroller

DESCRIPTION

The V850E/CG3 ("CarGate+") Flash microcontroller, is a member of NEC's V850 32-bit RISC family, which match the performance gains attainable with RISC-based controllers to the needs of embedded control applications. The V850 CPU offers easy pipeline handling and programming, resulting in compact code size comparable to 16-bit CISC CPUs.
The V850E/CG3 ("CarGate+") is especially designed for the high performance requirements of sophisticated algorithms and calculations. It combines a powerful CPU-Core with a 16-bit wide external memory interface and embedded Flash. Furthermore, it offers an excellent combination of general purpose peripheral functions, like serial communication interfaces (UART, clocked SI and I²C) and measurement inputs (A/D converter), with dedicated CAN network support.
Thus equipped, the V850E/CG3 ("CarGate+") is ideally suited for automotive applications, like CAN Gateways. It is also an excellent choice for other applications where a combination of sophisticated peripheral functions and CAN network support is required.

Functions in detail are described in the following user's manual. Be sure to read these manual when you design your systems.

V850E/CG3 CarGate+ Preliminary User's Manual: U16881EE1V0UM00

FEATURES

- 32-bit RISC CPU with Harvard Architecture
- 256 kB Flash, 12 kB RAM
- Full-CAN Interface: 5 channels
- Serial Interfaces: 6 channels
  - 3-wire mode: 3 channels
  - UART mode: 2 channels
  - I²C mode: 1 channel
- Timers: 3 channels
  - 16-bit multi purpose timer/event counter: channels: 3 channels
- 10-bit resolution A/D Converter: 4 channels
- Non-Multiplexed External Bus Interface (16-/8-bit data / 20-bit address)
- I/O lines: max. 80
- Power supply voltage range:
  - +4.3 V ≤ V_{DD5} ≤ +5.5 V
- Frequency range: up to 32 MHz
- Built-in low power saving mode
- Built-in clock oscillator circuit with internal PLL
- Temperature range:
  - -40 °C to +85 °C
- Package:
  - 100 LQFP, 0.5 mm pin-pitch (14 × 14 mm)

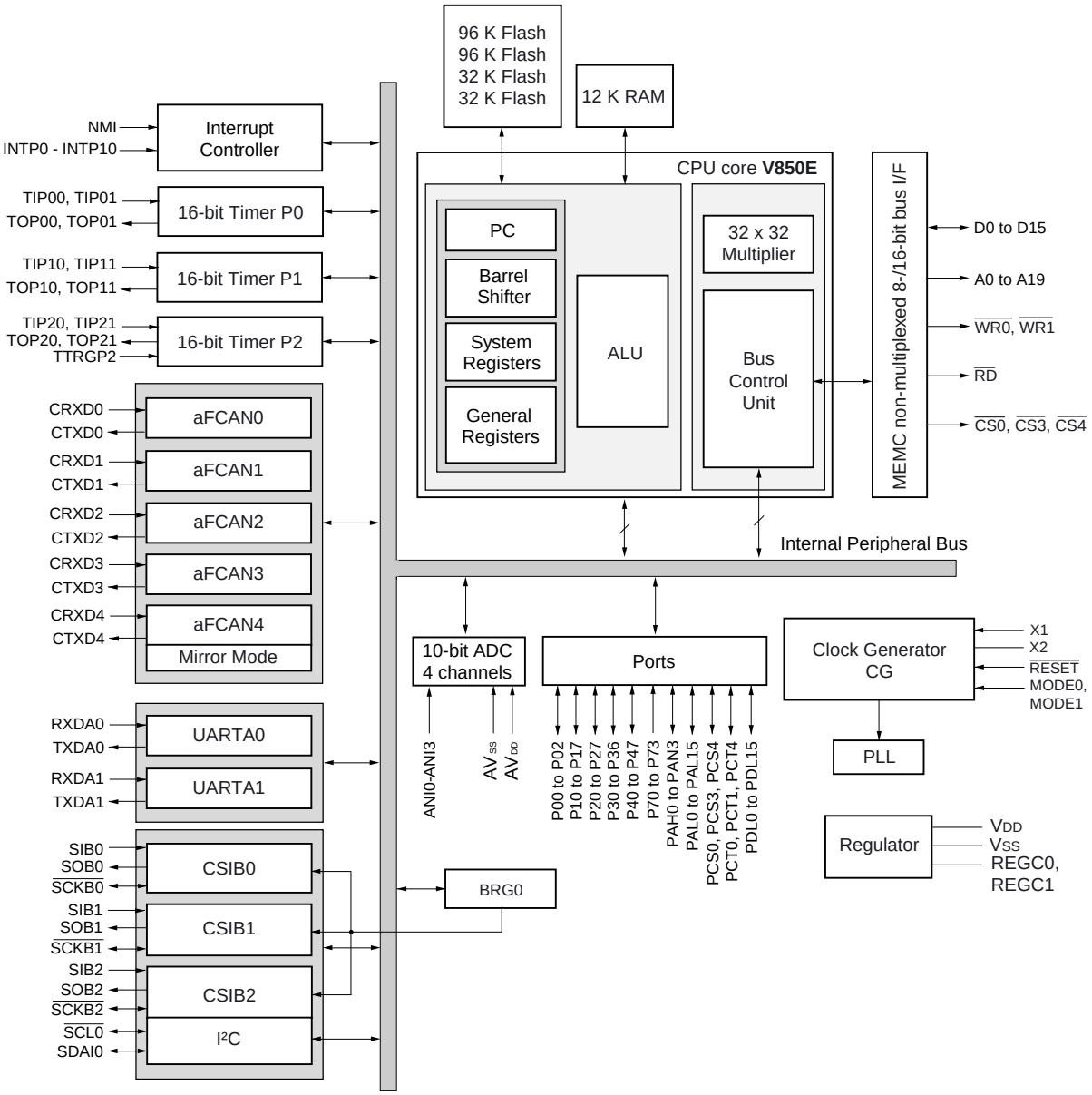
ORDERING INFORMATION

Device	Part Number	Package	ROM	RAM	FCAN Option	Operating Temperature (T_A)
V850E/CG3	μPD70F3178(A)	LQFP100 14 × 14 mm	256 kB Flash	12 kB	5 Channels	-40°C ~ +85°C

The information contained in this document is released in advance of the production cycle for the device. The parameters for the device may change before final production, or NEC Corporation may, at its own discretion, withdraw the device prior to production.

Document No. U17344EE1V1DS00
Data Published: February 2005

INTERNAL BLOCK DIAGRAM

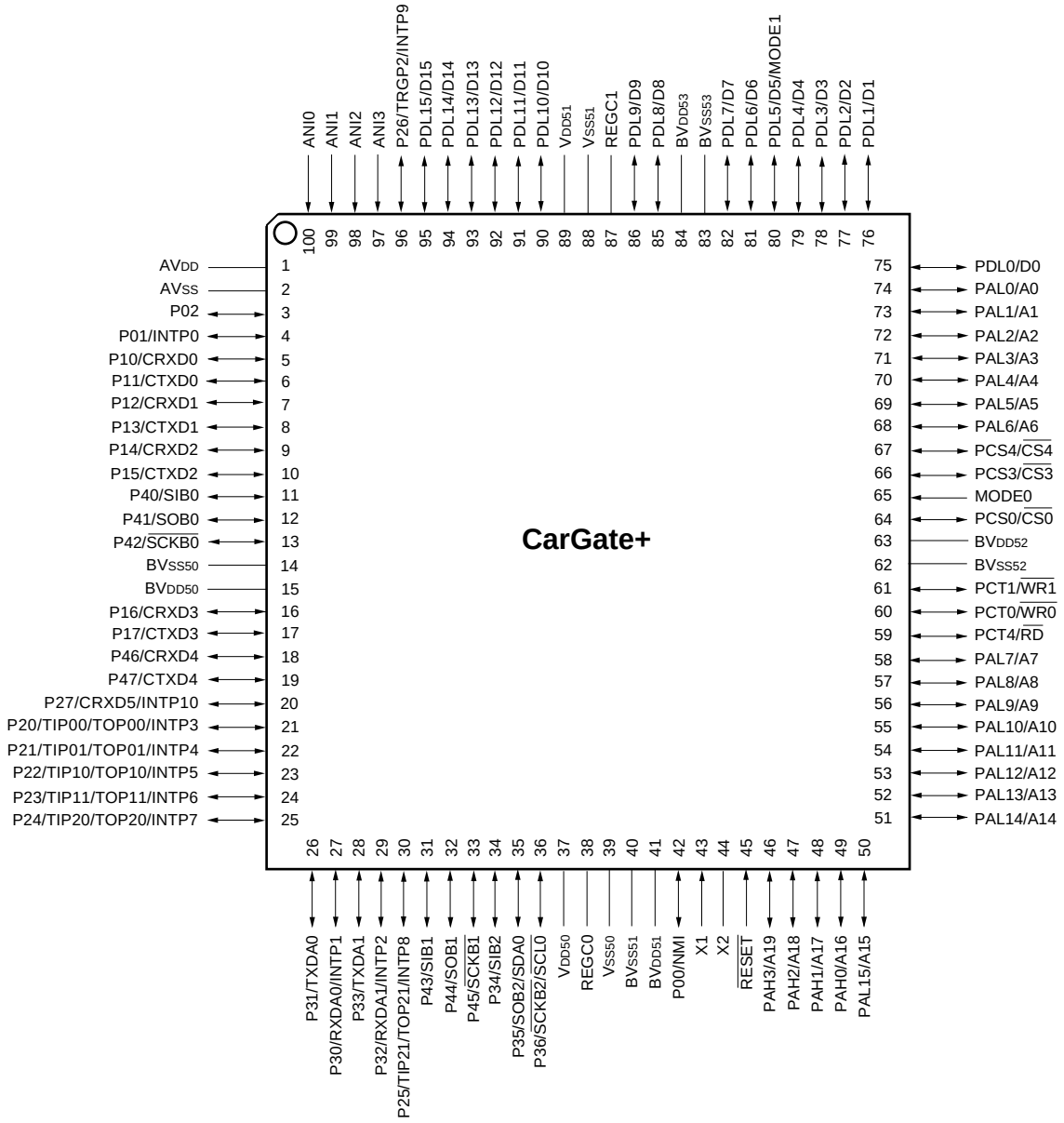


PIN IDENTIFICATION

A0 to A19 : Address Bus
D0 to D15 : Data Bus
ANI0 to ANI3 : Analog Input
AV_{DD} : Analog Power Supply
AV_{SS} : Analog Ground
CRXD0 to CRXD5 : CAN Receive Line Input
CTXD0 to CTXD4 : CAN Transmit Line Output
CV_{DD} : Clock Generator Power Supply
CV_{SS} : Clock Generator Ground
$BVSS_{50}$ to $BVSS_{53}$ Ground for 5 V Power Supply
VSS_{50} to VSS_{51} Ground for 5 V Power Supply
INTP0 to INTP10 External interrupt request
INTPn0, INTPn5, INTP2n : Interrupt Request from Peripherals
MODE0, MODE1 : Mode Inputs
NMI : Non-Maskable Interrupt Request
P00 to P02 Port 0
P10 to P17 : Port 1
P20 to P27 : Port 2
P30 to P36 : Port 3
P40 to P47 : Port 4
P70 to P73 Port 7
PAH0 to PAH3 : Port AH
PAL0 to PAL 15 Port AL
PCS0, PCS3, PCS4 : Port CS
PCT0, PCT1, PCT4 : Port CT
PDL0 to PDL15 Port PDL
$\overline{RESET}$: Reset
RXDA0 to RXDA1 : UART Receive Data Input
$\overline{SCKB0}$, $\overline{SCKB1}$, $\overline{SCKB2}$: Serial Clock
$\overline{SCL}$ I^2C Clock
SDA I^2C Data
SIB0, SIB1, SIB2 : Serial Input
SOB0, SOB1, SOB2 : Serial Output
TIP00 to TIP01, TIP10 to TIP11, TIP20 to TIC21 : Timer Input
TOP00 to TOP01, TOP10 to TOP11, TOP20 to TOP21 Timer Output
TXDA0 to TXDA1 : Transmit Data Output
TTRGP2 Timer Trigger Input
BV_{DD50} to BV_{DD53} : 5 V Power Supply
V_{DD50} to V_{DD51} : 5 V Power Supply
$\overline{WR0}$, $\overline{WR1}$ Write Enable
$\overline{RD}$: Read
$\overline{CS0}$, $\overline{CS3}$, $\overline{CS4}$ Chip Select
X1, X2 : Crystal (Main-OSC)

PIN CONFIGURATION (Top View)

100-Pin Plastic LQFP (fine pitch) (14 mm × 14 mm)



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1. Pin Functions

(1) Port pins

Table 1-1: Pin Functions (1/3)

Port	I/O	Function	Alternate
P00	I/O	Port 0 3-bit input/output port	NMI (I)
P01			INTP0 (I)
P02			
P10	I/O	Port 1 8-bit input/output port	CRXD0 (I)
P11			CTXD0 (O)
P12			CRXD1 (I)
P13			CTXD1 (O)
P14			CRXD2 (I)
P15			CTXD2 (O)
P16			CRXD3 (I)
P17			CTXD3 (O)
P20	I/O	Port 2 8-bit input/output port	TOP00 (O) TIP00 (I) INTP3 (I) CRXD4 (I)
P21			INTP4 (I) TOP01 (O) TIP01 (I)
P22			INTP5 (I) TOP10 (O) TIP10 (I)
P23			INTP6 (I) TOP11 (O) TIP11 (I)
P24			INTP7 (I) TOP20 (O) TIP20 (I)
P25			INTP8 (I) TOP21 (O) TIP21 (I)
P26			TTRGP2 (I) INTP9 (I)
P27			INTP10 (I)
P30	I/O	Port 3 7-bit input/output port	RXDA0 (I) INTP1 (I)
P31			TXDA0 (O)
P32			RXDA1 (I) INTP2 (I)
P33			TXDA1 (O)
P34			SIB2 (I)
P35			SDAO0 (O) SDAI0 (I) SOB2 (O)
P36			SCLO0 (O) SCKIB2 (I) SCLI0 (I) SCKOB2 (O)
P40	I/O	Port 4 8-bit input/output port	SIB0 (I)
P41			SOB0 (O)
P42			SCKIB0 (I) SCKOB0 (O)
P43			SIB1 (I)
P44			SOB1 (O)
P45			SCKIB1 (I) SCKOB1 (O)
P46			CRXD4 (I)
P47			CTXD4 (O)

Table 1-1: Pin Functions (2/3)

Port	I/O	Function	Alternate
PAH0	I/O	Port PAH 4-bit input/output	A16 (O)
PAH1			A17 (O)
PAH2			A18 (O)
PAH3			A19 (O)
PAL0	I/O	Port PAL 16-bit input/output	A0 (O)
PAL1			A1 (O)
PAL2			A2 (O)
PAL3			A3 (O)
PAL4			A4 (O)
PAL5			A5 (O)
PAL6			A6 (O)
PAL7			A7 (O)
PAL8			A8 (O)
PAL9			A9 (O)
PAL10			A10 (O)
PAL11			A11 (O)
PAL12			A12 (O)
PAL13			A13 (O)
PAL14			A14 (O)
PAL15			A15 (O)
PCS0	I/O	Port PCS 3-bit input/output	$\overline{CS0}$ (O)
PCS3			$\overline{CS3}$ (O)
PCS4			$\overline{CS4}$ (O)
PCT0	I/O	Port PCT 3-bit input/output	$\overline{WR0}$ (O)
PCT1			$\overline{WR1}$ (O)
PCT4			$\overline{RD}$ (O)

Table 1-1: Pin Functions (3/3)

Port	I/O	Function	Alternate
PDL0	I/O	Port PDL 16-bit input/output	DO0 (O) DI0 (I)
PDL1			DO1 (O) DI1 (I)
PDL2			DO2 (O) DI2 (I)
PDL3			DO3 (O) DI3 (I)
PDL4			DI4 (I) DO4 (O)
PDL5			DI5 (I) DO5 (O) MODE1 (I)
PDL6			DI6 (I) DO6 (O)
PDL7			DI7 (I) DO7 (O)
PDL8			DO8 (O) DI8 (I)
PDL9			DO9 (O) DI9 (I)
PDL10			DI10 (I) DO10 (O)
PDL11			DI11 (I) DO11 (O)
PDL12			DO12 (O) DI12 (I)
PDL13			DO13 (O) DI13 (I)
PDL14			DI14 (I) DO14 (O)
PDL15			DI15 (I) DO15 (O)

(2) Non-port pins

Table 1-2: Non-Port Pins (1/2)

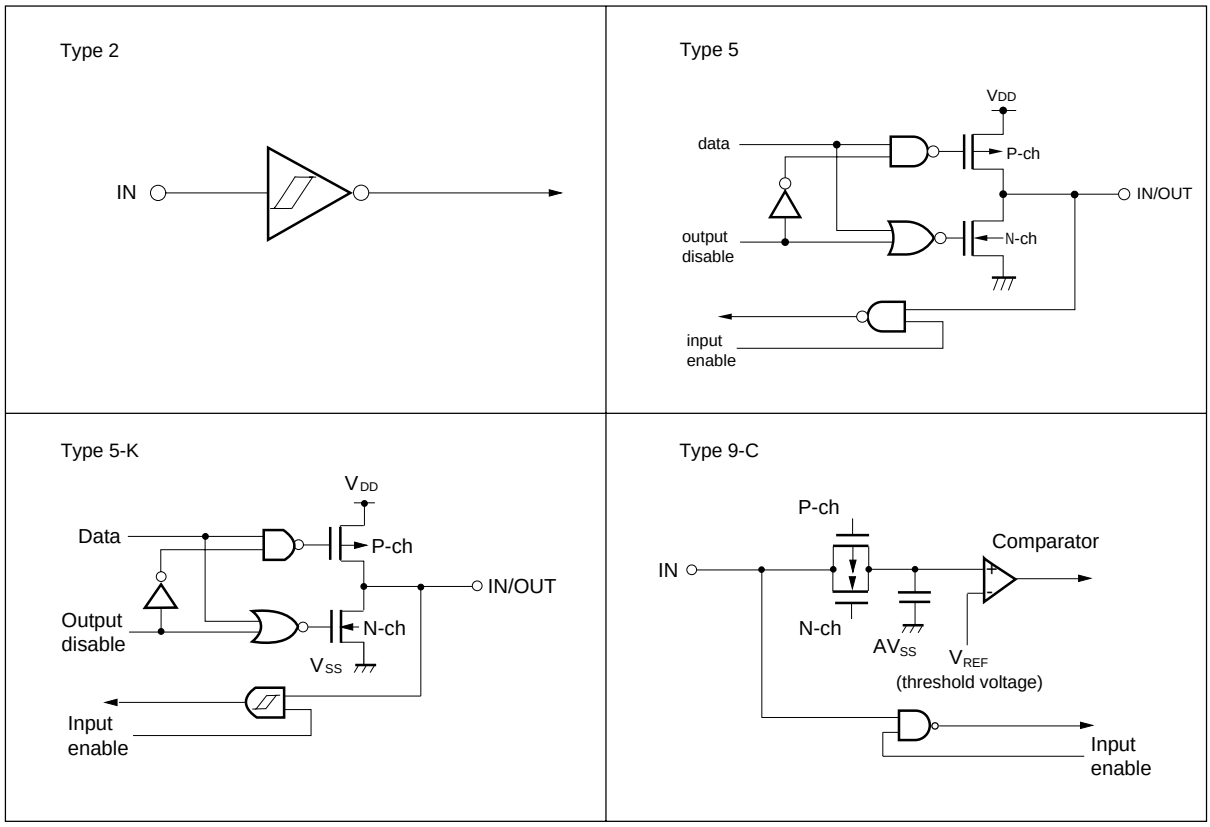
Pin Name	I/O	Function	Port
A0 - A15	O	Address bus of external bus	PAL0 - PAL15
A16 - A19	O		PAH0 -PAH3
AIN0 - AIN3	I	Analog input for A/D converter	
CRXD0	I	Serial receive data input for aFCAN0 to aFCAN4	P10
CRXD1	I		P12
CRXD2	I		P14
CRXD3	I		P16
CRXD4	I		P46
CRXD5	I	Additional Receive Input for Mirror Mode	P20
$\overline{CS0}$	O	Chip select output for external bus	PCS0
$\overline{CS3}$	O		PCS3
$\overline{CS4}$	O		PCS4
CTXD0	O	Serial transmit data for aFCAN0 to aFCAN4	P11
CTXD1	O		P13
CTXD2	O		P15
CTXD3	O		P17
CTXD4	O		P47
D0 - D15	I/O	Data bus of external bus	PDL0 - PDL15
INTP0	I	External interrupt request	P01
INTP1	I		P30
INTP2	I		P32
INTP3	I		P20
INTP4	I		P21
INTP5	I		P22
INTP6	I		P23
INTP7	I		P24
INTP8	I		P25
INTP9	I		P26
INTP10	I		P27
NMI	I	Non maskable interrupt	P00
$\overline{RD}$	O	Read strobe signal	PCT4
RXDA0	I	Serial receive data UARTA0 & UARTA1	P30
RXDA1	I		P32
SCKB0	I/O	Serial clock I/O from CSIB0 - CSIB2	P42
SCKB1	I/O		P45
SCKB2	I/O		P36
SCL0	I/O	Serial clock line I²C	P36
SDAI0	I/O	Serial data line I²C	P35

Table 1-2: Non-Port Pins (2/2)

Pin Name	I/O	Function	Port
SIB0	I	Serial data input CSIB0 - CSIB2	P40
SIB1	I		P43
SIB2	I		P34
SOB0	O	Serial data output CSIB0- CSIB2	P41
SOB1	O		P44
SOB2	O		P35
TIP00	I	Capture input 0-1 Timer P0 - Timer P2	P20
TIP01	I		P21
TIP10	I		P22
TIP11	I		P23
TIP20	I		P24
TIP21	I		P25
TOP00	O	Compare output 0-1 Timer P0 - Timer P2	P20
TOP01	O		P21
TOP10	O		P22
TOP11	O		P23
TOP20	O		P24
TOP21	O		P25
TTRGP2	I	Timer Trigger Input Timer P2	P26
TXDA0	O	Serial transmit data output UARTA0 - UARTA1	P31
TXDA1	O		P33
$\overline{WR0}$	O	Write strobe signal for external bus	PCT0
$\overline{WR1}$	O		PCT1
AV_{DD}	–	5 V power supply ADC	–
AV_{SS}	–	GND potential for 5 V power supply ADC	–
V_{DD50}-V_{DD51}	–	5 V power supply	–
BV_{DD50}-BV_{DD53}	–		–
V_{SS50}-V_{SS50}	–	GND potential for 5 V power supply	–
BV_{SS50}-BV_{SS53}	–		–
MODE	I	Specifies Operation mode	–
MODE1	I		PDL5
REGC0	–	Connection of regulator stabilization capacitance	–
REGC1	–		–
$\overline{RESET}$	I	System reset input	–
X1	I	Connection of external oscillator	–
X2	0		–
All V_{DD5} pins have to be connected to each other. On each pin of V_{DD5}, a capacitor containing a very low serial impedance has to be attached as tight as possible to the pin.			

1.1 I/O Circuits

Figure 1-1: Pin I/O Circuits



2. Programming Flash Memory

The device μPD70F3178(A) supports the programming of the internal flash in two ways: Either by using the *flash*PRO4 programming tool or by performing self-programming using software functions and I/O communications.
For programming details about both methods, see the User's Manual. For timing characteristics about the initial programming using *flash*PRO4 and some more electrical data about the Flash Memory, see 3.7 "Flash Memory" on page 30.

3. Electrical Specifications

All electrical parameters which are shown in the following tables are representing target values.

3.1 Absolute Maximum Ratings

(T_A = 25°C, V_{SS5} = 0 V)

Table 3-1: Absolute Maximum Ratings

Parameter		Symbol	Test Conditions	Ratings	Unit
Supply voltage		V_{DD5}		-0.5 ~ +6.5	V
		AV_{DD}		-0.5 ~ +6.5	V
		BV_{DD5}		-0.5 ~ +6.5	V
		BV_{SS5}		-0.5 ~ +0.5	V
		AV_{SS}		-0.5 ~ +0.5	V
Input voltage		V_{I4}	$V_{I4} < BV_{DD5}$ + 0.5 V	-0.5 ~ + 6.5	V
		V_{IA} **Note**	$V_{IA} < AV_{DD}$ + 0.5 V	-0.5 ~ + 6.5	V
Output current low	1 pin	I_{OL4}		4.0	mA
	All pins	I_{OLA}		50	mA
Output current high	1 pin	I_{OH4}		-4.0	mA
	All pins	I_{OHA}		-50	mA
Output voltage		V_O	$V_O < BV_{DD5}$ +0.5 V	-0.5 ~ +6.5	V
Operating temperature (ambient)		T_{OPR}		-40 ~ +85	°C
Storage temperature		T_{STGB}		-40 ~ +125	°C

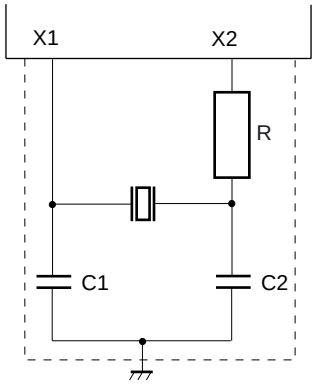
Note: V_{IA} is the voltage applied to the analog input pins P73…P70

Remark: V_{DD5} is the supply voltage for the internal voltage regulators applied to pins V_{DD5x}.
A_{VDD} is the supply and reference voltage for analog part of the A/D converter
BV_{DD5} is the supply voltage for the I/O buffers applied to pins BV_{DD5x}
V_{SS5} is the ground for the internal logic applied to pins V_{SS5x}
A_{VSS} is the ground for the analog part of the A/D converter
BV_{SS5} is the ground for the I/O buffers applied to pins BV_{SS5x}

3.2 General Characteristics

3.2.1 Recommended Main Oscillator circuit

Figure 3-1: Ceramic Resonator or Crystal Resonator Connection



Note: Values of C_1, C_2 and R depend on the used crystal or resonator and must be specified in cooperation with resonator manufacturer.

3.2.2 Oscillator characteristics

(T_A = -40 ~ +85°C, V_{DD5} = BV_{DD5} = 4.3 V ~ 5.5 V, V_{SS5} = BV_{SS5} = 0 V)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Oscillation stabilization time	T_{OST}	OSC MODE			16[Note]	ms

Note: T_{OST} depends on the external crystal and the correct selection of C1, C2 and R.

Remark: This value is valid only for crystal operation.

3.2.3 Peripheral PLL characteristics

(T_A = -40 ~ +85°C, V_{DD5} = BV_{DD} = 4.3 V ~ 5.5 V, V_{SS5} = BV_{SS5} = 0 V)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
PLL start-up time	T_{PST}	OSC MODE			$4800/f_{OSC}$[Note]	μs

Note: f_{OSC} is the oscillator frequency.

3.2.4 I/O capacitances

(T_A = -40 ~ +85°C, V_{DD5} = BV_{DD5} = 4.3 V ~ 5.5 V, V_{SS5} = BV_{SS5} = 0 V)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Input capacitance	C_I	f_C = 1 MHz Unmeasured pins returned to 0 V			10	pF
Input/output capacitance	C_{IO}				10	pF
Output capacitance	C_O				10	pF

3.2.5 Recommended capacitor values for REGC

The recommended capacitor value for REGC0 and REGC1 is 4.7 μF.

Remarks: 1. NEC recommends to use a second capacitor with 100 nF in parallel to reduce disturbances with high frequencies.

2. The terminals REGC0 and REGC1 must not be connected to each other.

3.3 Operating Conditions

3.3.1 CPU clock

(T_A = -40 ~ +85°C, V_{DD5} = BV_{DD5} = AV_{DD} = 4.3 V ~ 5.5 V, V_{SS5} = BV_{SS5} = AV_{SS} = 0 V)

Clock Mode	Operation Mode	Inside Operation Clock Frequency [MHz]
OSC mode, PLL off	all modes C_1 Note 1 = C_2 Note 2 = 4.7 μF	4 to 6
OSC mode, PLL × 4		20 to 24
OSC mode, PLL × 8		32

Notes: 1. C_1 is the external capacitance connected to pin REGC0

2. C_2 is the external capacitance connected to pin REGC1

3.4 DC Characteristics

(T_A = -40 ~ +85°C, V_{DD5} = BV_{DD5} =AV_{DD} = 4.3 V ~ 5.5 V, V_{SS5} = BV_{SS5} = AV_{SS} = 0 V)

Table 3-2: DC Characteristics

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Input voltage high	V_{IH1}	Pin group 1 **Note 1**	0.7 BV_{DD5}		BV_{DD5}	V
Input voltage low	V_{IL1}		0		0.3 BV_{DD5}	V
Input voltage high	V_{IH1}	Pin group 2 **Note 2**	0.7 BV_{DD5}		BV_{DD5}	V
Input voltage low	V_{IL1}		0		0.3 BV_{DD5}	V
P73…P70 Input voltage high	V_{IHA}		0.7 AV_{DD}		AV_{DD}	V
P73…P70 Input voltage low	V_{ILA}		0		0.3 AV_{DD}	V
Output voltage high	V_{OH}	I_{OH} = -3.0 mA	BV_{DD5} - 1			V
Output voltage low	V_{OL}	I_{OL} = 3.0 mA			0.4	V
Input leakage current high	I_{LIH}	V_I = V_{DD5x}			-3	μA
Input leakage current low	I_{LIL}	V_I = 0 V			3	μA
P73…P70 Input leakage current high	I_{LIHA}	V_{IA} = AV_{DD}			-3	μA
P73…P70 Input leakage current low	I_{LILA}	V_{IA} = 0 V			3	μA
Supply current	I_{DD10}	Operating (f_{CPU} = 32 MHz) PLL: on		74	110	mA
	I_{DD11}	Operating (f_{CPU} = 24 MHz) PLL: on		57	90	mA
	I_{DD20}	HALT Mode (f_{PLL} = 32 MHz) PLL: on		45	70	mA
	I_{DD21}	HALT Mode (f_{PLL} = 24 MHz) PLL: on		35	55	mA
	I_{DD30}	IDLE Mode (f_{PLL} = 32 MHz) PLL: on		2.6	4	mA
	I_{DD31}	IDLE Mode (f_{PLL} = 24 MHz) PLL: on		2.6	4	mA
	I_{DD5}	STOP		30	200	μA

Notes: 1. Pin group 1 is PAL, PAH, PDL, PCS, PCT

2. Pin group 2 is P0, P1, P2, P3, P4, P7, MODE, $\overline{\text{RESET}}$

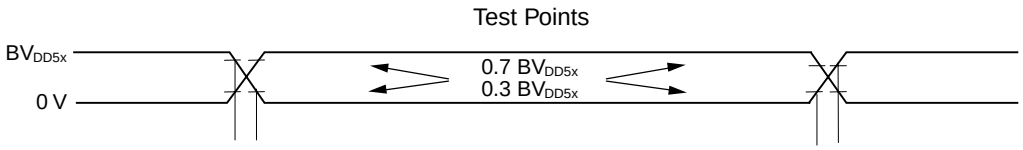
Remark: These values are without consumption of I/O-pins

3.5 AC Characteristics

T_A = -40~ +85°C,
$BV_{DD5} = V_{DD5} = AV_{DD}$ = 4.3V~5.5V, $BV_{SS5} = V_{SS5} = A_{VSS5}$ = 0V,
Output pin load capacitance: C_L= 50 pF

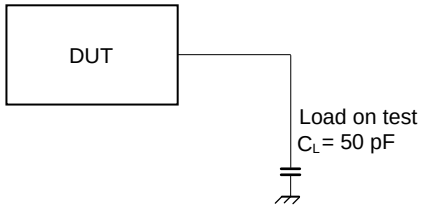
3.5.1 AC test input/output waveform

Figure 3-2: AC Test Input/Output Waveform



3.5.2 AC test load condition

Figure 3-3: AC Test Load Condition



3.5.3 Clock AC characteristics

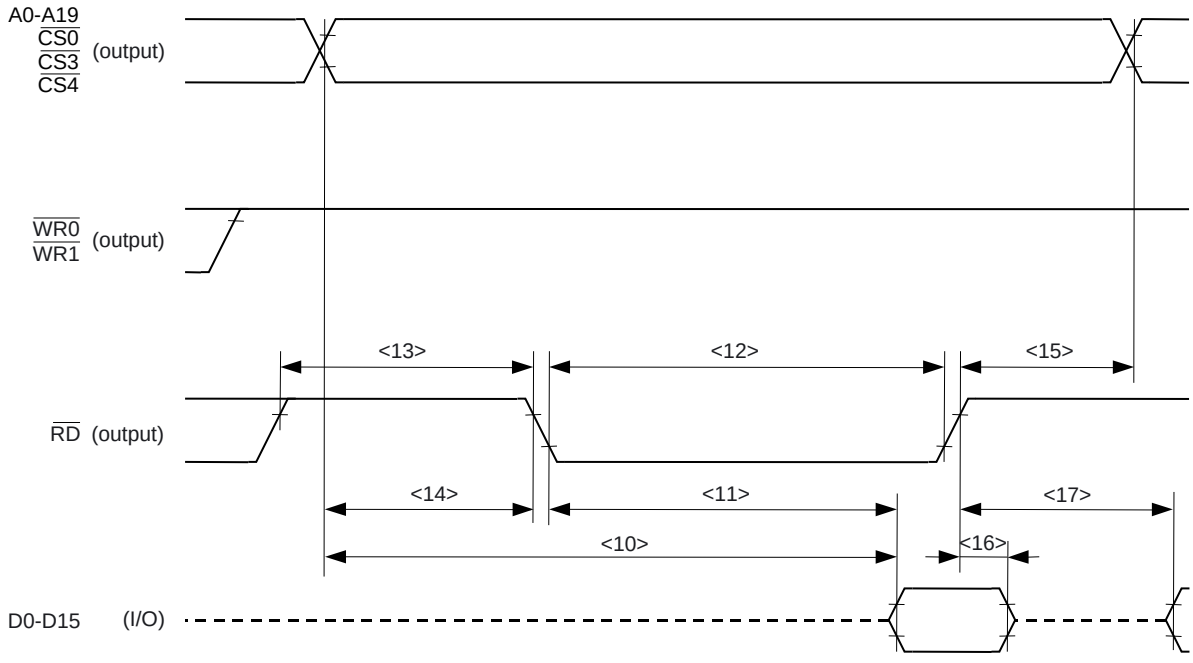
Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
X1, X2 oscillator frequency	f_{OSC}	OSC MODE; PLL × 4	4		6	MHz
		PLL × 8	4		4	MHz

3.5.4 External memory access read timing

Parameter	Symbol		Conditions	Min.	Max	Unit
Data input set up time (vs. address)	<10>	T_{SAID}			$(2+W_T)T - 45$	ns
Data input set up time (vs. $\overline{RD}\downarrow$)	<11>	T_{SRDID}			$(1.5+W_D)T - 40$	ns
$\overline{RD}$ Low level width	<12>	T_{WRDL}		$(1.5+W_D)T - 15$		ns
$\overline{RD}$ High level width	<13>	T_{WRDH}		$(0.5+W_{AS} + iT - 13$		ns
Address, $\overline{CSn}$ $\overline{RD}$ delay time	<14>	T_{DARD}		$(0.5+W_{AS})T - 20$		ns
$\overline{RD}$ address delay time	<15>	T_{DRDA}		iT - 15		ns
Data input hold time (vs. $\overline{RD}\uparrow$)	<16>	T_{HRDID}		0		ns
$\overline{RD}$ data output delay time	<17>	T_{DRDOD}		(0.5+i)T - 35		ns

Note: T : 1 / f_{CPU} (= frequency of system clock)
i : Number of idle states specified by BCC register
W_T : Total Number of waits, $W_T = W_{AS}+W_D$
W_{AS} : Number of waits specified by ASC register
W_D : Number of waits specified by DWC1, DWC2 register

Figure 3-4: SRAM Read Timing

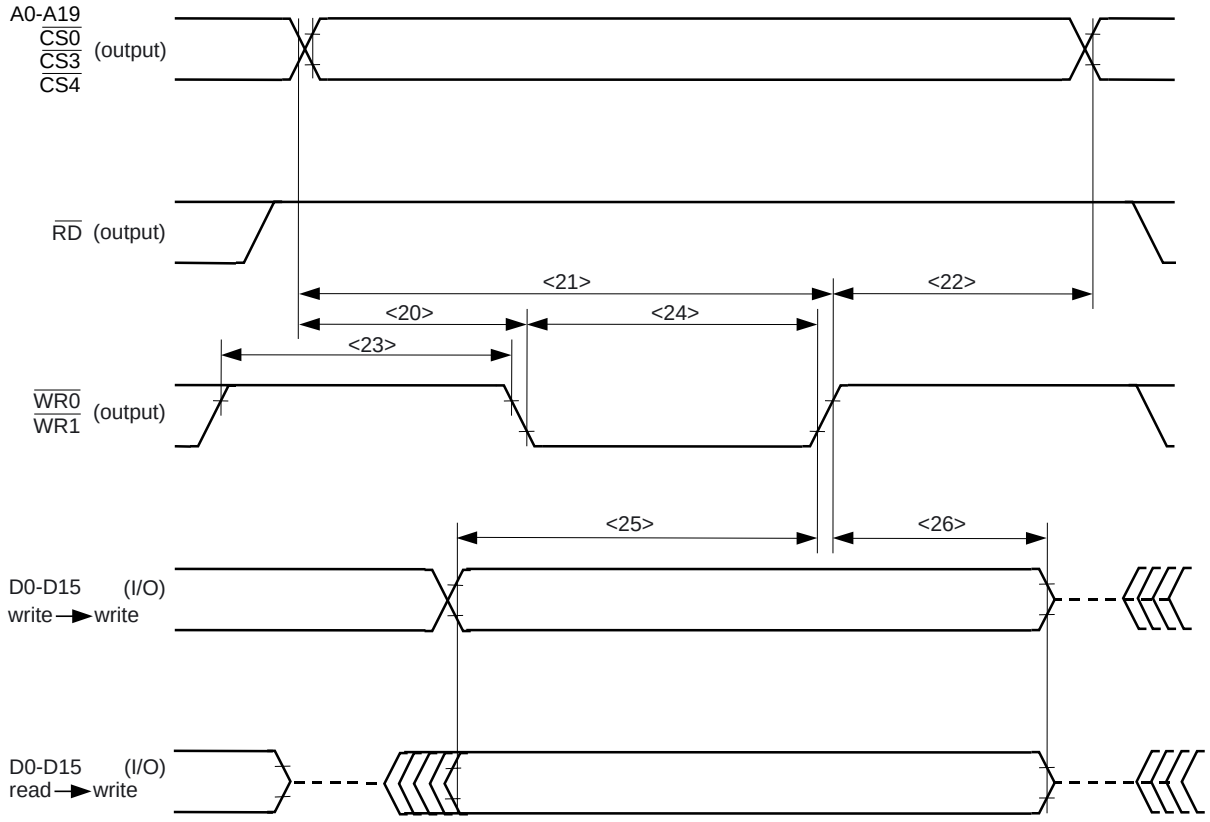


3.5.5 External memory access write timing

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
Address, $\overline{CSn}$ $\overline{WR0}$, $\overline{WR1}$ delay time	<20>	T_{DAWR}		$(0.5+W_{AS})T - 25$		ns
Address set up (vs. $\overline{WR0}$, $\overline{WR1}\uparrow$)	<21>	T_{SAWR}		$(1.5+W_T)T - 20$		ns
$\overline{WR0}$, $\overline{WR1}$ address delay time	<22>	T_{DWRA}		$(0.5+i)T - 15$		ns
$\overline{WR0}$, $\overline{WR1}$ High level width	<23>	T_{WWRH}		$(1+ i +W_{AS})T - 15$		ns
$\overline{WR0}$, $\overline{WR1}$ Low level width	<24>	T_{WWRL}		$(1+W_D)T - 15$		ns
Data output set up time (vs. $\overline{WR0}$, $\overline{WR1}\uparrow$)	<25>	T_{SODWR}		$(0.5+W_T)T - 25$		ns
Data output hold time (vs. $\overline{WR0}$, $\overline{WR1}\uparrow$)	<26>	T_{HWROD}		$(0.5+I)T - 20$		ns

Note: T : 1 / f_{CPU} (= frequency of system clock)
i : Number of idle states specified by BCC register
W_T : Total Number of waits, $W_T = W_{AS}+W_D$
W_{AS} : Number of waits specified by ASC register
W_D : Number of waits specified by DWC1, DWC2 register

Figure 3-5: SRAM Write Timing

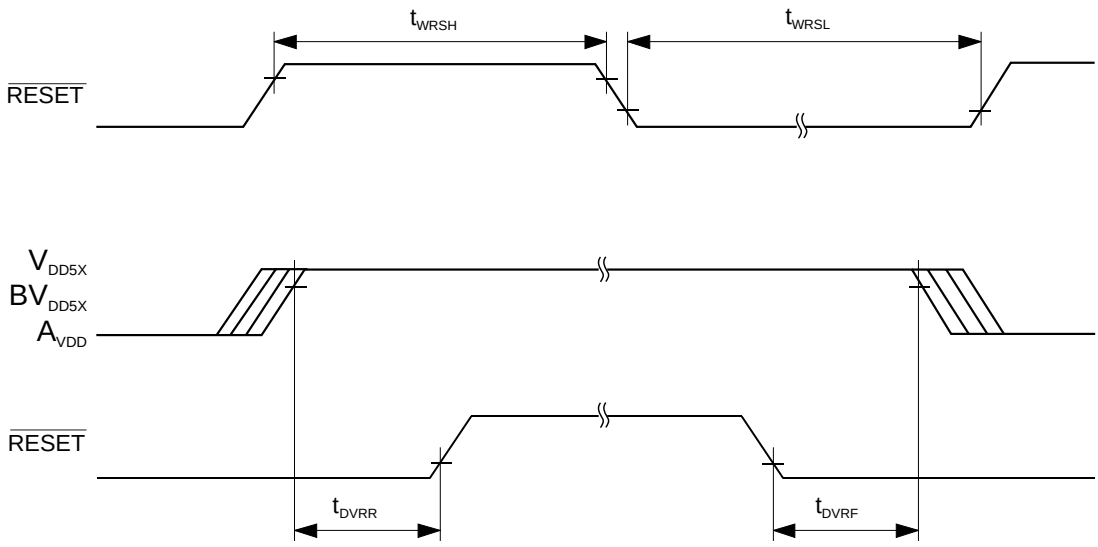


3.5.6 Reset (power up/down sequence)

Table 3-3: Reset Timing

Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
$\overline{\text{RESET}}$ high-level width	t_{WRSH}		500		ns
$\overline{\text{RESET}}$ low-level width	t_{WRSL0}	STOP Mode release, OSC mode	T_{OST}		ms
	t_{WRSL1}	except STOP Mode release & Power Up	1.5		ms
$\overline{\text{RESET}}$ hold time	t_{DVRR}	OSC Mode on power-on	T_{WRSLx}		ms
$\overline{\text{RESET}}$ setup time	t_{DVRF}	OSC Mode on power-off	0		ns

Figure 3-6: Reset Timing



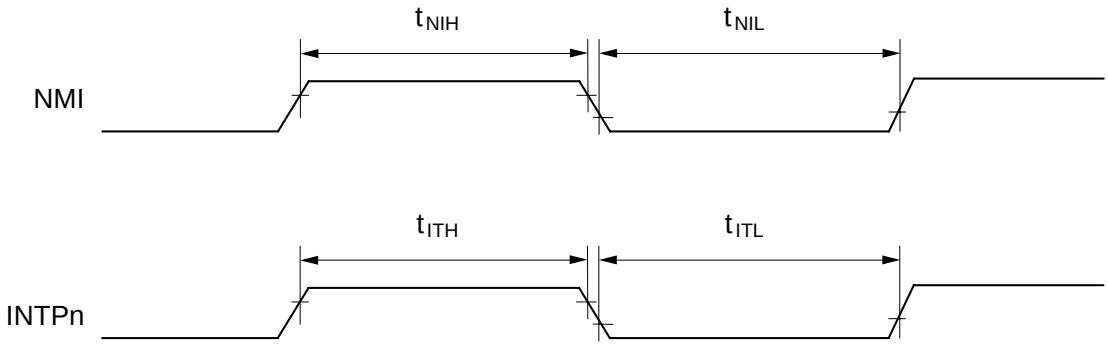
3.5.7 Interrupt timing

Table 3-4: Interrupt Timing

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
NMI high-level width	t_{NIH}	analog filter	500	45		ns
NMI low-level width	t_{NIL}	analog filter	500	45		ns
INTPi**Note** high-level width	t_{ITH}	analog filter	500	45		ns
INTPi**Note** low-level width	t_{ITL}	analog filter	500	45		ns

Note: i = 10…0

Figure 3-7: Interrupt Timing



3.6 Peripheral Function Characteristics

3.6.1 Timer P

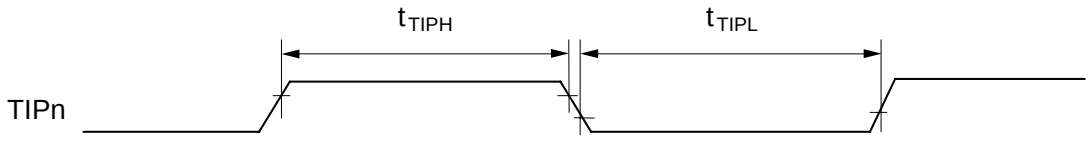
Table 3-5: Timer P Characteristics

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
TIPmn[Note 1] high-level width	t_{TIPH}		$150+4/f_{CLK}$	$45+4/f_{CLK}$[Note 2]		ns
TIPmn[Note 1] low-level width	t_{TIPL}		$150+4/f_{CLK}$	$45+4/f_{CLK}$[Note 2]		ns

Notes: 1. m = 2…0, n = 1…0

2. f_{CLK} is the system clock frequency as specified in section 3.3.1 “CPU clock” on page 18.

Figure 3-8: Timer P Characteristics



3.6.2 CSI B

Table 3-6: CSIB Master Mode Characteristics

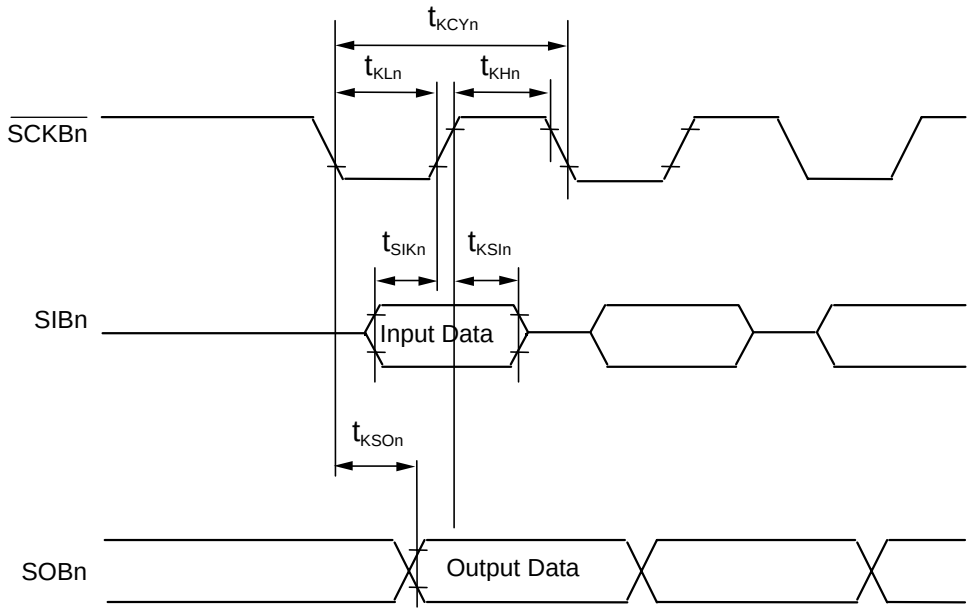
Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
$\overline{SCKBn}$ cycle time	t_{KCY1}		125		ns
$\overline{SCKBn}$ high level width	t_{KH1}		0.5 t_{KCY1} - 15		ns
$\overline{SCKBn}$ low level width	t_{KL1}		0.5 t_{KCY1} - 15		ns
SIBn setup time (to $\overline{SCKBn}$)	t_{SIK1}		30		ns
SIBn hold time (from $\overline{SCKBn}$)	t_{KSI1}		25		ns
Delay time from $\overline{SCKBn}$ to SOBn	t_{KSO1}			25	ns

Table 3-7: CSIB Slave Mode Characteristics

Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
$\overline{SCKBn}$ cycle time	t_{KCY1}		200		ns
$\overline{SCKBn}$ high level width	t_{KH1}		0.5 t_{KCY1} - 15		ns
$\overline{SCKBn}$ low level width	t_{KL1}		0.5 t_{KCY1} - 15		ns
SIBn setup time (to $\overline{SCKBn}$)	t_{SIK1}		50		ns
SIBn hold time (from $\overline{SCKBn}$)	t_{KSI1}		50		ns
Delay time from $\overline{SCKBn}$ to SOBn	t_{KSO1}			50	ns

Remark: n = 2…0

Figure 3-9: CSI Slave Mode Characteristics



3.6.3 UARTA

Table 3-8: UART Characteristics

Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
Transfer rate	T_{UARTA}			312.5	kbps

3.6.4 I²C

Table 3-9: Characteristics I²C

Parameter		Symbol	Normal Mode		High-speed Mode		Unit
			min.	max.	min.	max.	
SCL0 clock frequency		f_{CLK}	0	100	0	400	kHz
Bus-free time (between stop/start conditions)		t_{BUF}	4.7	—	1.3	—	μs
Hold time**Note 1**		$t_{HD:STA}$	4.0	—	0.6	—	μs
SCL0 clock low-level width		t_{LOW}	4.7	—	1.3	—	μs
SCL0 clock high-level width		t_{HIGH}	4.0	—	0.6	—	μs
Setup time for start/restart conditions		$t_{SU:STA}$	4.7	—	0.6	—	μs
Data hold time	CBUS compatible master	$t_{HD:DAT}$	5.0	—	—	—	μs
	I²C mode		0**Note 2**	—	0**Note 2**	0.9**Note 3**	μs
Data setup time		$t_{SU:DAT}$	250	—	100**Note 4**	—	ns
STOP condition setup time		$t_{SU:STO}$	4.0	—	0.6	—	μs
Capacitive load of each bus line		C_b	—	50	—	50	pF

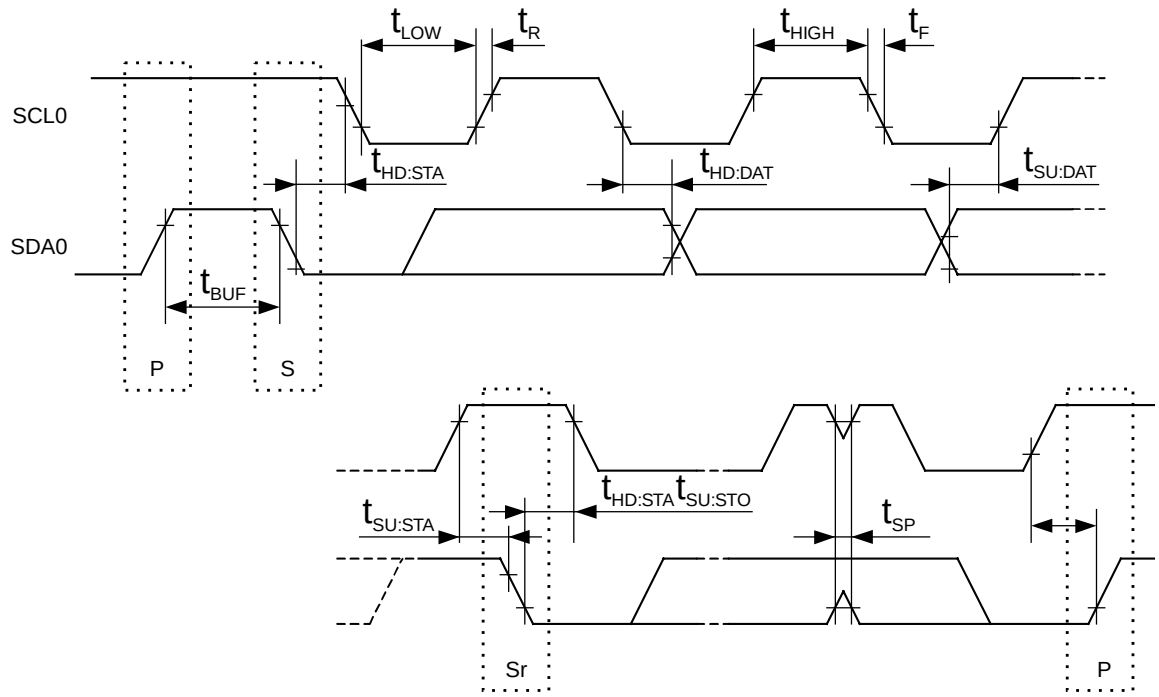
Notes: 1. At the start condition, the first clock pulse is generated after the hold time.

2. The system requires a minimum of 300 ns hold time Internally for the SDA signal (at V_{IHmin} of SCL0 signal) in order to occupy the undefined area at the falling edge of SCL0.

3. If the system does not extend the SCL0 signal low hold time (t_{low}), only the maximum data hold time ($t_{HD:DAT}$) needs to be satisfied.

4. The high-speed-mode IIC bus can be used In a normal-mode IIC bus system.
In this case, set the high-speed-mode IIC bus so that It meets the following conditions:
- If the system does not extend the SCL0n signal's low state hold time: $t_{SU:DAT}$ Š 250 ns
- If the system extends the SCL0n signal's low state hold time:
Transmit the following data bit to the SDA0 line prior to releasing the SCL0 line ($t_{Rmax.}$+$t_{SU:DAT}$ = 1000 + 250 = 1250 ns: Normal mode IIC bus specification).

Figure 3-10: I²C Timing



Remarks: 1. P: Stop condition

2. S: Start condition

3. S_R: Restart condition

3.6.5 FCAN

Table 3-10: AFCAN Characteristics

Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
Transfer rate	T_{FCAN}	$f_{Peripheral} \geq 16$ MHz		1	Mbps

3.6.6 A/D converter

(T_A = -40 ~ +85°C, BV_{DD5} = V_{DD5} = V_{AVDD} = 4.3 ~ 5.5 V, BV_{SS5} = V_{SS5} = AV_{SS} = 0 V)

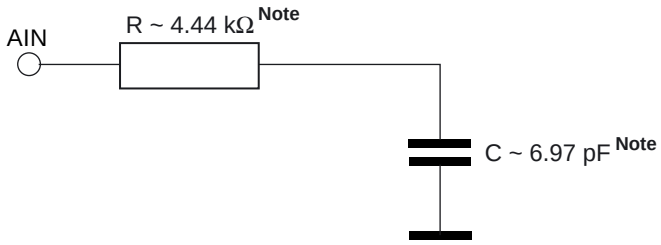
Table 3-11: A/D Converter Characteristics

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Resolution	-			10		Bit
Overall error Note 1	-				± 4	LSB
Conversion time Note 2	T_{CONV}		4.84		38.75	μs
Analog input voltage	V_{IAN}		AV_{SS}		AV_{DD}	V
Analogue supply current	I_{AVDD}			5	10	mA

Notes: 1. Quantization error is not included

2. T_{CONV} depends on register ADA0M1

Figure 3-11: Analog Input Equivalent Circuit



Note: These are typical values only for reference. This values aren't part of the mass production test.

3.7 Flash Memory

3.7.1 Basic characteristics

(T_A = -40 ~ +85°C, BV_{DD5} = V_{DD5} = V_{AVDD} = 4.3 ~ 5.5 V, BV_{SS5} = V_{SS5} = AV_{SS} = 0 V)

Table 3-12: Flash Memory Characteristics

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Operation frequency	f_{CPU}		4		32	MHz
Number of rewrites	C_{WRT}				100	times
High level input voltage	V_{IH}	FLMD0[Note]	0.8 BV_{DD}		BV_{DD}	V
Low level input voltage	V_{IL}		0		0.2 BV_{DD}	V
Programming temperature	t_{PRG}		-40		+85	°C

Note: FLMD0 is shared function of the MODE pin.

3.7.2 Serial write operation characteristics

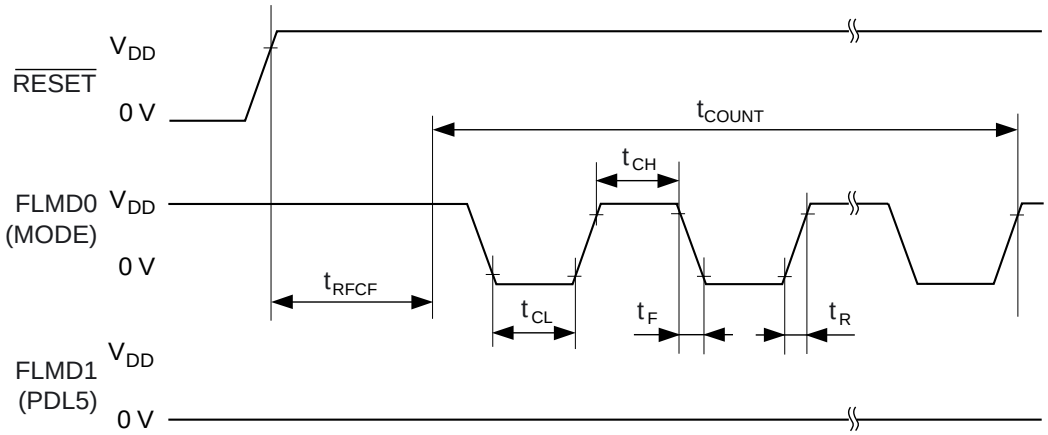
(T_A = -40 ~ +85°C, BV_{DD5} = V_{DD5} = V_{AVDD} = 4.3 ~ 5.5 V, BV_{SS5} = V_{SS5} = AV_{SS} = 0 V)

Table 3-13: Flash Memory Characteristics

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Count start time from rising edge of $\overline{RESET}$ to FLMD0[Note]	t_{RFCF}		t_{OST} + 4500/ f_{OSC}			ms
Count execution time	t_{COUNT}				7800/f_{OSC}	ms
FLMD0 counter High/Low level width	t_{CH},t_{CL}		1			μs

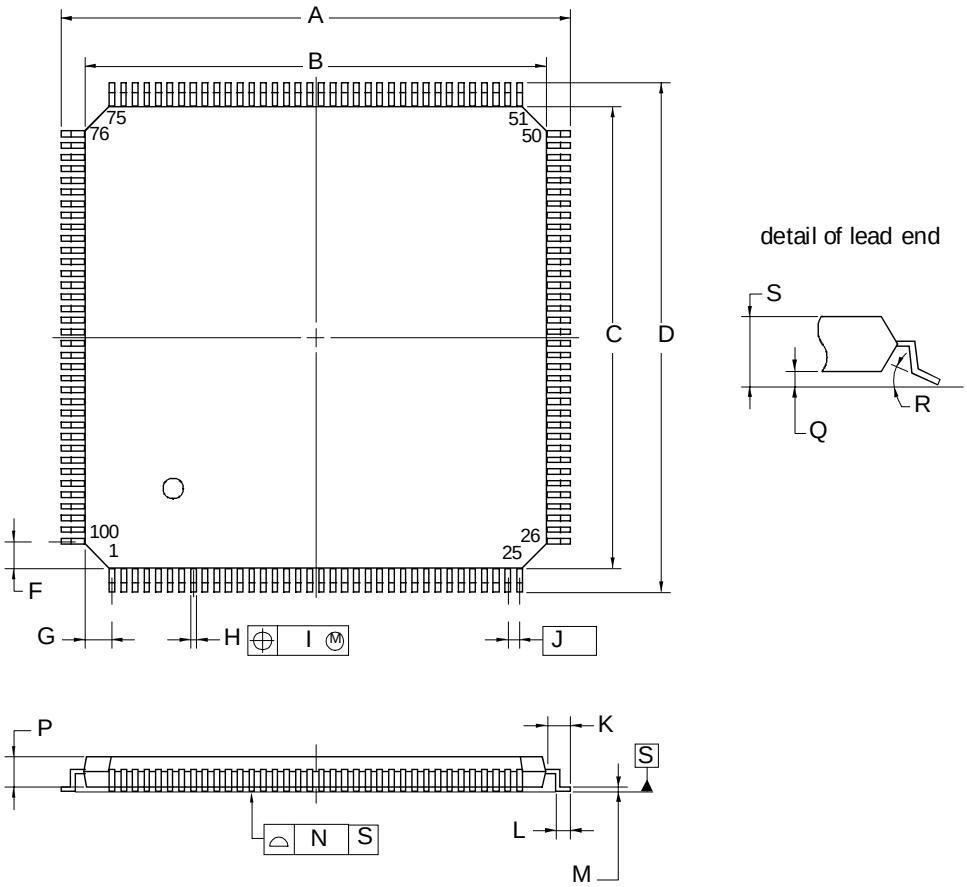
Note: FLMD0 is shared function of the MODE pin.

Figure 3-12: Flash Memory Timing



4. Package Drawing

Figure 4-1: Package Drawing



ITEM	MILLIMETERS
A	16.0±0.2
B	14.0±0.2
C	14.0±0.2
D	16.0±0.2
F	1.00
G	1.00
H	$0.22^{+0.05}_{-0.04}$
I	0.08
J	0.5 (T.P.)
K	1.0±0.2
L	0.5±0.2
M	$0.17^{+0.03}_{-0.07}$
N	0.08
P	1.40±0.05
Q	0.10±0.05
R	3^{+7}_{-3}
S	1.60 MAX

S100GC-50-8EU-1

5. Recommended Soldering Conditions

Solder this product under the following recommended conditions.
For details of the recommended soldering conditions, refer to information document Semiconductor Device:

Mounting Technology Manual (C10535E).

For soldering methods and conditions other than those recommended please consult NEC.

Table 5-1: Soldering Conditions

Soldering Method	Soldering Condition	Symbol of Recommended Soldering Condition
Infrared reflow	Package peak temperature: 235 °C, Time: 10 seconds max., Number of times: 3 max., Number of days: 7 **Note**	IR35-107-3

Note: After that, prebaking is necessary at 125 °C for 10 hours.
The number of days refers to storage at 25°C, 65% RH MAX after the dry pack has been opened.

Caution: Do not use two or more soldering methods in combination (except partial heating method).

6. Revision History

Version	Date	Author	Remarks
0.1	2004/09/20	S.Vollhardt	First released version of this document
0.2	2004/10/05	S.Vollhardt	First official release
		S.Vollhardt	CSIB max speed for master & slave mode corrected
		S.Vollhardt	UARTA max speed added
		S.Vollhardt	AC values added
		S.Vollhardt	Flash write / erase time and FLMD0 rise/fall time removed
EE1V1	2005/02/25	S.Vollhardt	This version replaced the “Preliminary” one U17344EE1V0DS00.
			Table 3-2, DC characteristics, page 19, the value of supply current I_{DD11} (max.) has been changed from 85 mA to 90 mA.

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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[MEMO]