

To our customers,

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## Old Company Name in Catalogs and Other Documents

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April 1<sup>st</sup>, 2010  
Renesas Electronics Corporation

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## 7400 PIXELS CCD LINEAR IMAGE SENSOR

The  $\mu$ PD8670A is a high sensitive and high-speed CCD (Charge Coupled Device) linear image sensor which changes optical images to electrical signal.

The  $\mu$ PD8670A is a 2-output type CCD sensor with 2 rows of high-speed charge transfer register, which transfers the photo signal electrons of 7400 pixels separately in odd and even pixels. And it has reset feed-through level clamp circuits and voltage amplifiers. Therefore, it is suitable for 600 dpi/A3 high-speed digital copiers, multi-function products and so on.

### FEATURES

- Valid photocell : 7400 pixels
- Photocell pitch : 4.7  $\mu$ m
- Photocell size : 4.7  $\times$  4.7  $\mu$ m<sup>2</sup>
- Resolution : 24 dot/mm (600 dpi) A3 (297  $\times$  420 mm) size (shorter side)
- Data rate : 44 MHz MAX. (22 MHz/1 output)
- Output type : 2 outputs in-phase operation, and out of phase also supported
- High sensitivity : 17.0 V/lx $\cdot$ s TYP. (Light source: Daylight color fluorescent lamp)
- Peak response wavelength : 550 nm (green)
- Low image lag : 1 % MAX.
- Drive clock level : CMOS output under +5 V operation
- Power supply : +12 V
- On-chip circuits : Reset feed-through level clamp circuits  
Voltage amplifiers

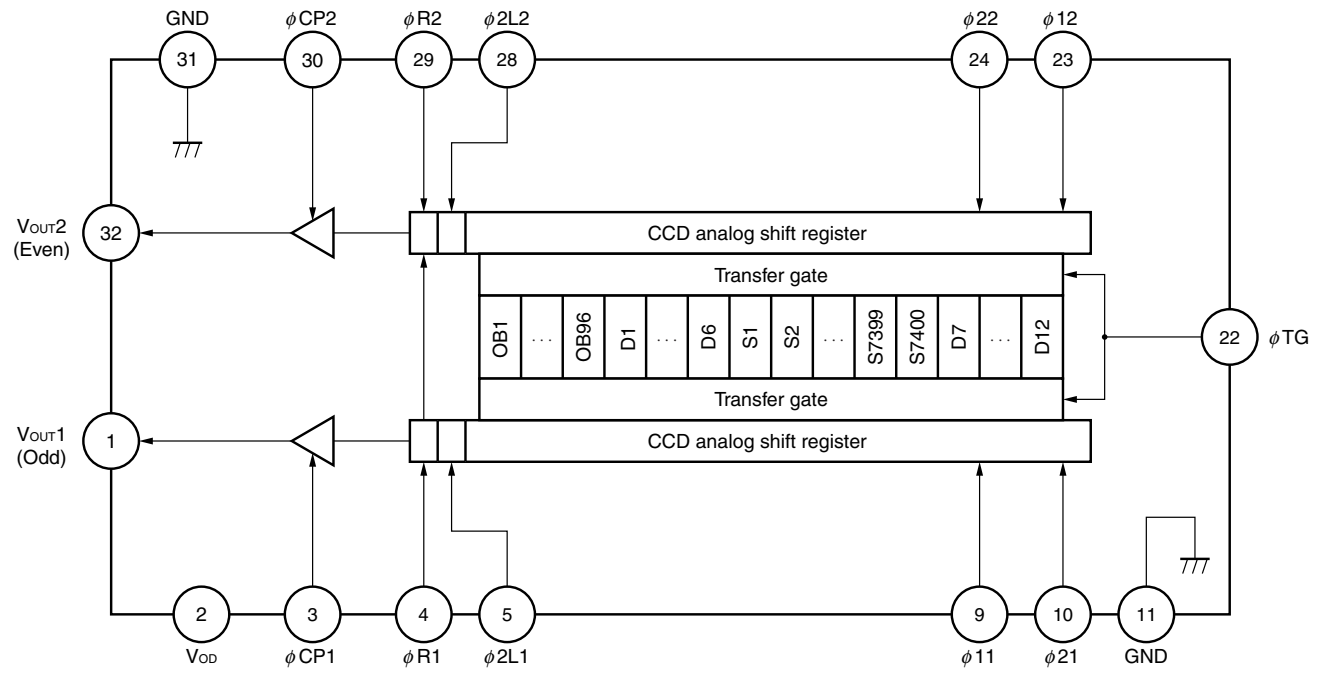
### ORDERING INFORMATION

Part Number	Package
$\mu$ PD8670ACY-A	CCD linear image sensor 32-pin plastic DIP (10.16 mm (400))

<R> **Remark** The  $\mu$ PD8670ACY-A is a lead-free product.

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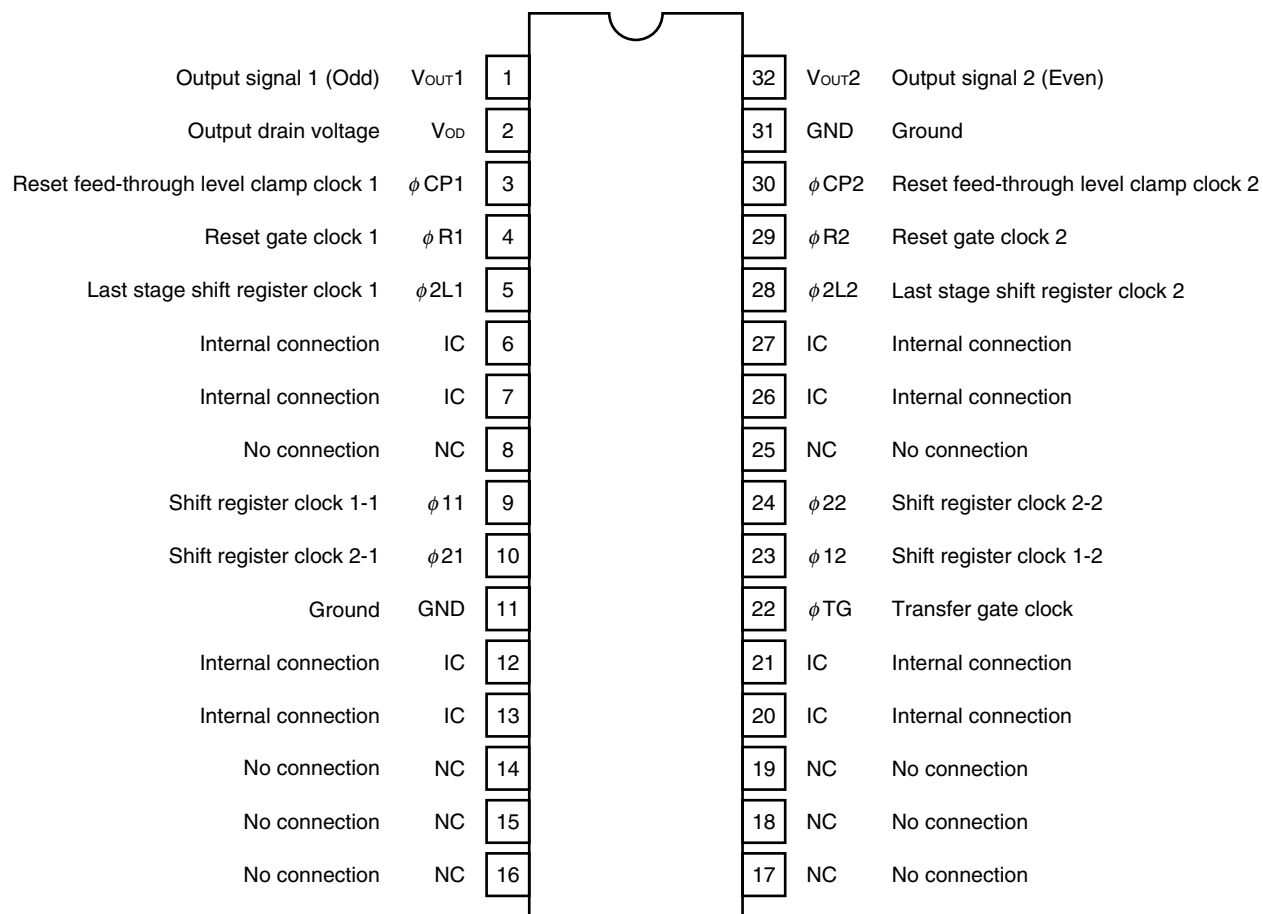
BLOCK DIAGRAM



**PIN CONFIGURATION (Top View)**

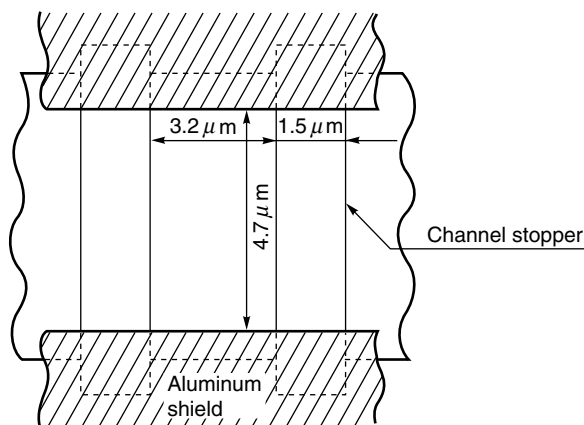
**CCD linear image sensor 32-pin plastic DIP (10.16 mm (400))**

• μPD8670ACY-A



- Cautions**
1. Leave pins 6, 7, 12, 13, 20, 21, 26 and 27 (IC) unconnected.
  2. Connect the No connection pins (NC) to GND.

**PHOTOCELL STRUCTURE DIAGRAM**



**ABSOLUTE MAXIMUM RATINGS (T<sub>A</sub> = +25°C)**

Parameter	Symbol	Ratings	Unit
Output drain voltage	V <sub>OD</sub>	-0.3 to +14.0	V
Shift register clock voltage	V <sub>φ1</sub> , V <sub>φ2</sub>	-0.3 to +8.0	V
Last stage shift register clock voltage	V <sub>φ2L</sub>	-0.3 to +8.0	V
Reset gate clock voltage	V <sub>φR</sub>	-0.3 to +8.0	V
Transfer gate clock voltage	V <sub>φTG</sub>	-0.3 to +8.0	V
Reset feed-through level clamp clock voltage	V <sub>φCP</sub>	-0.3 to +8.0	V
Operating ambient temperature <sup>Note</sup>	T <sub>A</sub>	0 to +60	°C
Storage temperature	T <sub>stg</sub>	-40 to +70	°C

**Note** Use at the condition without dew condensation.

**Caution** Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

**RECOMMENDED OPERATING CONDITIONS (T<sub>A</sub> = +25°C)**

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Output drain voltage	V <sub>OD</sub>		11.4	12.0	12.6	V
Shift register clock high level	V <sub>φ1H</sub> , V <sub>φ2H</sub>		4.5	5.0	5.5	V
Shift register clock low level	V <sub>φ1L</sub> , V <sub>φ2L</sub>		-0.3	0	+0.5	V
Last stage shift register clock high level	V <sub>φ2LH</sub>		4.5	5.0	5.5	V
Last stage shift register clock low level	V <sub>φ2LL</sub>		-0.3	0	+0.5	V
Reset gate clock high level	V <sub>φRH</sub>		4.5	5.0	5.5	V
Reset gate clock low level	V <sub>φRL</sub>		-0.3	0	+0.5	V
Reset feed-through level clamp clock high level	V <sub>φCPH</sub>		4.5	5.0	5.5	V
Reset feed-through level clamp clock low level	V <sub>φCPL</sub>		-0.3	0	+0.5	V
Transfer gate clock high level	V <sub>φTGH</sub>		4.5	5.0	5.5	V
Transfer gate clock low level	V <sub>φTGL</sub>		-0.3	0	+0.5	V
Shift register clock amplitude	V <sub>φ1_pp</sub> , V <sub>φ2_pp</sub>	f < 10 MHz/ch	4.0	5.0	5.8	V
		f ≥ 10 MHz/ch	4.5	5.0	5.8	V
Last stage shift register clock amplitude	V <sub>φ2L_pp</sub>		4.5	5.0	5.8	V
Reset gate clock amplitude	V <sub>φR_pp</sub>		4.5	5.0	5.8	V
Reset feed-through level clamp clock amplitude	V <sub>φCP_pp</sub>		4.5	5.0	5.8	V
Transfer gate clock amplitude	V <sub>φTG_pp</sub>		4.5	5.0	5.8	V
Data rate	2f <sub>φR</sub>		1	2	44	MHz

**ELECTRICAL CHARACTERISTICS**

$T_A = +25^{\circ}\text{C}$ ,  $V_{OD} = 12\text{ V}$ ,  $f_{\phi R} = 1\text{ MHz}$ , data rate = 2 MHz, storage time = 10 ms, input signal clock = 5 V<sub>p-p</sub>,  
light source : 3200 K halogen lamp + C-500S (infrared cut filter, t = 1 mm) + HA-50 (heat absorbing filter, t = 3 mm)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit	
Saturation voltage	V <sub>sat</sub>		1.5	2.0	–	V	
Saturation exposure	SE	Daylight color fluorescent lamp	–	0.10	–	lx•s	
Photo response non-uniformity	PRNU	V <sub>OUT</sub> = 500 mV	–	5.0	10.0	%	
Average dark signal	ADS	Light shielding	–	1.0	6.0	mV	
Dark signal non-uniformity	DSNU	Light shielding	–	16.0	28.0	mV	
Power consumption	P <sub>w</sub>		–	350	420	mW	
Output impedance	Z <sub>o</sub>		–	0.2	0.3	kΩ	
Response	R <sub>f</sub>	Daylight color fluorescent lamp	13.6	17.0	20.4	V/lx•s	
Image lag	IL	V <sub>OUT</sub> = 500 mV	–	0.5	1.0	%	
Offset level <sup>Note 1</sup>	V <sub>OS</sub>		3.7	4.7	5.7	V	
Output fall delay time <sup>Note 2</sup>	t <sub>d</sub>	V <sub>OUT</sub> = 500 mV	11.0	13.0	15.0	ns	
Total transfer efficiency	TTE	V <sub>OUT</sub> = 1 V, data rate = 44 MHz	94	98	–	%	
Register imbalance	RI	V <sub>OUT</sub> = 500 mV	0	1.0	4.0	%	
Response peak			–	550	–	nm	
Dynamic range	DR1	V <sub>sat</sub> /DSNU	–	125	–	times	
	DR2	V <sub>sat</sub> /σ <sub>bit</sub> , t <sub>6</sub> ≥ 20 ns	–	1000	–	times	
Reset feed-through noise <sup>Note 1</sup>	PRFTN	Light shielding, t <sub>4</sub> = 5 ns	–	+0.4	–	V	
	RFTN1		–1.0	–0.4	+0.2	V	
	RFTN2		–0.3	+0.2	+0.7	V	
Random noise	σ <sub>bit</sub>	Light shielding, bit clamp mode	t <sub>6</sub> = 5 ns	–	2.6	–	mV
			t <sub>6</sub> ≥ 20 ns	–	2.0	–	mV
	σ <sub>line</sub>	Light shielding, line clamp mode	t <sub>6</sub> ≥ 5 ns	–	8.0	–	mV
Shot noise	σ <sub>shot</sub>	V <sub>OUT</sub> = 500 mV, bit clamp mode	t <sub>6</sub> ≥ 5 ns	–	10.0	–	mV

**Notes 1.** Refer to 13 and 14 of **DEFINITION OF CHARACTERISTIC ITEMS**.

**2.** When the fall time of φ2L (t<sub>2'</sub>) is the TYP. value (refer to **TIMING CHART 5, 6**). Note that V<sub>OUT1</sub> and V<sub>OUT2</sub> are the outputs of the two steps of emitter-follower shown in **APPLICATION CIRCUIT EXAMPLE**.

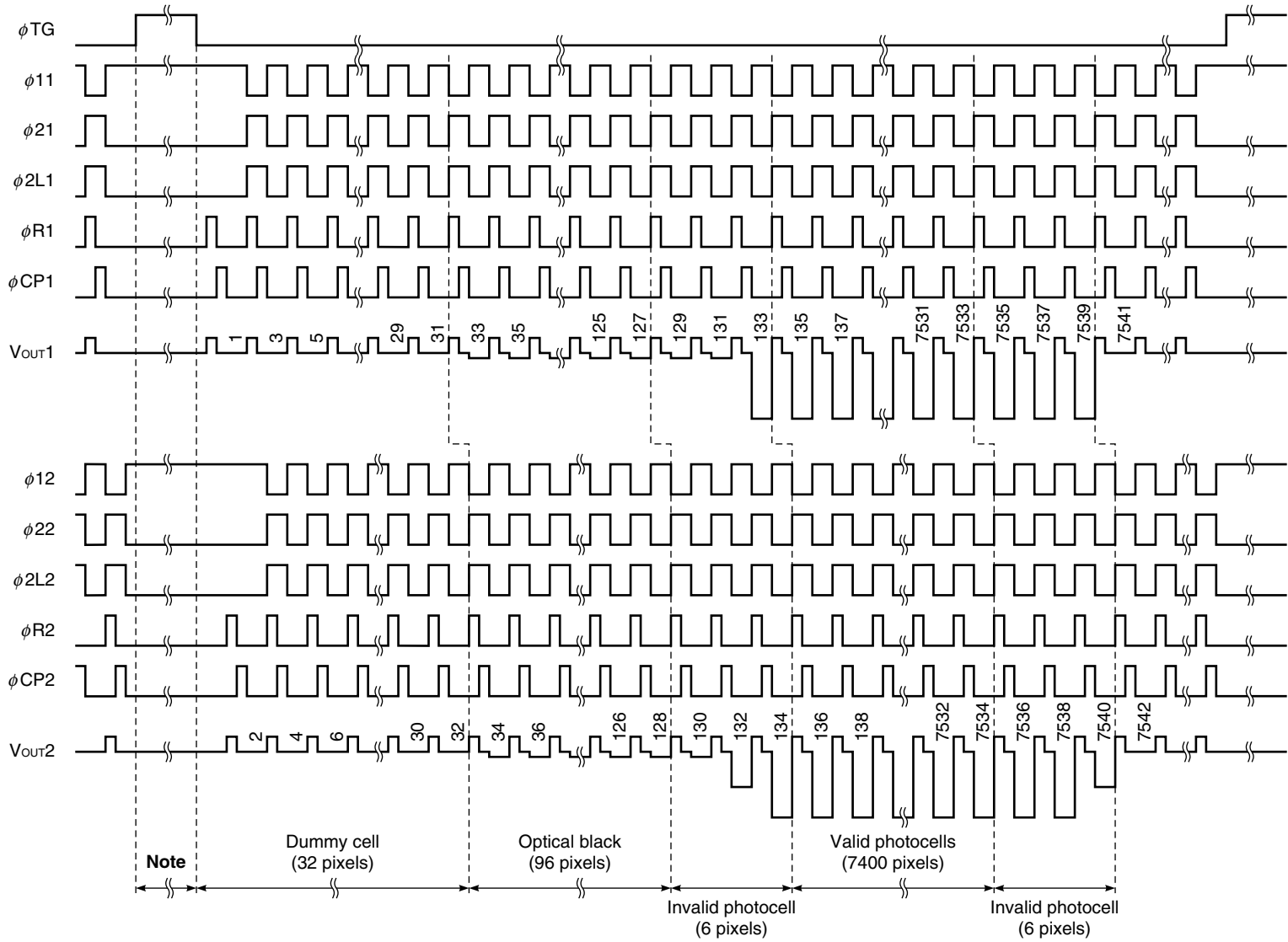
**INPUT PIN CAPACITANCE (T<sub>A</sub> = +25°C, V<sub>OD</sub> = 12 V)**

Parameter	Symbol	Pin name	Pin No.	MIN.	TYP.	MAX.	Unit
Shift register clock pin capacitance 1	C <sub>φ1</sub> <sup>Note</sup>	φ 11	9	225	250	275	pF
		φ 12	23	200	220	240	pF
Shift register clock pin capacitance 2	C <sub>φ2</sub> <sup>Note</sup>	φ 21	10	200	220	240	pF
		φ 22	24	225	250	275	pF
Last stage shift register clock pin capacitance	C <sub>φL</sub>	φ 2L1	5	4	5	6	pF
		φ 2L2	28	4	5	6	pF
Reset gate clock pin capacitance	C <sub>φR</sub>	φ R1	4	4	5	6	pF
		φ R2	29	4	5	6	pF
Reset feed-through level clamp clock pin capacitance	C <sub>φCP</sub>	φ CP1	3	7	8	9	pF
		φ CP2	30	7	8	9	pF
Transfer gate clock pin capacitance	C <sub>φTG</sub>	φ TG	22	240	270	300	pF

**Note** C<sub>φ1</sub>, C<sub>φ2</sub> are equivalent capacitance with driving device, including the co-capacitance between φ1 and φ2.

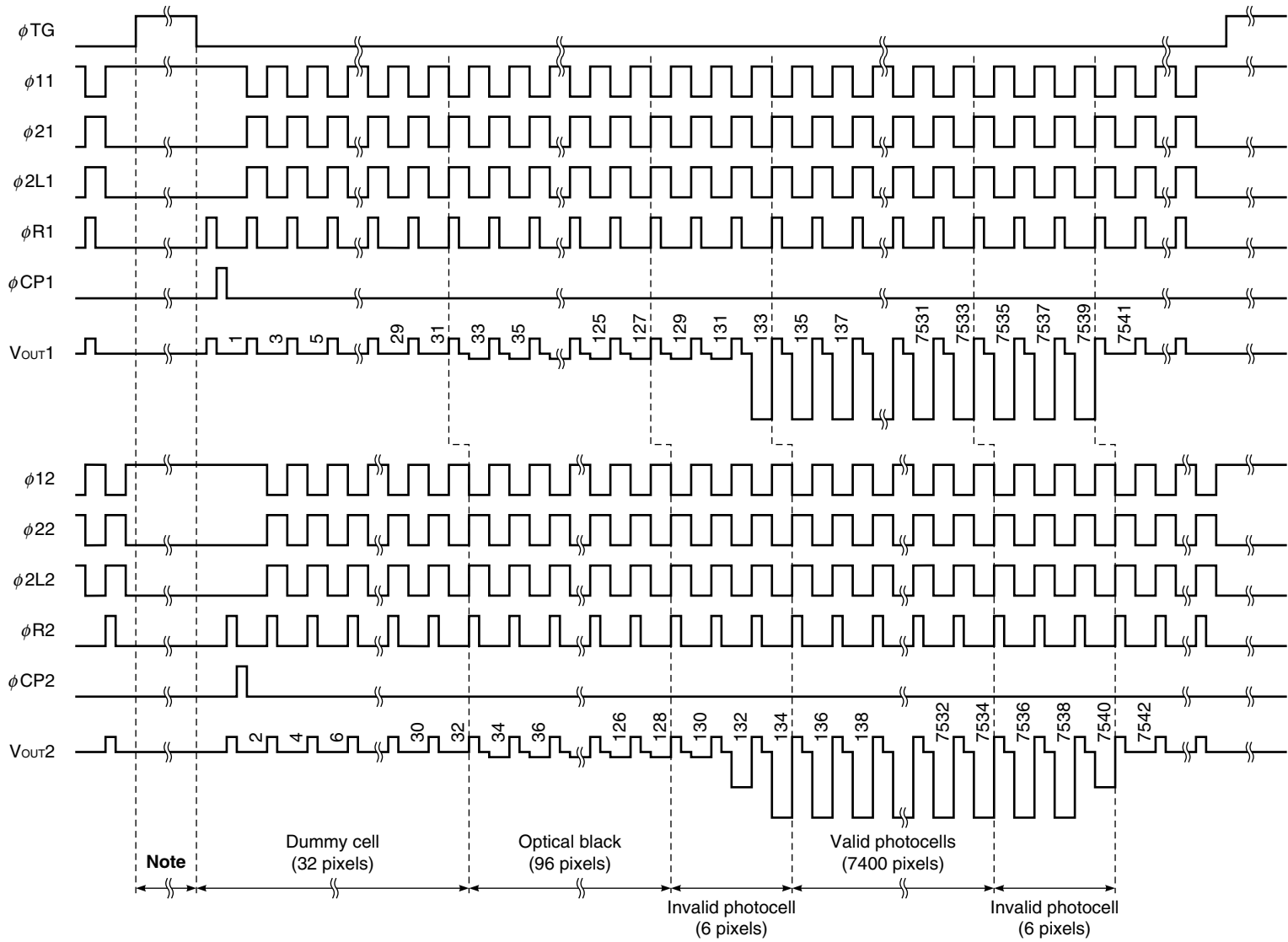
**Remark** Pins 9 and 23 (φ11 and φ12), Pins 10 and 24 (φ21 and φ22) aren't each connected inside of the device.

**TIMING CHART 1 (Bit clamp mode, Out of phase operation)**



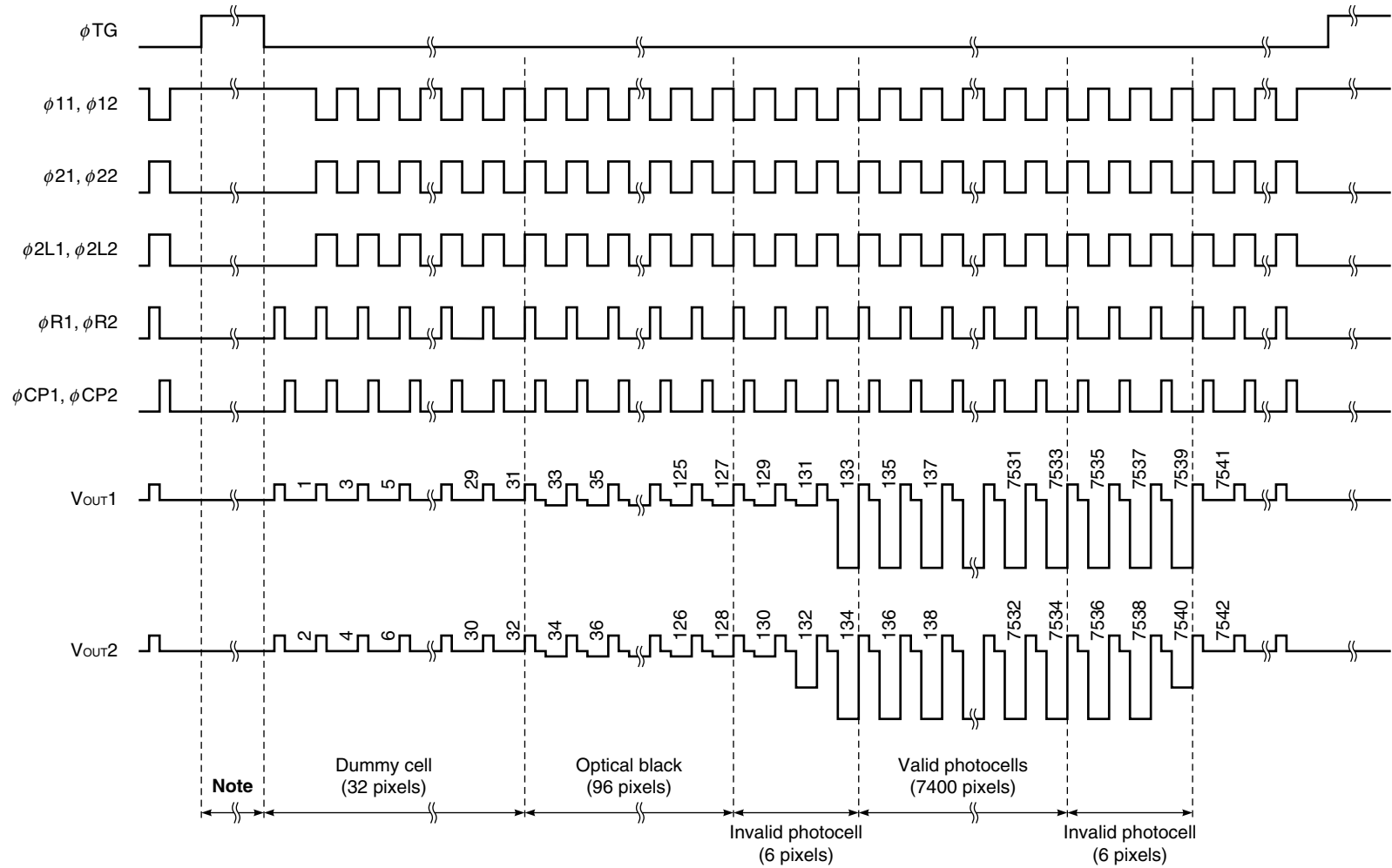
**Note** Set the  $\phi_{R1}$ ,  $\phi_{R2}$ ,  $\phi_{CP1}$  and  $\phi_{CP2}$  to low level during this period.

**TIMING CHART 2 (Line clamp mode, Out of phase operation)**



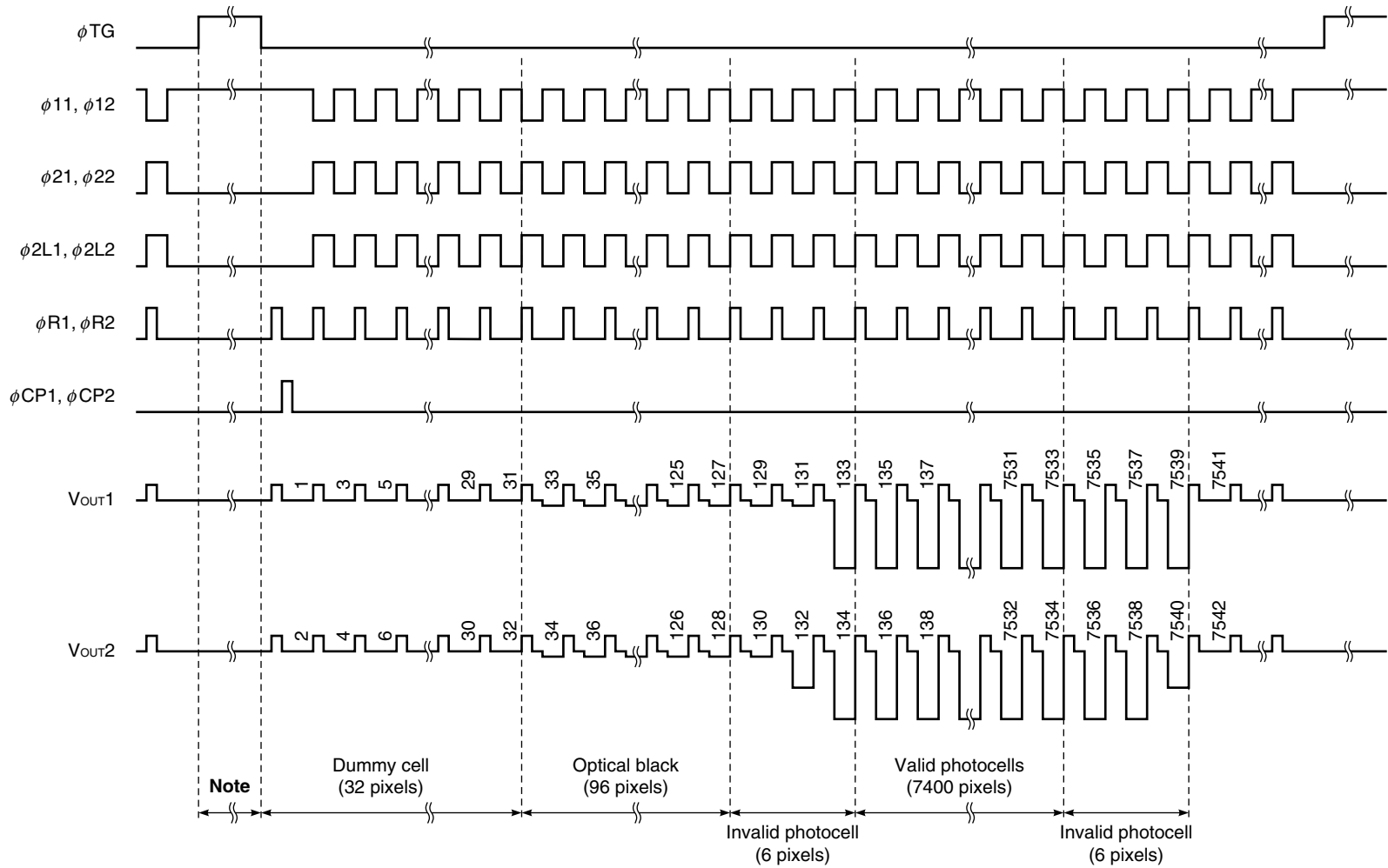
**Note** Set the  $\phi_{R1}$ ,  $\phi_{R2}$ ,  $\phi_{CP1}$  and  $\phi_{CP2}$  to low level during this period.

**TIMING CHART 3 (Bit clamp mode, In phase operation)**



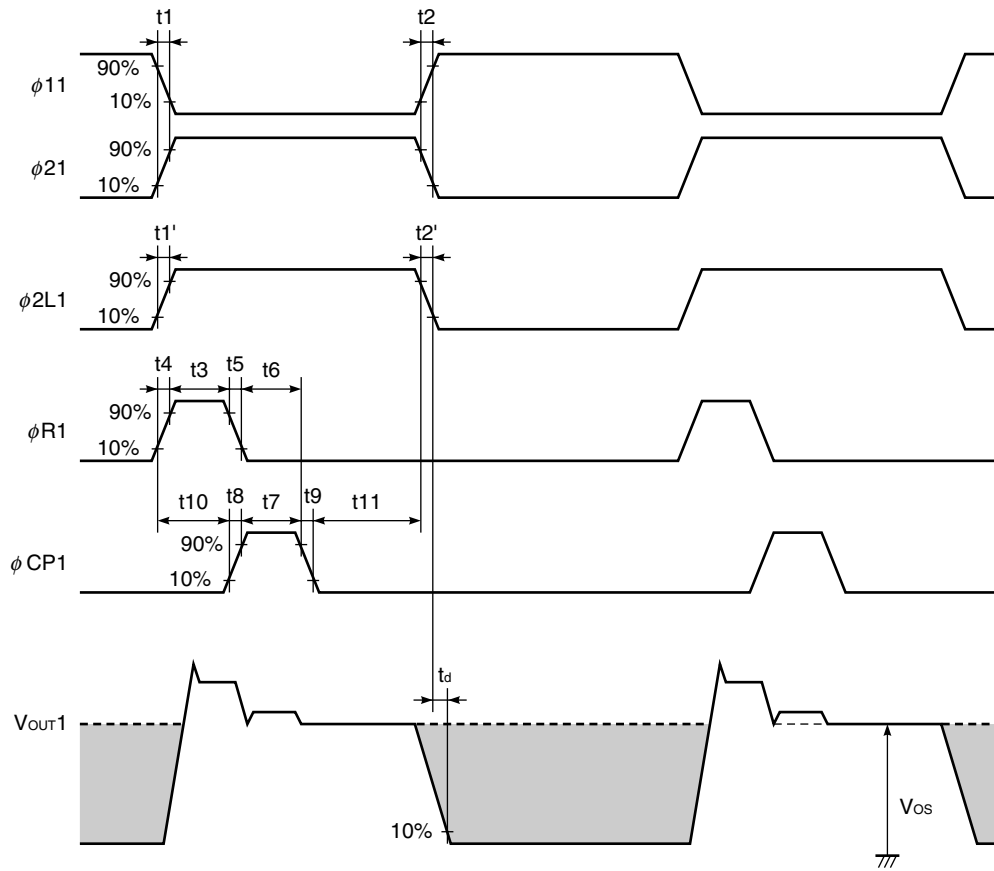
**Note** Set the  $\phi_{R1}$ ,  $\phi_{R2}$ ,  $\phi_{CP1}$  and  $\phi_{CP2}$  to low level during this period.

**TIMING CHART 4 (Line clamp mode, In phase operation)**



**Note** Set the  $\phi_{R1}$ ,  $\phi_{R2}$ ,  $\phi_{CP1}$  and  $\phi_{CP2}$  to low level during this period.

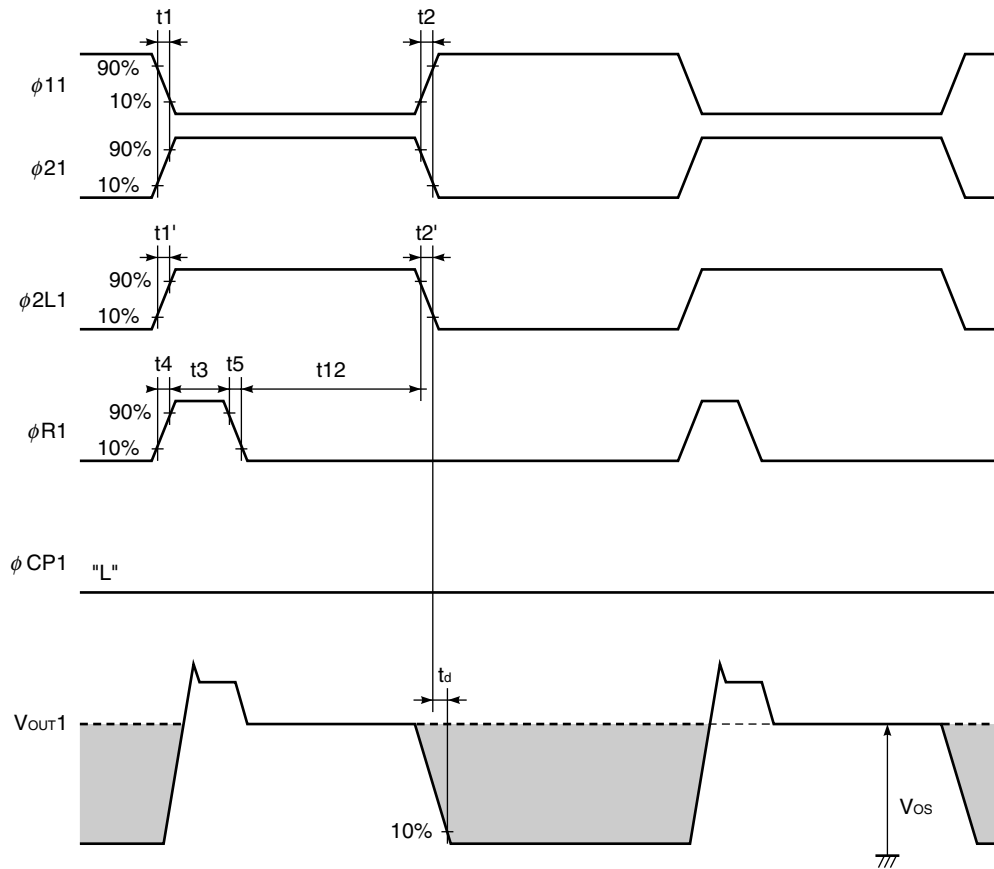
**TIMING CHART 5 (Bit clamp mode)**



Symbol	MIN.	TYP.	MAX.	Unit
$t_1, t_2$	0	50	–	ns
$t_1', t_2'$	0	5	–	ns
$t_3$	10	125	–	ns
$t_4, t_5$	0	5	–	ns
$t_6$	5	125	–	ns
$t_7$	5	125	–	ns
$t_8, t_9$	0	5	–	ns
$t_{10}$	0	125	–	ns
$t_{11}$	0	250	–	ns

**Caution** This shows timing chart of  $V_{OUT1}$  side ( $\phi_{11}$ ,  $\phi_{21}$ ,  $\phi_{2L1}$ ,  $\phi_{R1}$ ,  $\phi_{CP1}$ ,  $V_{OUT1}$ ). The timing chart of  $V_{OUT2}$  side ( $\phi_{12}$ ,  $\phi_{22}$ ,  $\phi_{2L2}$ ,  $\phi_{R2}$ ,  $\phi_{CP2}$ ,  $V_{OUT2}$ ) is equal.

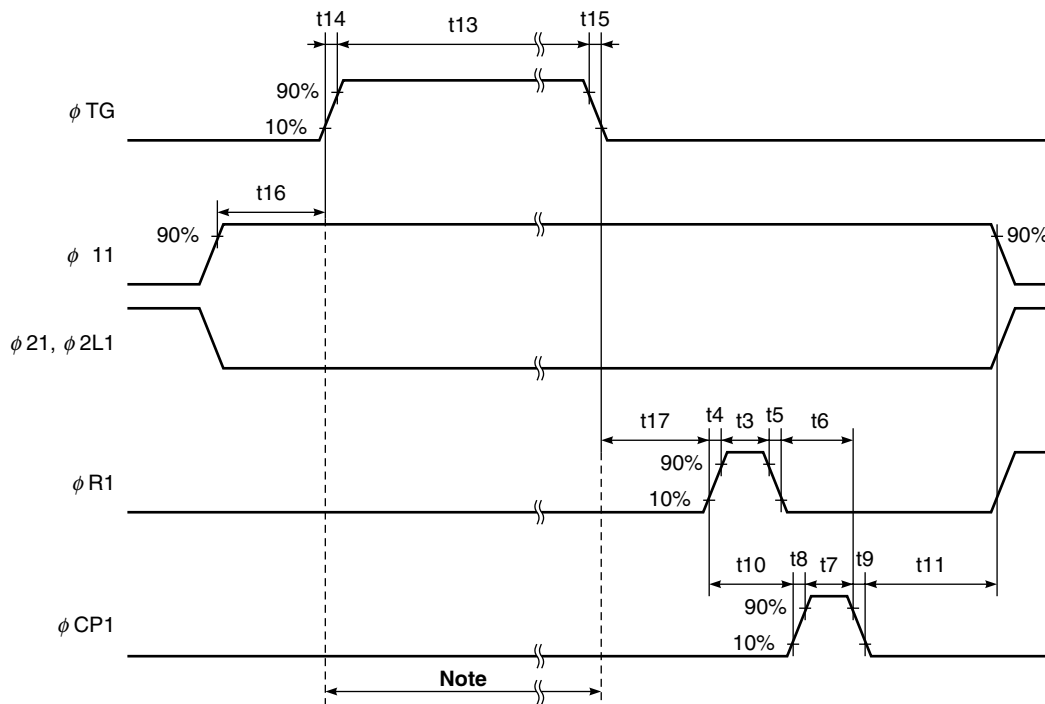
**TIMING CHART 6 (Line clamp mode)**



Symbol	MIN.	TYP.	MAX.	Unit
$t_1, t_2$	0	50	–	ns
$t_1', t_2'$	0	5	–	ns
$t_3$	10	125	–	ns
$t_4, t_5$	0	5	–	ns
$t_{12}$	5	250	–	ns

**Caution** This shows timing chart of  $V_{OUT1}$  side ( $\phi_{11}, \phi_{21}, \phi_{2L1}, \phi_{R1}, \phi_{CP1}, V_{OUT1}$ ). The timing chart of  $V_{OUT2}$  side ( $\phi_{12}, \phi_{22}, \phi_{2L2}, \phi_{R2}, \phi_{CP2}, V_{OUT2}$ ) is equal.

**TIMING CHART 7 (Bit clamp mode, Line clamp mode)**

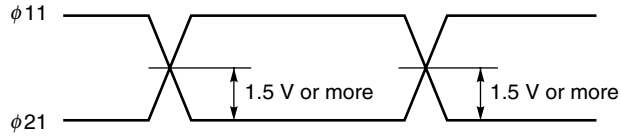


**Note** Set the  $\phi$  R and  $\phi$  CP to low level during this period.

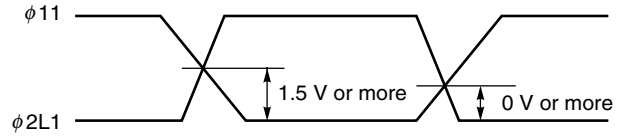
Symbol	MIN.	TYP.	MAX.	Unit
t3	10	125	–	ns
t4, t5	0	5	–	ns
t6	5	125	–	ns
t7	5	125	–	ns
t8, t9	0	5	–	ns
t10	0	125	–	ns
t11	0	250	–	ns
t13	1000	1500	10000	ns
t14, t15	0	50	–	ns
t16, t17	200	300	10000	ns

**Caution** This shows timing chart of  $V_{OUT1}$  side ( $\phi$ 11,  $\phi$ 21,  $\phi$ 2L1,  $\phi$ R1,  $\phi$ CP1,  $V_{OUT1}$ ). The timing chart of  $V_{OUT2}$  side ( $\phi$ 12,  $\phi$ 22,  $\phi$ 2L2,  $\phi$ R2,  $\phi$ CP2,  $V_{OUT2}$ ) is equal.

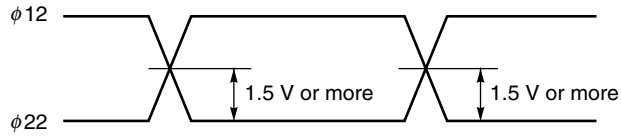
**φ11, φ21 cross points**



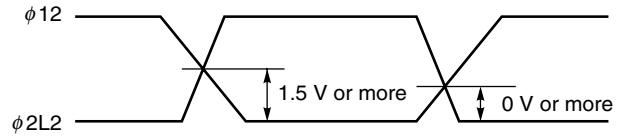
**φ11, φ2L1 cross points**



**φ12, φ22 cross points**

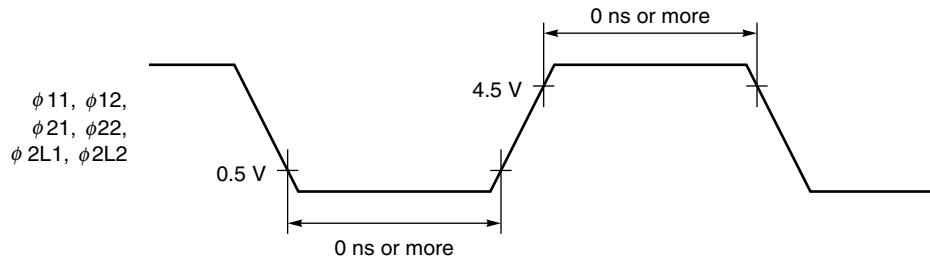


**φ12, φ2L2 cross points**



**Remark** Adjust cross points of (φ11, φ21), (φ11, φ2L1), (φ12, φ22) and (φ12, φ2L2) with input resistance of each pin.

**φ11, φ12, φ21, φ22, φ2L1, φ2L2 clock width**



**DEFINITIONS OF CHARACTERISTIC ITEMS**

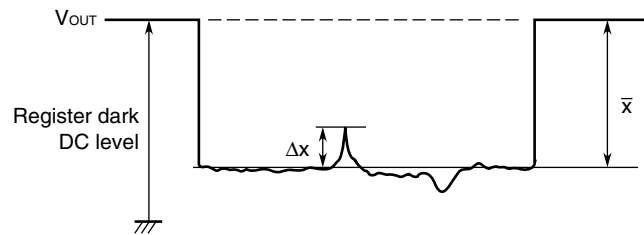
1. Saturation voltage : **V<sub>sat</sub>**  
Output signal voltage at which the response linearity is lost.
2. Saturation exposure : **SE**  
Product of intensity of illumination (lx) and storage time (s) when saturation of output voltage occurs.
3. Photo response non-uniformity : **PRNU**  
The output signal non-uniformity of all the valid pixels when the photosensitive surface is applied with the light of uniform illumination. This is calculated by the following formula.

$$PRNU (\%) = \frac{\Delta x}{\bar{x}} \times 100$$

Δx: maximum of  $|x_j - \bar{x}|$

$$\bar{x} = \frac{\sum_{j=1}^{7400} x_j}{7400}$$

x<sub>j</sub>: Output voltage of valid pixel number j



4. Average dark signal : **ADS**  
Average output signal voltage of all the valid pixels at light shielding. This is calculated by the following formula.

$$ADS (mV) = \frac{\sum_{j=1}^{7400} d_j}{7400}$$

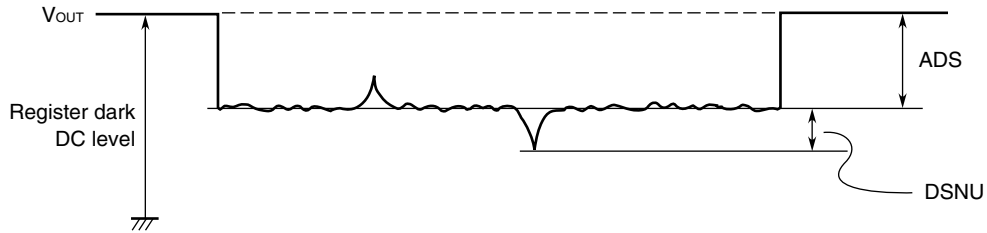
d<sub>j</sub>: Dark signal of valid pixel number j

5. Dark signal non-uniformity : **DSNU**

Absolute maximum of the difference between ADS and voltage of the highest or lowest output pixel of all the valid pixels at light shielding. This is calculated by the following formula.

DSNU (mV): maximum of  $|d_j - ADS|$   $|j = 1 \text{ to } 7400$

$d_j$ : Dark signal of valid pixel number  $j$



6. Output impedance : **Zo**

Impedance of the output pins viewed from outside.

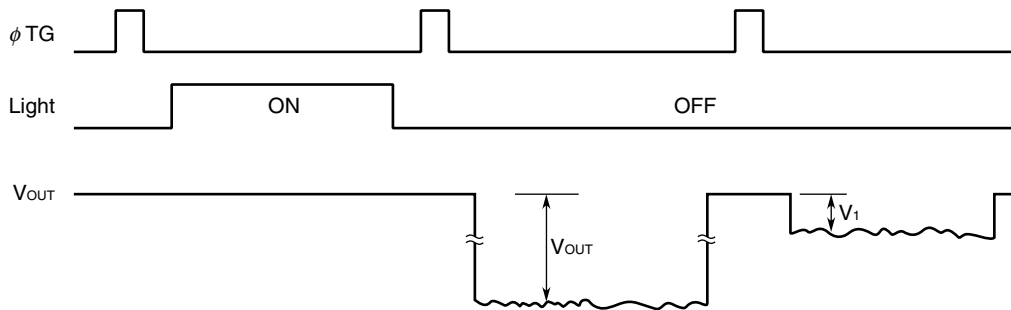
7. Response : **R**

Output voltage divided by exposure ( $lx \cdot s$ ).

Note that the response varies with a light source (spectral characteristic).

8. Image lag : **IL**

The rate between the last output voltage and the next one after read out the data of a line.

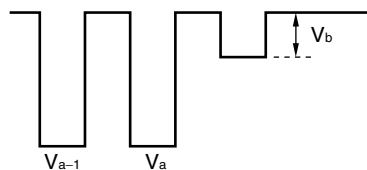


$$IL (\%) = \frac{V_1}{V_{OUT}} \times 100$$

9. Total transfer efficiency : **TTE**

The total transfer rate of CCD analog shift register. This is calculated by the following formula, it is defined by each output.

$$TTE (\%) = (1 - V_b / \text{average output of all the valid pixels}) \times 100$$



$V_{a-1}$  : The last pixel output - 1 (Odd pixel: 7537th pixel)

$V_a$  : The last pixel output (Odd pixel: 7539th pixel)

$V_b$  : The split pixel output (Odd pixel: 7541st pixel)

10. Register imbalance : **RI**

The rate of the difference between the averages of the output voltage of Odd and Even pixels, against the average output voltage of all the valid pixels.

$$RI (\%) = \frac{\frac{2}{n} \left| \sum_{j=1}^{\frac{n}{2}} (V_{2j-1} - V_{2j}) \right|}{\frac{1}{n} \sum_{j=1}^n V_j} \times 100$$

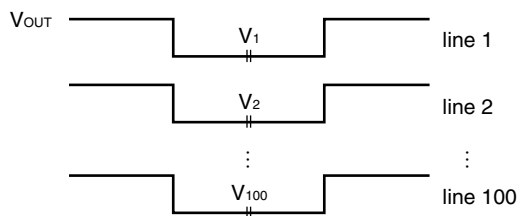
n : Number of valid pixels  
 V<sub>j</sub>: Output voltage of each pixel

11. Random noise : **σ**

Random noise σ is defined as the standard deviation of a valid pixel output signal with 100 times (= 100 lines) data sampling at dark (light shielding).

$$\sigma (mV) = \sqrt{\frac{\sum_{i=1}^{100} (V_i - \bar{V})^2}{100}}, \quad \bar{V} = \frac{1}{100} \sum_{i=1}^{100} V_i$$

V<sub>i</sub>: A valid pixel output signal among all of the valid pixels



This is measured by the DC level sampling of only the signal level, not by CDS (Correlated Double Sampling).

12. Shot noise : **σ<sub>shot</sub>**

Shot noise is defined as the standard deviation of a valid pixel output signal with 100 times (= 100 lines) data sampling in the light. This includes the random noise.

The formula is the same with that of random noise.

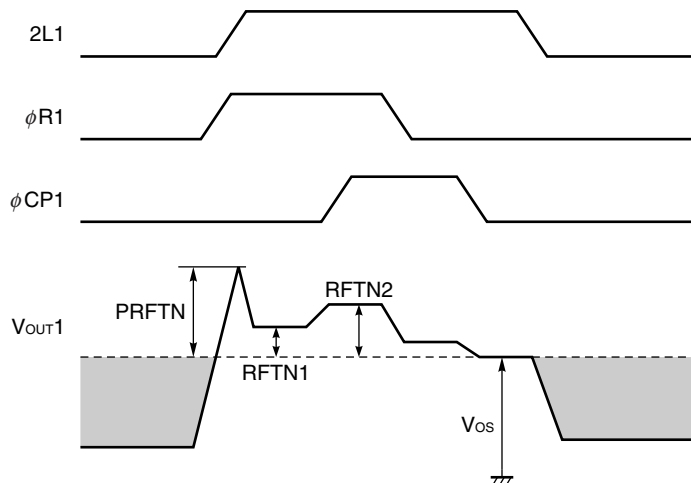
13. Offset level :  $V_{os}$

DC level of output signal is defined as follows.

14. Reset feed-through noise and peak reset feed-through noise : **RFTN** and **PRFTN**

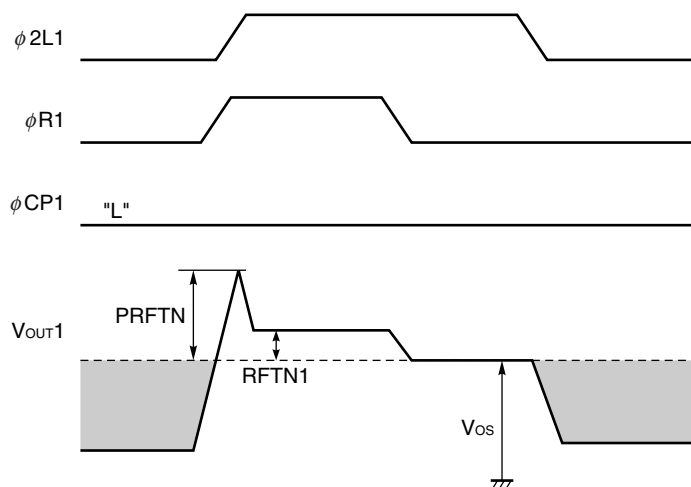
RFTN is switching noise of  $\phi_R$  and  $\phi_{CP}$ . Reset feed-through noise (RFTN) and peak of RFTN (PRFTN) are defined as follows.

<1> Bit clamp operation



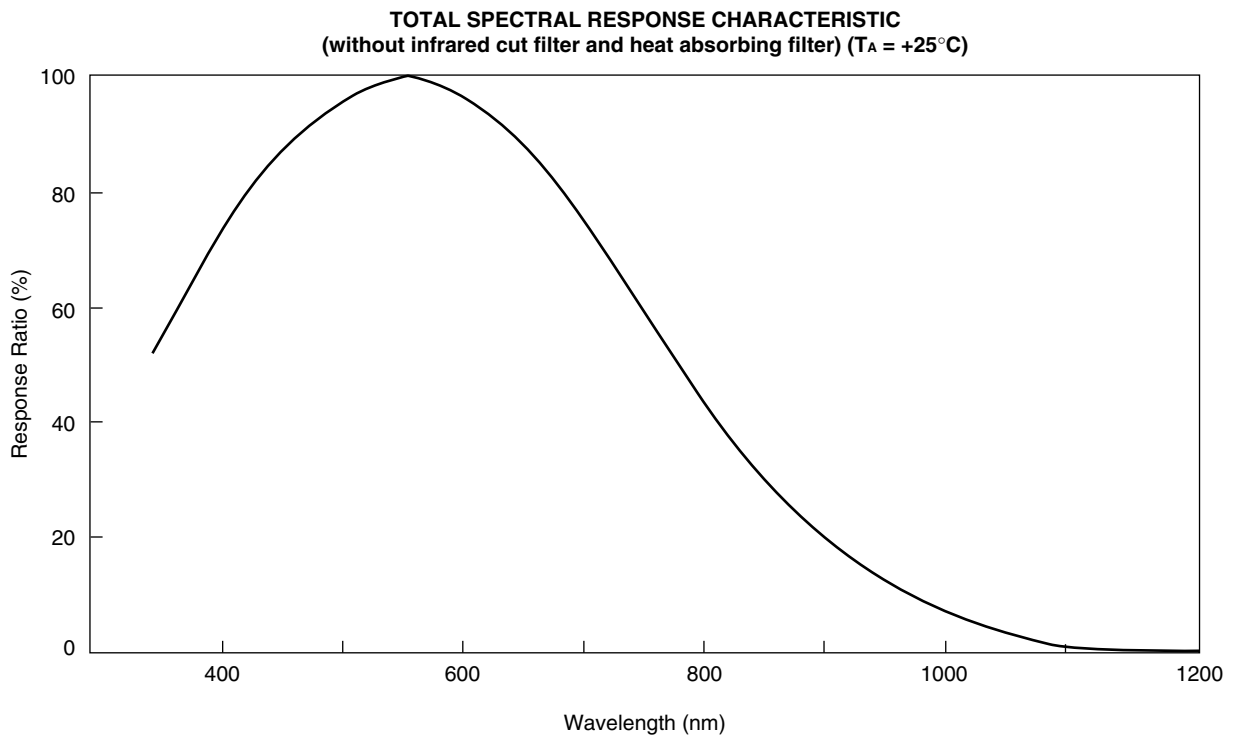
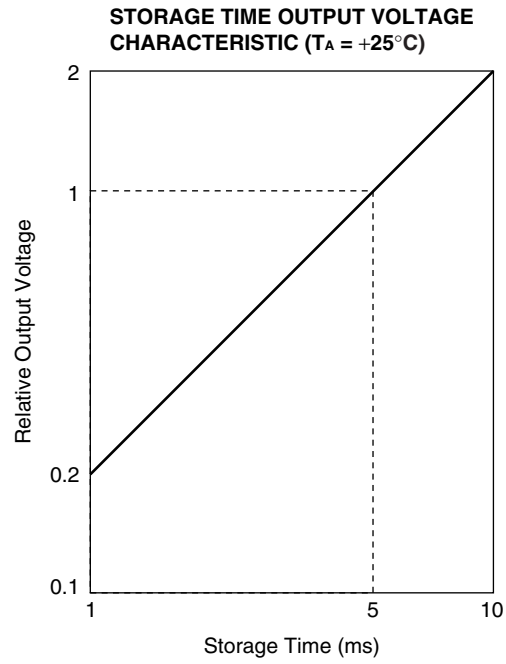
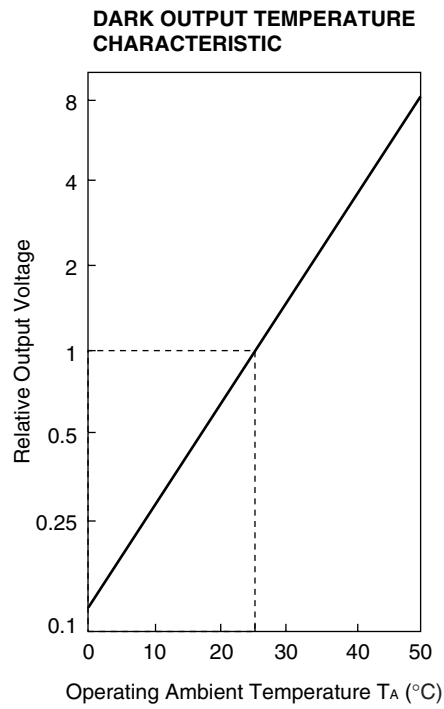
**Caution** This shows timing of  $V_{out1}$  side ( $\phi 2L1$ ,  $\phi R1$ ,  $\phi CP1$ ,  $V_{out1}$ ). The definition of  $V_{out2}$  side ( $\phi 2L2$ ,  $\phi R2$ ,  $\phi CP2$ ,  $V_{out2}$ ) is equal.

<2> Line clamp operation

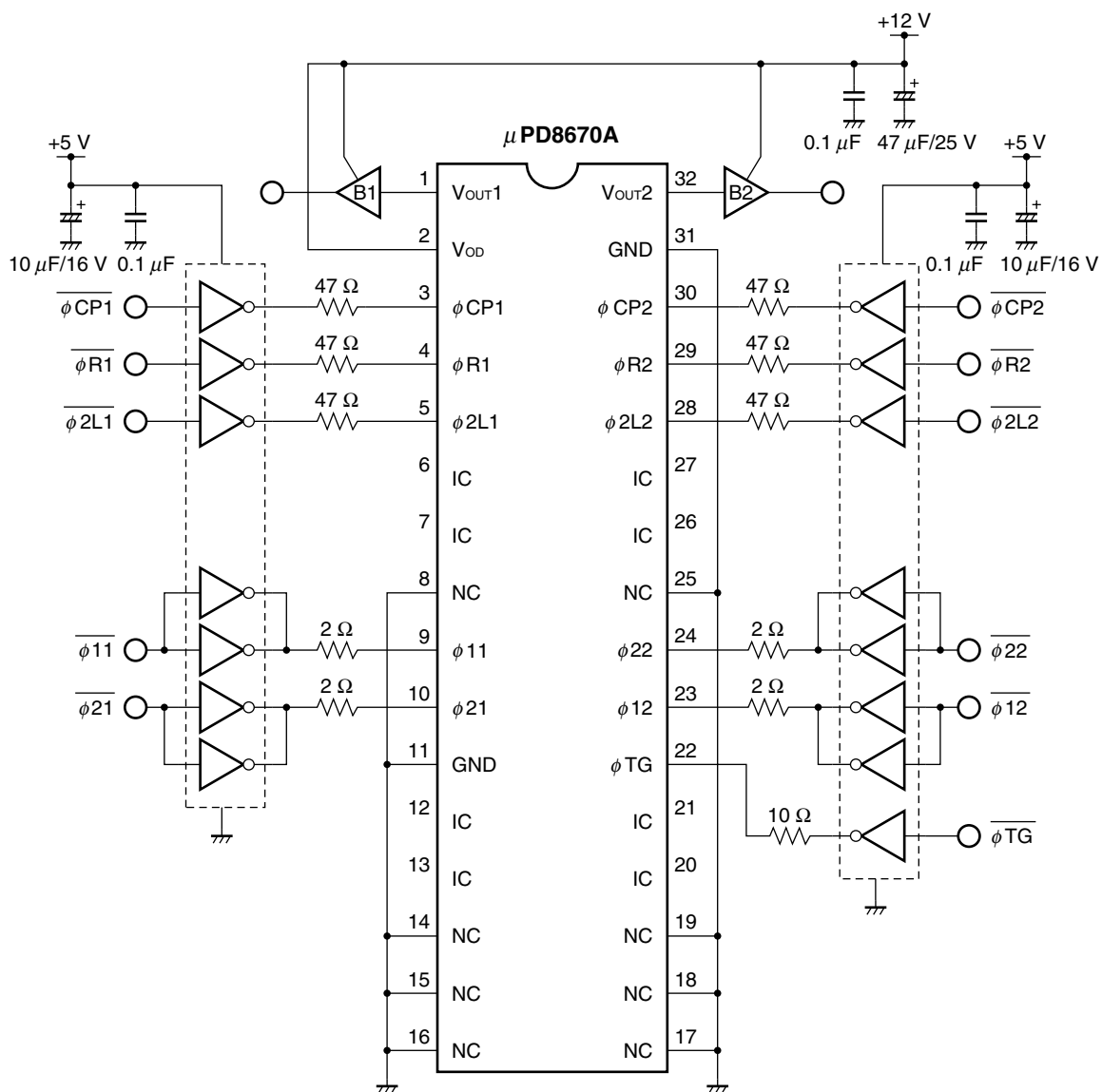


**Caution** This shows timing of  $V_{out1}$  side ( $\phi 2L1$ ,  $\phi R1$ ,  $\phi CP1$ ,  $V_{out1}$ ). The definition of  $V_{out2}$  side ( $\phi 2L2$ ,  $\phi R2$ ,  $\phi CP2$ ,  $V_{out2}$ ) is equal.

STANDARD CHARACTERISTIC CURVES (Reference Value)

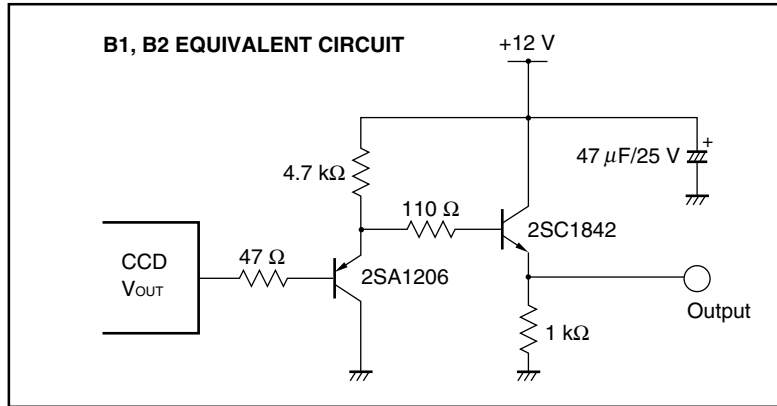


APPLICATION CIRCUIT EXAMPLE



- Cautions**
1. Leave pins 6, 7, 12, 13, 20, 21, 26 and 27 (IC) unconnected.
  2. Connect the No connection pins (NC) to GND.

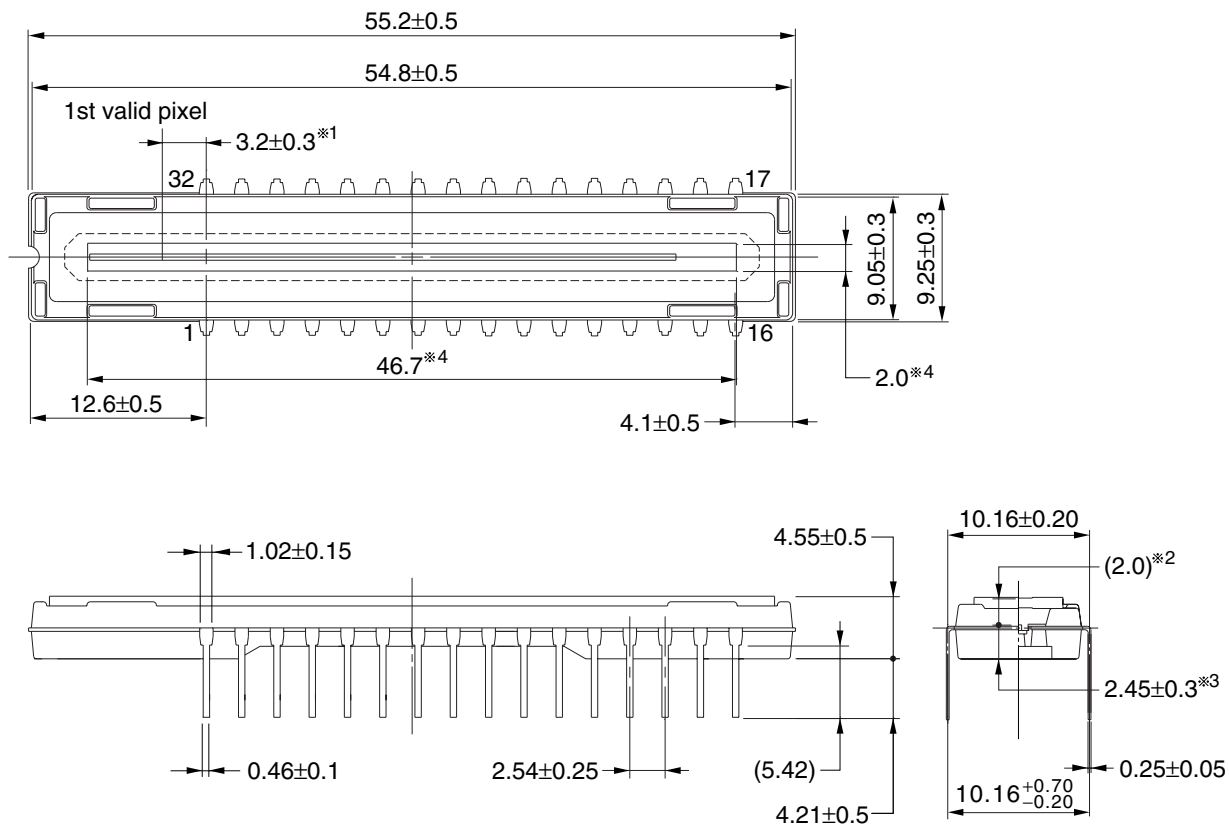
**Remark** The inverters shown in the above application circuit example are the 74AC04.



PACKAGE DRAWING

μPD8670CY, μPD8670ACY  
 CCD LINEAR IMAGE SENSOR 32-PIN PLASTIC DIP (10.16 mm (400) )

(Unit : mm)



Name	Dimensions	Refractive index
Plastic cap	52.2×6.4×0.8 (0.7 <sup>*5</sup> )	1.5

- ※1 1st valid pixel ↔ The center of the pin1
- ※2 The surface of the CCD chip ↔ The top of the cap
- ※3 The bottom of the package ↔ The surface of the CCD chip
- ※4 Mirror finished surface
- ※5 Thickness of mirror finished surface

32C-1CCD-PKG10-2

**RECOMMENDED SOLDERING CONDITIONS**

When soldering this product, it is highly recommended to observe the conditions as shown below.

If other soldering processes are used, or if the soldering is performed under different conditions, please make sure to consult with our sales offices.

**Type of Through-hole Device**

**μPD8670ACY-A : CCD linear image sensor 32-pin plastic DIP (10.16 mm (400))**

Process	Conditions
Partial heating method	Pin temperature : 350°C or below, Heat time : 3 seconds or less (per pin)

- Cautions**
1. During assembly care should be taken to prevent solder or flux from contacting the plastic cap. The optical characteristics could be degraded by such contact.
  2. Soldering by the solder flow method may have deleterious effects on prevention of plastic cap soiling and heat resistance. So the method cannot be guaranteed.

**NOTES ON HANDLING THE PACKAGES**

**① DUST AND DIRT PROTECTING**

The optical characteristics of the CCD will be degraded if the cap is scratched during cleaning. Don't either touch plastic cap surface by hand or have any object come in contact with plastic cap surface. Should dirt stick to a plastic cap surface, blow it off with an air blower. For dirt stuck through electricity ionized air is recommended. And if the plastic cap surface is grease stained, clean with our recommended solvents.

**○ CLEANING THE PLASTIC CAP**

Care should be taken when cleaning the surface to prevent scratches. We recommend cleaning the cap with a soft cloth moistened with one of the recommended solvents below. Excessive pressure should not be applied to the cap during cleaning. If the cap requires multiple cleanings it is recommended that a clean surface or cloth be used.

**○ RECOMMENDED SOLVENTS**

The following are the recommended solvents for cleaning the CCD plastic cap. Use of solvents other than these could result in optical or physical degradation in the plastic cap. Please consult your sales office when considering an alternative solvent.

Solvents	Symbol
Ethyl Alcohol	EtOH
Methyl Alcohol	MeOH
Isopropyl Alcohol	IPA
N-methyl Pyrrolidone	NMP

**② MOUNTING OF THE PACKAGE**

The application of an excessive load to the package may cause the package to warp or break, or cause chips to come off internally. Particular care should be taken when mounting the package on the circuit board. Don't have any object come in contact with plastic cap. You should not reform the lead frame. We recommended to use a IC-inserter when you assemble to PCB.

Also, be care that the any of the following can cause the package to crack or dust to be generated.

1. Applying heat to the external leads for an extended period of time with soldering iron.
2. Applying repetitive bending stress to the external leads.
3. Rapid cooling or heating

**③ OPERATE AND STORAGE ENVIRONMENTS**

Operate in clean environments. CCD image sensors are precise optical equipment that should not be subject to mechanical shocks. Exposure to high temperatures or humidity will affect the characteristics. So avoid storage or usage in such conditions.

Keep in a case to protect from dust and dirt. Dew condensation may occur on CCD image sensors when the devices are transported from a low-temperature environment to a high-temperature environment. Avoid such rapid temperature changes.

For more details, refer to our document "Review of Quality and Reliability Handbook" (C12769E)

**④ ELECTROSTATIC BREAKDOWN**

CCD image sensor is protected against static electricity, but destruction due to static electricity is sometimes detected. Before handling be sure to take the following protective measures.

1. Ground the tools such as soldering iron, radio cutting pliers of or pincer.
2. Install a conductive mat or on the floor or working table to prevent the generation of static electricity.
3. Either handle bare handed or use non-chargeable gloves, clothes or material.
4. Ionized air is recommended for discharge when handling CCD image sensor.
5. For the shipment of mounted substrates, use box treated for prevention of static charges.
6. Anyone who is handling CCD image sensors, mounting them on PCBs or testing or inspecting PCBs on which CCD image sensors have been mounted must wear anti-static bands such as wrist straps and ankle straps which are grounded via a series resistance connection of about 1 MΩ.

[ MEMO ]

[ MEMO ]

## NOTES FOR CMOS DEVICES

**① VOLTAGE APPLICATION WAVEFORM AT INPUT PIN**

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between  $V_{IL}$  (MAX) and  $V_{IH}$  (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between  $V_{IL}$  (MAX) and  $V_{IH}$  (MIN).

**② HANDLING OF UNUSED INPUT PINS**

Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to  $V_{DD}$  or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

**③ PRECAUTION AGAINST ESD**

A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

**④ STATUS BEFORE INITIALIZATION**

Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

**⑤ POWER ON/OFF SEQUENCE**

In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current.

The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

**⑥ INPUT OF SIGNAL DURING POWER OFF STATE**

Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

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