

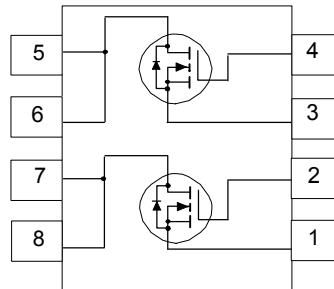
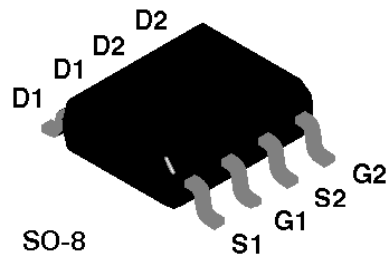
## NDS9959 Dual N-Channel Enhancement Mode Field Effect Transistor

### General Description

These N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulses in the avalanche and commutation modes. These devices are particularly suited for low voltage applications such as DC motor control and DC/DC conversion where fast switching, low in-line power loss, and resistance to transients are needed.

### Features

- 2.0A, 50V.  $R_{DS(ON)} = 0.3\Omega @ V_{GS} = 10V$
- High density cell design for extremely low  $R_{DS(ON)}$ .
- High power and current handling capability in a widely used surface mount package.
- Dual MOSFET in surface mount package.



### Absolute Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	NDS9959	Units
$V_{DS}$	Drain-Source Voltage	50	V
$V_{GS}$	Gate-Source Voltage	$\pm 20$	V
$I_D$	Drain Current - Continuous @ $T_A = 25^\circ\text{C}$ (Note 1a)	$\pm 2.0$	A
	- Continuous @ $T_A = 70^\circ\text{C}$ (Note 1a)	$\pm 1.6$	
	- Pulsed @ $T_A = 25^\circ\text{C}$	$\pm 8$	
$P_D$	Power Dissipation for Dual Operation	2	W
	Power Dissipation for Single Operation (Note 1a)	1.6	
	(Note 1b)	1	
	(Note 1c)	0.9	
$T_J, T_{STG}$	Operating and Storage Temperature Range	-55 to 150	$^\circ\text{C}$

### THERMAL CHARACTERISTICS

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	78	$^\circ\text{C/W}$
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Note 1)	40	$^\circ\text{C/W}$

**Electrical Characteristics** ( $T_A = 25^\circ\text{C}$  unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
$V_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	50			V
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 40\text{ V}, V_{GS} = 0\text{ V}$			2	$\mu\text{A}$
		$T_J = 55^\circ\text{C}$			25	$\mu\text{A}$
$I_{GSSF}$	Gate - Body Leakage, Forward	$V_{GS} = 20\text{ V}, V_{DS} = 0\text{ V}$			100	nA
$I_{GSSR}$	Gate - Body Leakage, Reverse	$V_{GS} = -20\text{ V}, V_{DS} = 0\text{ V}$			-100	nA
ON CHARACTERISTICS (Note2)						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	2	3	4	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\text{ V}, I_D = 1.5\text{ A}$			0.3	$\Omega$
		$V_{GS} = 5\text{ V}, I_D = 0.6\text{ A}$			0.5	
$I_{D(on)}$	On-State Drain Current	$V_{GS} = 10\text{ V}, V_{DS} = 5\text{ V}$	8			A
$g_{FS}$	Forward Transconductance	$V_{DS} = 15\text{ V}, I_D = 2.0\text{ A}$	1	2.7		S
DYNAMIC CHARACTERISTICS						
$C_{iss}$	Input Capacitance	$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$		152	250	pF
$C_{oss}$	Output Capacitance			50	85	pF
$C_{rss}$	Reverse Transfer Capacitance			12	25	pF
SWITCHING CHARACTERISTICS (Note 2)						
$t_{D(on)}$	Turn - On Delay Time	$V_{DD} = 30\text{ V}, I_D = 0.6\text{ A},$ $V_{GS} = 10\text{ V}, R_L = 50\text{ }\Omega,$ $R_{GEN} = 6\text{ }\Omega$		4	40	ns
$t_r$	Turn - On Rise Time			8	70	ns
$t_{D(off)}$	Turn - Off Delay Time			9	100	ns
$t_f$	Turn - Off Fall Time			11	70	ns
$Q_g$	Total Gate Charge	$V_{DS} = 25\text{ V},$ $I_D = 1.3\text{ A}, V_{GS} = 10\text{ V}$		4.3	15	nC
$Q_{gs}$	Gate-Source Charge			1.1		nC
$Q_{gd}$	Gate-Drain Charge			1.5		nC

Electrical Characteristics (T<sub>A</sub> = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
I <sub>S</sub>	Maximum Continuous Drain-Source Diode Forward Current				1.8	A
V <sub>SD</sub>	Drain-Source Diode Forward Voltage	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 1.25 A (Note 2)		0.84	1.2	V
t <sub>rr</sub>	Reverse Recovery Time	V <sub>GS</sub> = 0V, I <sub>F</sub> = 1.25 A, dI <sub>F</sub> /dt = 100 A/μs			100	ns

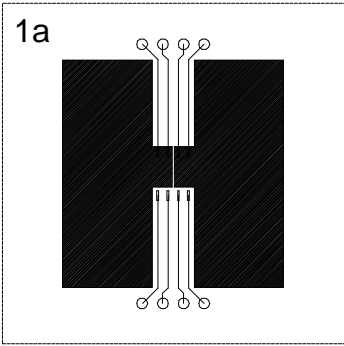
Notes:

1. R<sub>θJA</sub> is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. R<sub>θJC</sub> is guaranteed by design while R<sub>θCA</sub> is determined by the user's board design.

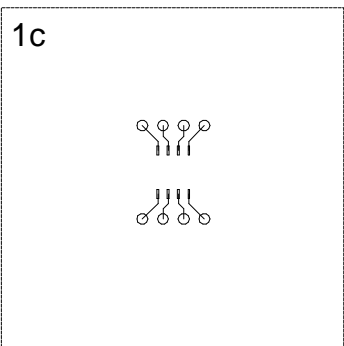
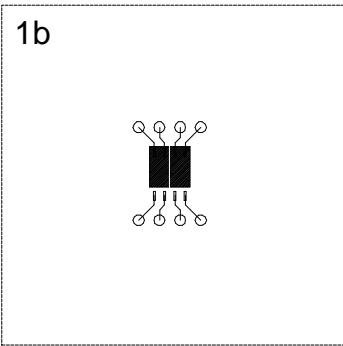
$$P_D(t) = \frac{T_J - T_A}{R_{\theta J A}(t)} = \frac{T_J - T_A}{R_{\theta J C} + R_{\theta CA}(t)} = I_D^2(t) \times R_{DS(on)} @ T_J$$

Typical R<sub>θJA</sub> for single device operation using the board layouts shown below on 4.5"x5" FR-4 PCB in a still air environment:

- a. 78°C/W when mounted on a 0.5 in² pad of 2oz copper.
- b. 125°C/W when mounted on a 0.02 in² pad of 2oz copper.
- c. 135°C/W when mounted on a 0.003 in² pad of 2oz copper.



Scale 1 : 1 on letter size paper



2. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2.0%.

## Typical Electrical Characteristics

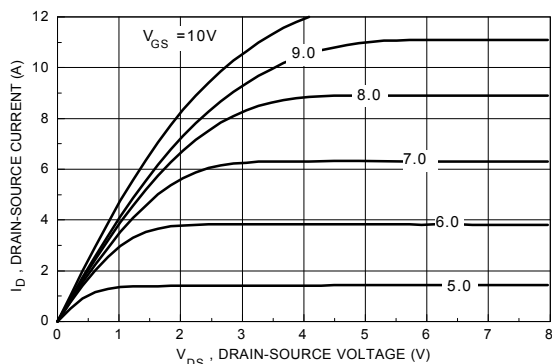


Figure 1. On-Region Characteristics.

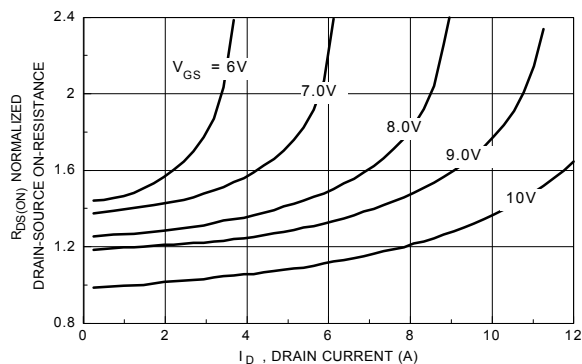


Figure 2. On-Resistance Variation with Gate Voltage and Drain Current.

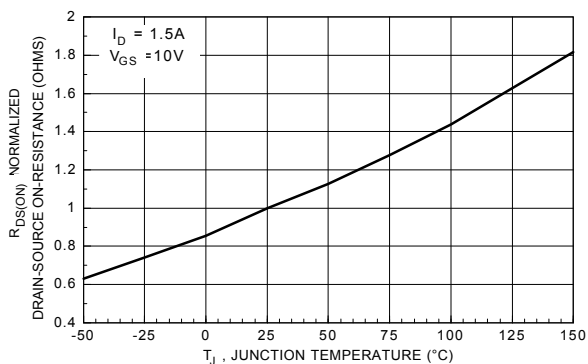


Figure 3. On-Resistance Variation with Temperature.

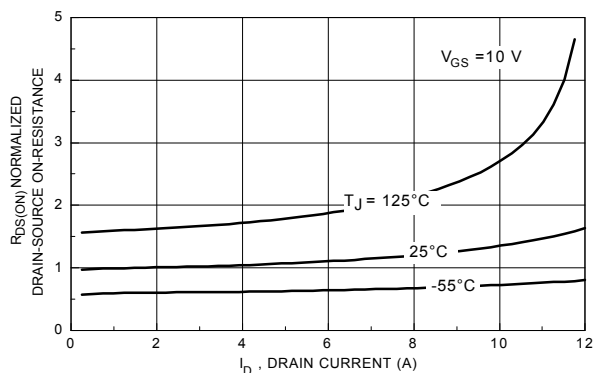


Figure 4. On-Resistance Variation with Drain Current and Temperature.

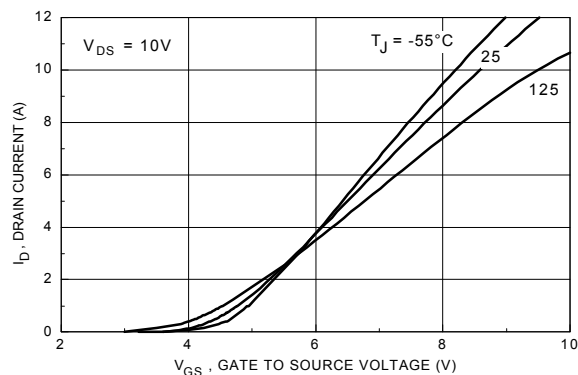


Figure 5. Transfer Characteristics.

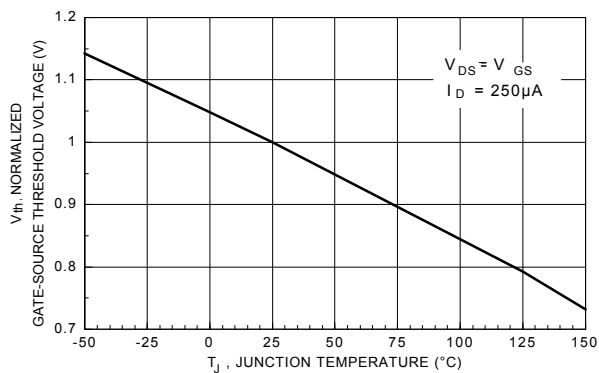
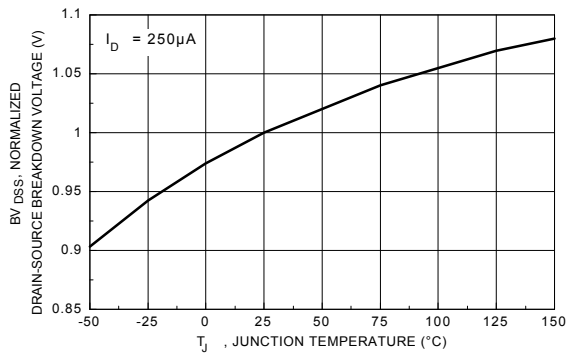
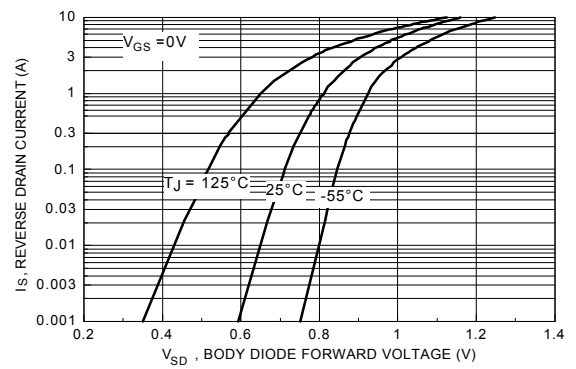


Figure 6. Gate Threshold Variation with Temperature.

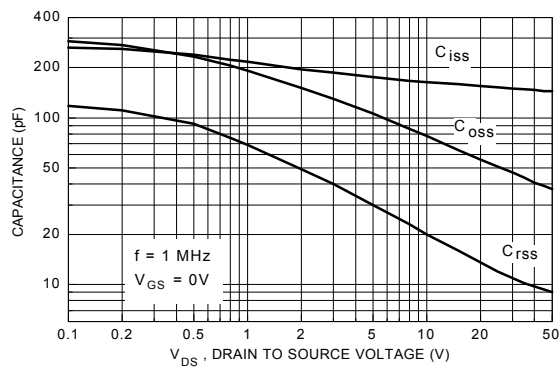
## Typical Electrical Characteristics (continued)



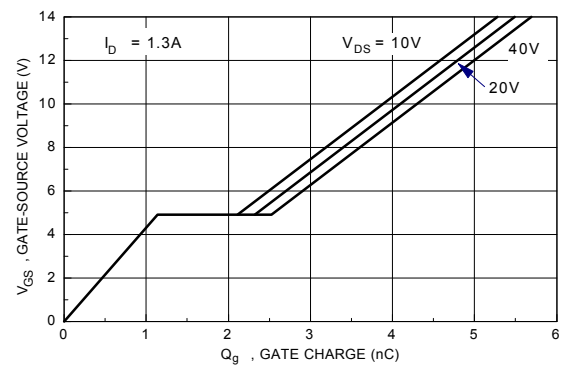
**Figure 7. Breakdown Voltage Variation with Temperature.**



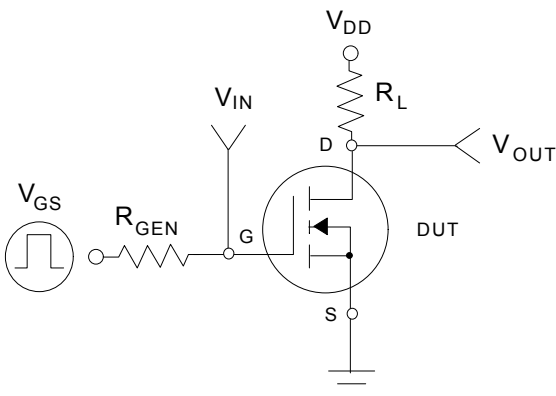
**Figure 8. Body Diode Forward Voltage Variation with Current and Temperature**



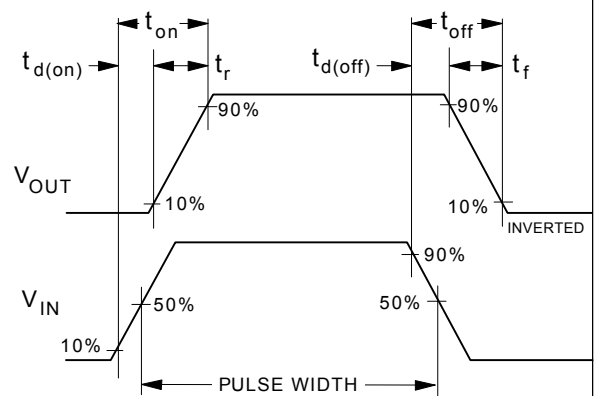
**Figure 9. Capacitance Characteristics.**



**Figure 10. Gate Charge Characteristics.**

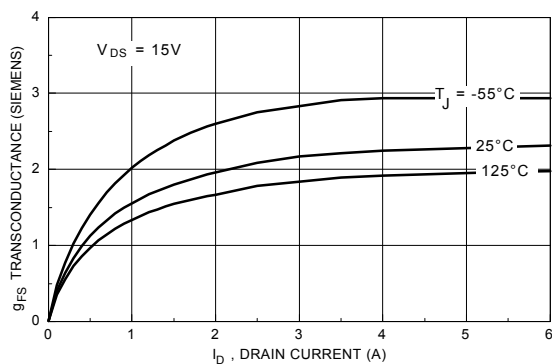


**Figure 11. Switching Test Circuit**

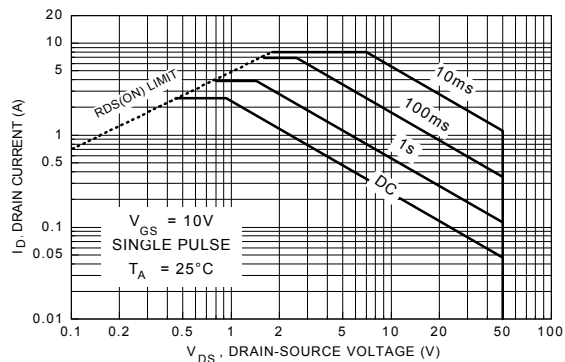


**Figure 12. Switching Waveforms**

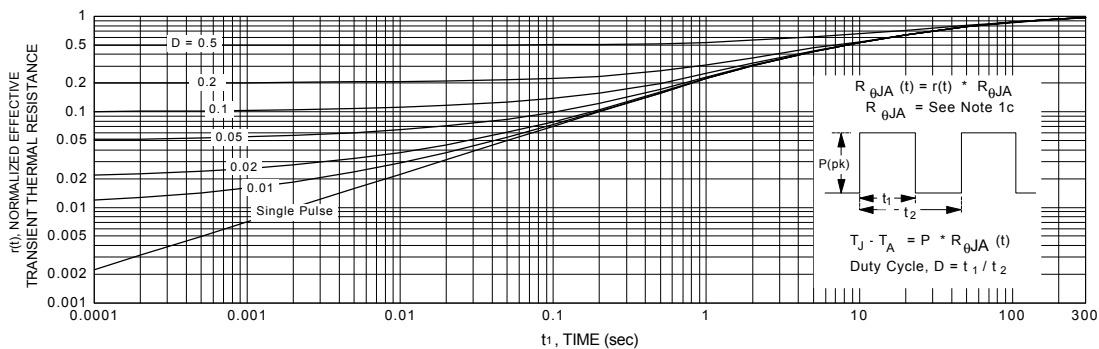
## Typical Electrical Characteristics (continued)



**Figure 13. Transconductance Variation with Drain Current.**



**Figure 14. Maximum Safe Operating Area.**



**Figure 15. Transient Thermal Response Curve.**

Note: Thermal characterization performed using the conditions described in note 1c. Transient thermal response will change depending on the circuit board design.

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