SMARTMESH® WIRELESSHART LTP5900-WHM

2.4 GHz 802.15.4 Wireless Mote

About SmartMesh WirelessHART

Dust Networks' SmartMesh® WirelessHART is an industry-leading wireless networking solution designed for critical monitoring and control applications. WirelessHART serves a wide range of applications from renewable energy generation, such as solar and wind power, to factory machine health monitoring and data center HVAC energy management. The SmartMesh WirelessHART system delivers dynamic network optimization and intelligent routing to achieve unsurpassed levels of wireless network scalability, system-wide reliability and low latency, coupled with industrial-class security. Additionally, ultra-low power operation permits even greater deployment flexibility for wire-free applications.

Product Description—LTP5900

The LTP5900 mote module combines Dust Networks' robust sensor networking solution breakthrough Eterna™ SoC technology in an easy-to-integrate 22-pin module. As part of the SmartMesh WirelessHART system, the LTP5900 enables customers to integrate a standards-based wireless network into sensors and actuators to provide scalable bidirectional communications.

The LTP5900 is designed for use in line-powered, battery-powered, or energy-scavenging sensor and actuator applications that demand reliable performance and ultra-low power operation. With Dust Networks' innovative IEEE 802.15.4-compliant design and integrated power amplifier, the LTP5900 enables a decade of battery life on two AA batteries. All motes function as wireless routers, enabling a redundant, high performance, full-mesh topology.

The LTP5900 integrates all radio circuitry components, including an MMCX-type antenna connector to eliminate the need for complex RF design. To accelerate customer development time and reduce development costs, Dust Networks provides a fully engineered RF solution, comprehensive APIs, and complete development documentation.

Key Product Features

WirelessHART Compliance

- Interoperable with WirelessHART Devices

Highly Scalable

- Automatic network formation—new motes join automatically from anywhere in the network
- All motes are wireless routers, providing a full-mesh network that easily scales to tens of thousands of motes per square km
- Time-synchronized communication across 15 channels virtually eliminates in-network collisions, allowing for dense deployments in overlapping radio space

Superior Reliability

- SmartMesh WirelessHART Intelligent Networking Platform enables greater than 99.99% network reliability even in the most challenging monitoring and control environments
- Time-synchronized channel hopping minimizes the impact of crippling multipath interference in dynamic RF environments

Ultra-low Power Operation

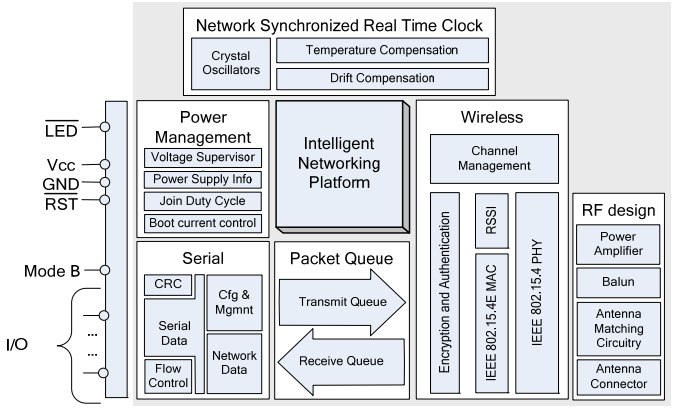
- Industry-leading radio technology capable of line-powered, battery-powered, or energy-scavenging operation
- Automatic network-wide coordination optimizes power consumption, enabling a decade of network operation on two Lithium AA batteries

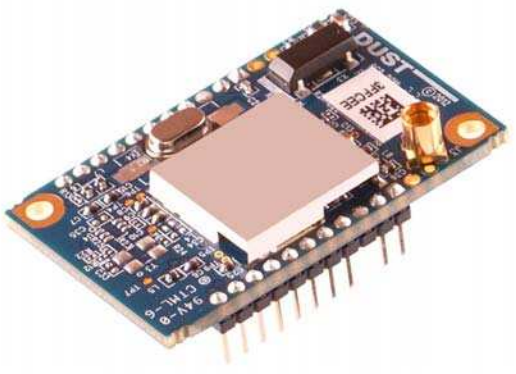
Easy to Integrate and Deploy

- Fully engineered RF, with power amplifier (PA), balun, crystals, antenna matching circuitry and antenna connector
- Comprehensive APIs provide rich and flexible functionality to ease software development and device integration

Secure Global Market Solution

- Fully engineered RF, with power amplifier (PA), balun, crystals, and antenna matching circuitry
- AES-128 bit encryption





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1.0 Absolute Maximum Ratings

The absolute maximum ratings shown below should not be violated under any circumstances. Permanent damage to the device may be caused by exceeding one or more of these parameters.

Unless otherwise noted, all voltages in Table 1 are made relative to V_{SS}.

Table 1 Absolute Maximum Ratings

Parameter	Min	Typ	Max	Units	Comments
Supply voltage (V_{DD} to V_{SS})	–0.3		3.76	V	
Voltage on any digital I/O pin	–0.3		V_{DD} + 0.3 up to 3.6	V	
Input RF level			10	dBm	Input power at antenna connector
Storage temperature range	–40		+85	°C	
Lead temperature			+245	°C	For 10 seconds
VSWR of antenna			3:1		
ESD protection					
Antenna pad			±8000	V	HBM
All other pads			±2	kV	HBM
			±200	V	CDM

Caution! ESD sensitive device. Precaution should be used when handling the device to prevent permanent damage.

2.0 Normal Operating Conditions

Unless otherwise noted, Table 2 assumes V_{DD} is 3.6 V and temperature is 25 °C.

Table 2 Normal Operating Conditions

Parameter	Min	Typ	Max	Units	Comments
Operational supply voltage range (between V_{DD} and V_{SS})	2.75		3.76	V	Including noise and load regulation
Voltage supply noise			200	mV_{p-p}	50 Hz to 2 MHz
Voltage supervisor trip point		1.5		V	Reset trip point
Peak current					
		4.4		mA	Searching for network, typically 150 ms on and 2850 ms in doze*
During Power on Reset			12	mA	max 750 uS + V_{DD} rise time from 1 V to 1.9 V.
Power amplifier enabled		9.5		mA	TX, 5 ms maximum
Power amplifier enabled			12	mA	TX, 5 ms maximum, +85 °C, 3.3 V
Power amplifier disabled		5.2		mA	TX, 5 ms maximum
Reset			1.5	uA	$\overline{RST}$ asserted, following PoR completion
Operating temperatures	-40		+85	°C	
Maximum allowed temperature ramp during operation			8	°C/min	-40 °C to +85 °C
Operating relative humidity	10		90	% RH	Non-condensing
* The duration of doze time and “on” time is determined by the joinDutyCycle command in the mote serial API. Refer to the *SmartMesh IA-510 Mote Serial API Guide* for details.					

Unless otherwise noted, Table 3 assumes V_{DD} is 3.6 V.

Table 3 Current Consumption

Parameter	Min	Typ	Max	Units	Comments
Transmit					
Power amplifier enabled		9.5		mA	
Power amplifier disabled		5.2		mA	
Receive		4.4		mA	

3.0 Electrical Specifications

Table 4 Device Load

Parameter	Min	Typ	Max	Units	Comments
Total capacitance			6	µF	V_{DD} to V_{SS}
Total inductance			4.9	µH	V_{DD} to V_{SS}

Unless otherwise noted, V_{DD} is 3.6 V and temperature is –40 °C to +85 °C.

Table 5 Digital I/O Type 1

Digital Signal	Min	Typ	Max	Units	Comments
V_{IL} (low-level input voltage)	–0.3		0.6	V	
V_{IH} (high-level input voltage)	V_{DD}-0.3		V_{DD} + 0.3	V	
V_{OL} (low-level output voltage)			0.4	V	$I_{OL(max)}$ = 1.2 mA
V_{OH} (high-level output voltage)	V_{DD}-0.3			V	$I_{OH(max)}$ = −1.8 mA
Input leakage current		50		nA	25 °C

4.0 Radio

4.1 Detailed Radio Specifications

Table 6 Detailed Radio Specifications

Parameter	Min	Typ	Max	Units	Comments
Operating frequency	2.4000		2.4835	GHz	
Number of channels		15			
Channel separation		5		MHz	
Occupied channel bandwidth		2.7		MHz	At –20 dBc
Frequency Accuracy	-40		+40	ppm	
Modulation					IEEE 802.15.4 DSSS
Raw data rate		250		kbps	
Receiver operating maximum input level		0		dBm	
Receiver sensitivity		–95.0		dBm	At 50% PER, V_{DD} = 3 V, 25 °C
		–92.5		dBm	At 1% PER, V_{DD} = 3 V, 25 °C
Output power, conducted					
Power amplifier enabled		+8		dBm	V_{DD} = 3.6 V, 25 °C
Power amplifier disabled		0		dBm	V_{DD} = 3.6 V, 25 °C

Parameter	Min	Typ	Max	Units	Comments
Range*					
Power amplifier enabled:					25 °C, 50% RH, +2 dBi omni-directional antenna
Indoor†		100		m	
Outdoor†		300		m	
Free space		1200		m	
Power amplifier disabled:					
Indoor†		25		m	
Outdoor†		200		m	
Free space		350		m	

* Actual RF range performance is subject to a number of installation-specific variables including, but not restricted to ambient temperature, relative humidity, presence of active interference sources, line-of-sight obstacles, near-presence of objects (for example, trees, walls, signage, and so on) that may induce multipath fading. As a result, actual performance varies for each instance.

† 1 meter above ground.

4.2 Antenna Specifications

A MMCX-compatible male connector is provided on board for the antenna connection. The antenna must meet specifications in Table 7. For a list of FCC-approved antennae, see section 10.1.2.

Table 7 Antenna Specifications

Parameter	Value
Frequency range	2.4 – 2.4835 GHz
Impedance	50 Ω
Maximum VSWR	3:1
Connector	MMCX*

* The LTP5900 can accommodate the following RF mating connectors:
- MMCX straight connector such as Johnson 135-3402-001, or equivalent
- MMCX right angle connector such as Tyco 1408149-1, or equivalent

When the mote is placed inside an enclosure, the antenna should be mounted such that the radiating portion of the antenna protrudes from the enclosure. The antenna should be connected using a MMCX connector on a coaxial cable. For optimum performance, the antenna should be positioned vertically when installed.

5.0 Pinout

The LTP5900 has two 11-pin Samtec MTMM-111-04-S-S-175-3 (or equivalent) connectors on the bottom side for handling all of the I/O. The third pin in each of the connectors is not populated, and serves as a key for alignment. The connectors are mounted on opposite edges of the long axis of the LTP5900.

5.1 LTP5900 Pinout

The LTP5900 provides a bidirectional flow-controlled serial interface (see section 8.3 Settable I/O Modes).

Table 8 LTP5900 Pin Functions

Pin Number	Pin Name	Description	I/O Type	Direction	Pin State in Deep Sleep†
1	V_{SS}	Ground	Power	–	–
2	V_{DD}	Power	Power	–	–
3	KEY (no pin)	–	–	–	–
4	RX	UART Rx	1	In	–
5	TX	UART Tx	1	Out	V_{DD}
6	*Reserved*	No connect	–	–	–

Pin Number	Pin Name	Description	I/O Type	Direction	Pin State in Deep Sleep[†]
7	$\overline{\text{MT\_RTS}}$	UART active low mote ready to send	1	Out	V_{DD}
8	$\overline{\text{MT\_CTS}}$	UART active low mote clear to send	1	Out	V_{DD}
9	$\overline{\text{SP\_CTS}}$	UART active low serial peripheral clear to send	1	In	–
10	$\overline{\text{TIME}}$	Falling edge time request	1	In	–
11	Mode_pin_B	Selects between Mode 1 & Mode 3 operation	1	In	–
12	$\overline{\text{FLASH\_P\_EN}}$	Active low flash power enable	1	In	–
13	*Reserved*	No connect	–	–	–
14	*Reserved*	No connect	–	–	–
15	*Reserved*	No connect	–	–	–
16	*Reserved*	No connect	–	–	–
17	SCK	SPI clock	1	In	–
18	MOSI	SPI master out slave in serial data	1	In	–
19	MISO	SPI master in slave out serial data	1	Out	–
20	KEY (no pin)	–	–	–	–
21	$\overline{\text{SPI\_CS}}$	Active low flash chip select	1	In	–
22	$\overline{\text{RST}}$	Active low reset	1	In	–

[†] Deep sleep is the lowest possible power state, with V_{DD} and GND connected. The mote microprocessor and radio are inactive, and the mote must be awakened using the /RST signal (for more information see the lowPowerSleep command in the *IA-510 Mote Serial API Guide*).

The $\overline{\text{RST}}$ input pin is internally pulled up and connecting it is optional. When driven active low, the mote is hardware reset until the signal is de-asserted. Refer to section 7.1 for timing requirements on the $\overline{\text{RST}}$ pin. Note that the mote may also be reset using the mote serial command (see the *SmartMesh IA-510 Mote Serial API Guide*).

The $\overline{\text{TIME}}$ input pin is optional, and must either be driven or pulled up with a 5.1 MΩ resistor. Unless noted otherwise, all signals are active low.

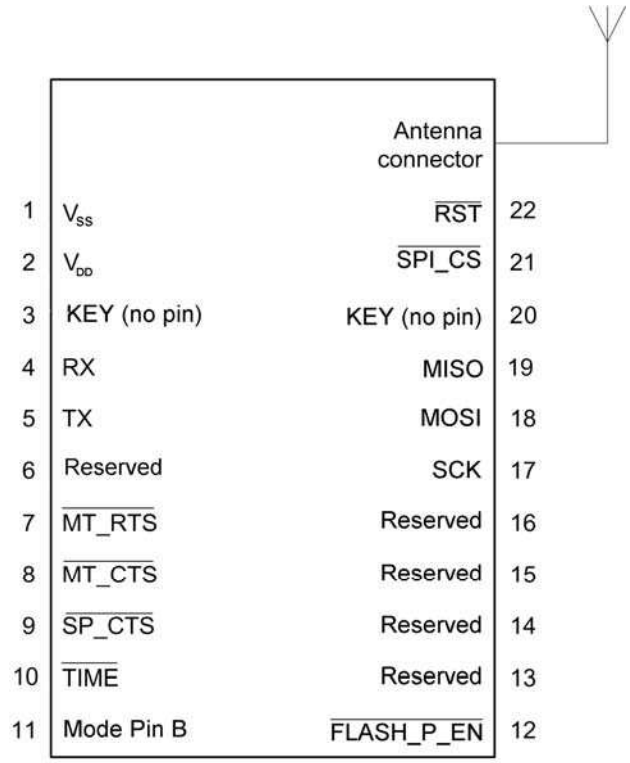

Figure 1 LTP5900 Package with Pin Labels

6.0 Power Supply Design

Care should be taken in cases where the mote inputs will be driven to logic level high. Refer to the *040-0067 SmartMesh IA-510 Mote Serial API Guide* for information on mote bring-up and power cycling.

7.0 Mote Boot Up

7.1 Power-on Sequence

The LTP5900 has internal power-on reset circuits that ensure that the mote will properly boot. External resetting of the device is not required and not recommended.

Table 9 Power-on Sequence

Parameter	Min	Typ	Max	Units	Comments
$\overline{RST}$ pulse width	125			µs	Reset timing

7.2 Inrush Current

During power on, the mote can be modeled as a lumped impedance, as shown in Figure 2. With a source impedance (R_{src}) of 1 Ω, the inrush current on the mote appears as shown in Figure 3.

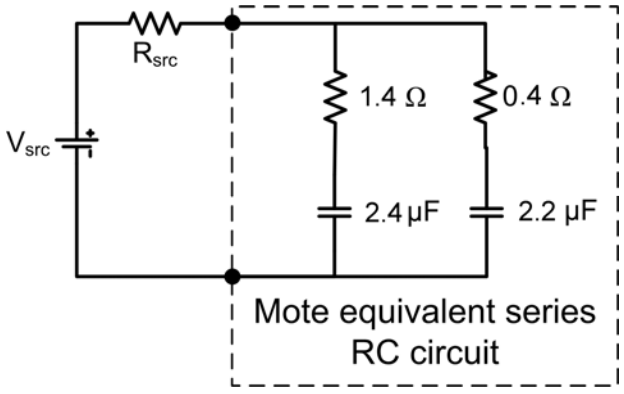

Figure 2 LTP5900 Equivalent Series RC Circuit

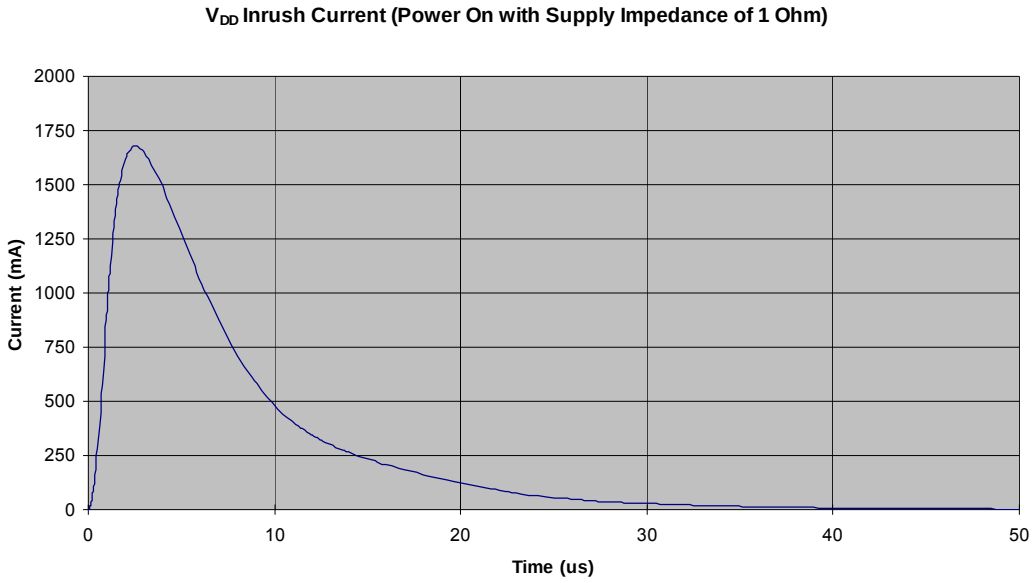

Figure 3 V_{DD} Inrush Current

7.3 Mote Boot Sequence

Following the negation of $\overline{RST}$ the mote completes its boot-up process by loading the application image and loading the operating parameters. The LTP5900 lowers average current consumption by spreading the boot operation over time. This method supports systems with supplies having a maximum DC current less than the peak current required by the LTP5900. These systems must store enough charge to maintain the supply through the LTP5900's peak current consumption. For more information, contact your Dust Networks applications engineer. The maximum "average current" consumption for the LTP5900 is defined by the maximum total charge Q consumed over a sliding window in time, T_{window}.

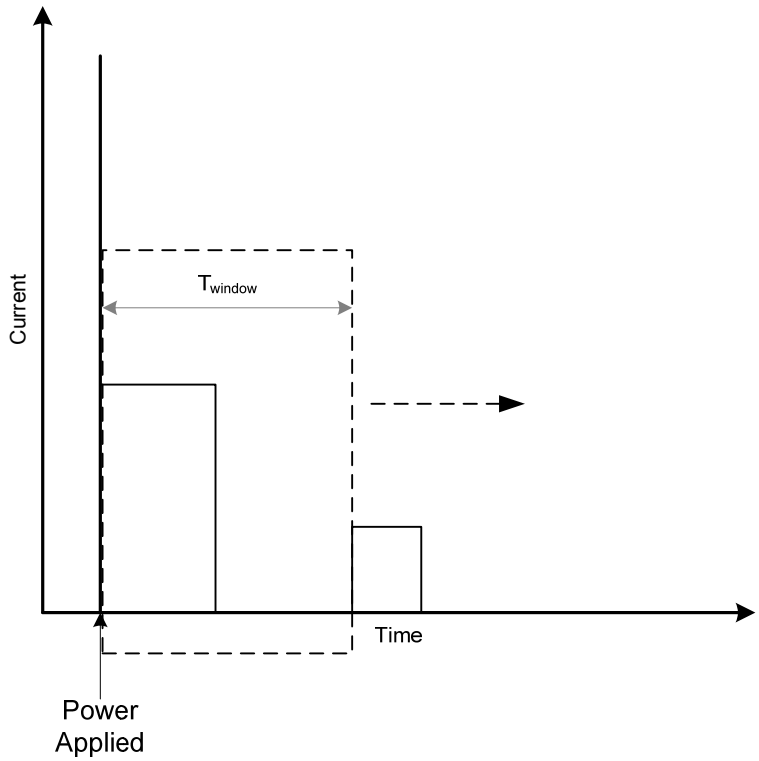

Figure 4 Boot Sequence

Table 10 Boot Sequence Parameters

Parameter	Min	Typ	Max	Units	Comments
t_{boot_delay}		3	5	s	The time between mote power greater than 1.9 V and serial interface availability.
Q			200	uC	T_{window} = 0.56 seconds

7.4 Serial Interface Boot Up

7.4.1 LTP5900 Serial Interface Boot Up

Upon LTP5900 power up, the $\overline{\text{MT\_CTS}}$ line is high (inactive). The LTP5900 serial interface boots within t_{boot_delay} (see 7.3 Mote Boot Sequence) of the mote powering up, at which time the LTP5900 will transmit an HDLC boot event packet. Note that full handshake is in effect and is required to receive this packet.

8.0 Interfaces

8.1 Reset Pin

The /RST input pin is internally pulled up. Connecting it is optional; however, in applications operating in the presence of EMI, /RST should be actively driven high. When driven low, the mote hardware is in reset. Note that the mote may also be reset using the mote reset command (0x08). For requirements on reset timing, see section 7.1.

The LTP5900 is a highly sophisticated device and Dust Networks recommends doing resets gracefully. If the device is in the network, a disconnect command (0x07) should be issued before the /RST signal is asserted. This will result in the device rebooting and sending the "boot" event.

The /RST signal may then be asserted since the device is not in the network.

Refer to the *SmartMesh IA-510 LTP5900 Integration Guide* for recommendations on how to connect to the /RST pin, including voltage supervision. For detailed information about mote serial commands, refer to the *SmartMesh IA-510 Mote Serial API Guide*.

8.2 Timestamps

The LTP5900 has the ability to deliver network-wide synchronized timestamps. The LTP5900 sends a time packet (as described in the *SmartMesh IA-510 Mote Serial API Guide*) through its serial interface when one of the following occurs:

- Mote receives an HDLC request to read time
- The $\overline{\text{TIME}}$ signal is asserted

The $\overline{\text{TIME}}$ pin is optional and has the advantage of being more accurate. The value of the timestamp is taken within approximately 1 ms of receiving a $\overline{\text{TIME}}$ signal activation. If the HDLC request is used, due to packet processing the value of the timestamp may be captured several milliseconds after receipt of the packet. Refer to the *IA-510 Mote Serial API Guide* for more information on timestamps.

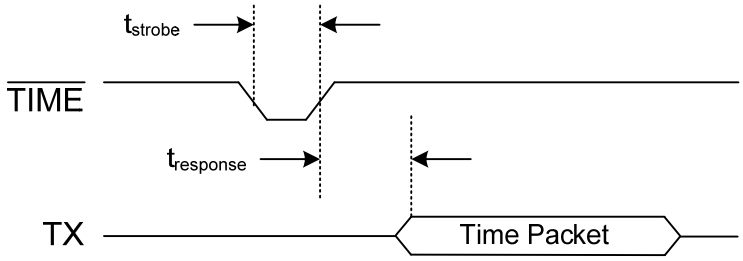

Figure 5 Operation of $\overline{\text{TIME}}$ Pin

Table 11 $\overline{\text{TIME}}$ Timing Values

Variable	Description	Min	Max	Units
t_{strobe}	$\overline{\text{TIME}}$ strobe pulse width	125		µs
$t_{response}$	Negation of Time strobe to start of time packet		100	ms

8.3 Settable I/O Modes

The LTP5900 offers a choice of two I/O modes. The functionality of the interface will be determined by the setting of Mode pin B whose pinout is described in 5.0 Pinout.

Table 12 Mode Pin Settings

Pin	Mode 1	Mode 3
Mode pin B	Externally tied low	Externally tied high

All modes provide a means of transmitting and receiving serial data through the wireless network, as well as a command interface that provides synchronized time stamping, local configuration, and diagnostics.

Mode 1 implements an 8-bit, no parity, 9600 bps baud three, four or five-signal serial interface with bidirectional packet-level flow control operating at 9600 bps. In certain OEM designs, one or two of the serial handshake signals may be optional for reduced pin count, as described in Table 13.

Mode 3 implements an 8-bit, no parity, 115.2 kbps baud five-signal serial interface with bidirectional packet-level flow control and byte-level flow control in the mote-to-microprocessor direction only.

8.3.1 Mode 1: Three/ Four/ Five-signal Serial Interface (9600 bps)

The LTP5900 mode 1 provides a three, four, or five-signal serial interface that is optimized for low-powered embedded applications (and in certain designs may provide a low pin count serial solution). The mode 1 serial interface is comprised of the data pins (TX, RX) as well as handshake pins ($\overline{\text{MT\_RTS}}$, $\overline{\text{MT\_CTS}}$, $\overline{\text{SP\_CTS}}$) used for bidirectional flow control. The $\overline{\text{MT\_RTS}}$ signal is ideal for designs where the microprocessor requires extra time to prepare to receive a packet (for example, the OEM microprocessor sleeps periodically, but requires a wake-up signal prior to receiving a packet). Refer to Table 13 for information on each handshake pin, including details on which pins are optional.

Table 13 Mode 1 Pin Usage

Pin	I/O	Usage
RX	Input	Serial data moving from the microprocessor to the mote.
TX	Output	Serial data moving from the mote to the microprocessor.
$\overline{\text{MT\_RTS}}$	Output	$\overline{\text{MT\_RTS}}$ provides a mechanism to wake up the microprocessor in order to receive a packet. This signal is asserted when the mote is ready to send a serial packet. The signal stays low until the $\overline{\text{SP\_CTS}}$ signal from the microprocessor is detected low by the mote (indicating readiness to receive a packet) or the $t_{MT\_RTS\ to\ SP\_CTS}$ timeout defined in Section 8.3.3 expires. If $\overline{\text{MT\_RTS}}$ times out, it will de-assert $\overline{\text{MT\_RTS}}$, wait for $t_{MT\_RTS\ retry}$ and then re-assert $\overline{\text{MT\_RTS}}$ to attempt to send the serial packet again (see Figure 9). $\overline{\text{MT\_RTS}}$ may be ignored by the microprocessor only if $\overline{\text{SP\_CTS}}$ always stays low.
$\overline{\text{SP\_CTS}}$	Input	$\overline{\text{SP\_CTS}}$ provides packet-level flow control for packets transferred from the mote to the microprocessor. When the microprocessor is capable of receiving a packet it should assert the $\overline{\text{SP\_CTS}}$ signal. $\overline{\text{SP\_CTS}}$ may be externally tied low (reducing pin count) only if the microprocessor is always ready to receive a serial packet.
$\overline{\text{MT\_CTS}}$	Output	$\overline{\text{MT\_CTS}}$ provides packet-level flow control for packets transferred from the microprocessor to the mote that are destined for transfer over the network. Upon reset, following boot the mote will negate $\overline{\text{MT\_CTS}}$ until the mote establishes a wireless network connection. During operation, the mote will negate $\overline{\text{MT\_CTS}}$ if the mote does not have sufficient buffering to accept another packet. $\overline{\text{MT\_CTS}}$ will also remain high if the mote is not part of the network. The microprocessor must check that the $\overline{\text{MT\_CTS}}$ pin is low before initiating each serial packet for wireless transmission. Note that the mote may receive local serial packets at any time regardless of the $\overline{\text{MT\_CTS}}$ state. (For a list of local commands, see the *SmartMesh IA-510 Mote Serial API Guide*.)
$\overline{\text{TIME}}$	Input	The $\overline{\text{TIME}}$ pin can be used for triggering a timestamp packet. Its usage is optional.

8.3.2 Mode 3: Five-signal Serial Interface (115.2 kbps)

The LTP5900 mode 3 provides a five-signal serial interface with byte-level flow control on transfers from the mote to the microprocessor. The mode 3 serial interface is comprised of the data pins (TX, RX) as well as handshake pins ($\overline{\text{MT\_RTS}}$, $\overline{\text{MT\_CTS}}$, $\overline{\text{SP\_CTS}}$) used for bidirectional flow control. The $\overline{\text{MT\_RTS}}$ signal is ideal for designs where the microprocessor requires extra time to prepare to receive a packet (for example, the OEM microprocessor sleeps periodically, but requires a wake-up signal prior to receiving a packet. Refer to Table 14 for information on each handshake pin, including details on which pins are optional.

Table 14 Mode 3 Pin Usage

Pin	I/O	Usage
RX	Input	Serial data moving from the microprocessor to the mote.
TX	Output	Serial data moving from the mote to the microprocessor.
$\overline{\text{MT\_RTS}}$	Output	$\overline{\text{MT\_RTS}}$ provides a mechanism to wake up the microprocessor in order to receive a packet. This signal is asserted when the mote is ready to send a serial packet. The signal stays low until the $\overline{\text{SP\_CTS}}$ signal from the microprocessor is detected low by the mote (indicating readiness to receive a packet) or the tMT_RTS to SP_CTS timeout defined in Section 8.3.3 expires. If $\overline{\text{MT\_RTS}}$ times out, it will de-assert $\overline{\text{MT\_RTS}}$, wait for tMT_RTS retry and then re-assert $\overline{\text{MT\_RTS}}$ to attempt to send the serial packet again (see Figure 9).
$\overline{\text{SP\_CTS}}$	Input	$\overline{\text{SP\_CTS}}$ provides byte-level flow control for packets transferred from the mote to the microprocessor. When the microprocessor is capable of receiving a packet it should assert the $\overline{\text{SP\_CTS}}$ signal. In mode 3 byte-level flow control is achieved by having the microprocessor negate and then reassert the $\overline{\text{SP\_CTS}}$ signal following the receipt of each byte. The mote will begin transmission of the next byte after detecting the reassertion of

		$\overline{SP\_CTS}$.
$\overline{MT\_CTS}$	Output	$\overline{MT\_CTS}$ provides packet-level flow control for packets transferred from the microprocessor to the mote that are destined for transfer over the network. Upon reset, following boot the mote will negate $\overline{MT\_CTS}$ until the mote establishes a wireless network connection. During operation, the mote will negate $\overline{MT\_CTS}$ if the mote does not have sufficient buffering to accept another packet. $\overline{MT\_CTS}$ will also remain high if the mote is not part of the network. The microprocessor must check that the $\overline{MT\_CTS}$ pin is low before initiating each serial packet for wireless transmission. Note that the mote may receive local serial packets at any time regardless of the $\overline{MT\_CTS}$ state. For a list of local commands, see the SmartMesh IA-510 Mote Serial API Guide.
$\overline{TIME}$	Input	The $\overline{TIME}$ pin can be used for triggering a timestamp packet. Its usage is optional.

8.3.3 UART AC Timing

Table 15 UART Timing Values

Variable	Description	Min	Max	Units
tRX_BAUD	Deviation from baud rate	-2	+2	%
tRX_STOP	Number of stop bits (9600 bps)	1		bit period
tRX_STOP	Number of stop bits (115.2 kbps)	1.5		bit period
tTX_BAUD	Deviation from baud rate	-1	+1	%
tTX_STOP	Number of stop bits	1		bit period
tSP_CTS to MT_RTS	Assertion of $\overline{SP\_CTS}$ to negation of $\overline{MT\_RTS}$	0	10	ms
tMT_RTS to SP_CTS	Assertion of $\overline{MT\_RTS}$ to assertion of $\overline{SP\_CTS}$		500	ms
tMT_RTS retry	Time from a $\overline{MT\_RTS}$ timeout to the retry.		500	ms
tSP_CTS to TX	Assertion of $\overline{SP\_CTS}$ to start of byte	0	10	ms
tTX to SP_CTS	Start of byte to negation of $\overline{SP\_CTS}$	1		bit period
tSP_CTS ack PW	Negation pulse width of $\overline{SP\_CTS}$	500		ns
tdiag_ack_timeout*	The mote responds to all requests within this time.		125	ms
tinterbyte_timeout	Falling edge of TX to falling edge of $\overline{SP\_CTS}$ (Mode 3 only)		7.1	ms
tinterpacket_delay	The sender of an HDLC packet must wait at least this amount of time before sending another packet	20		ms
* For more information about supported requests and details on when tdiag_ack_timeout applies, refer to the *SmartMesh IA-510 Mote Serial API Guide*.				

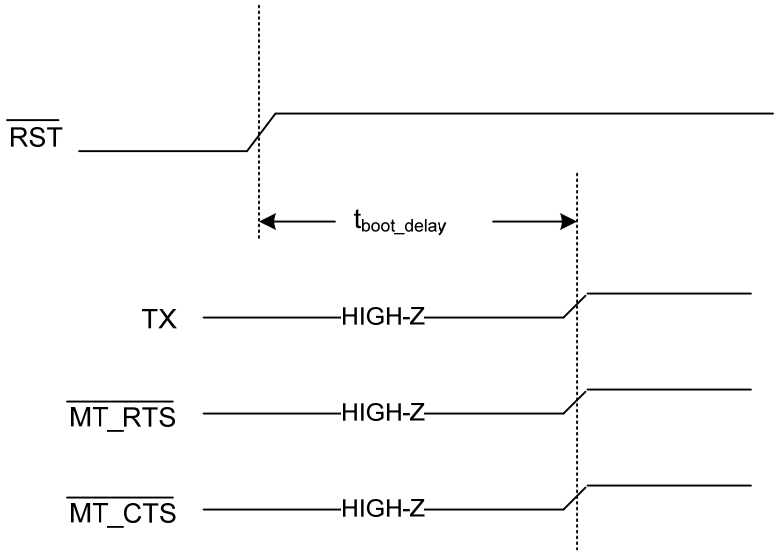

Figure 6 Power-on Sequence (see section 7.3 for value of t_{boot_delay})

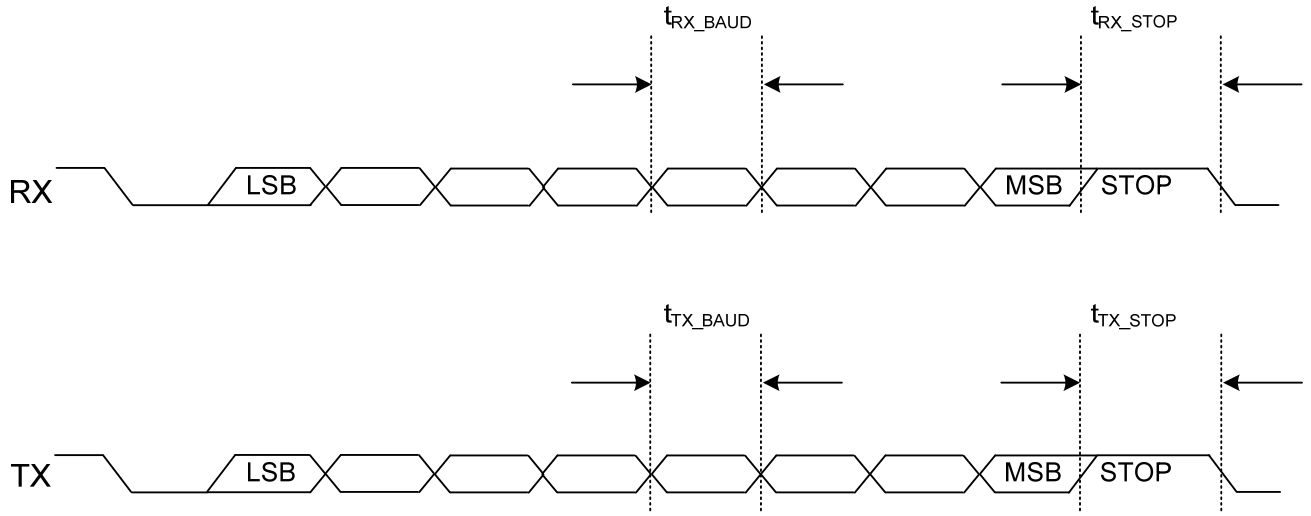

Figure 7 Byte-level Timing

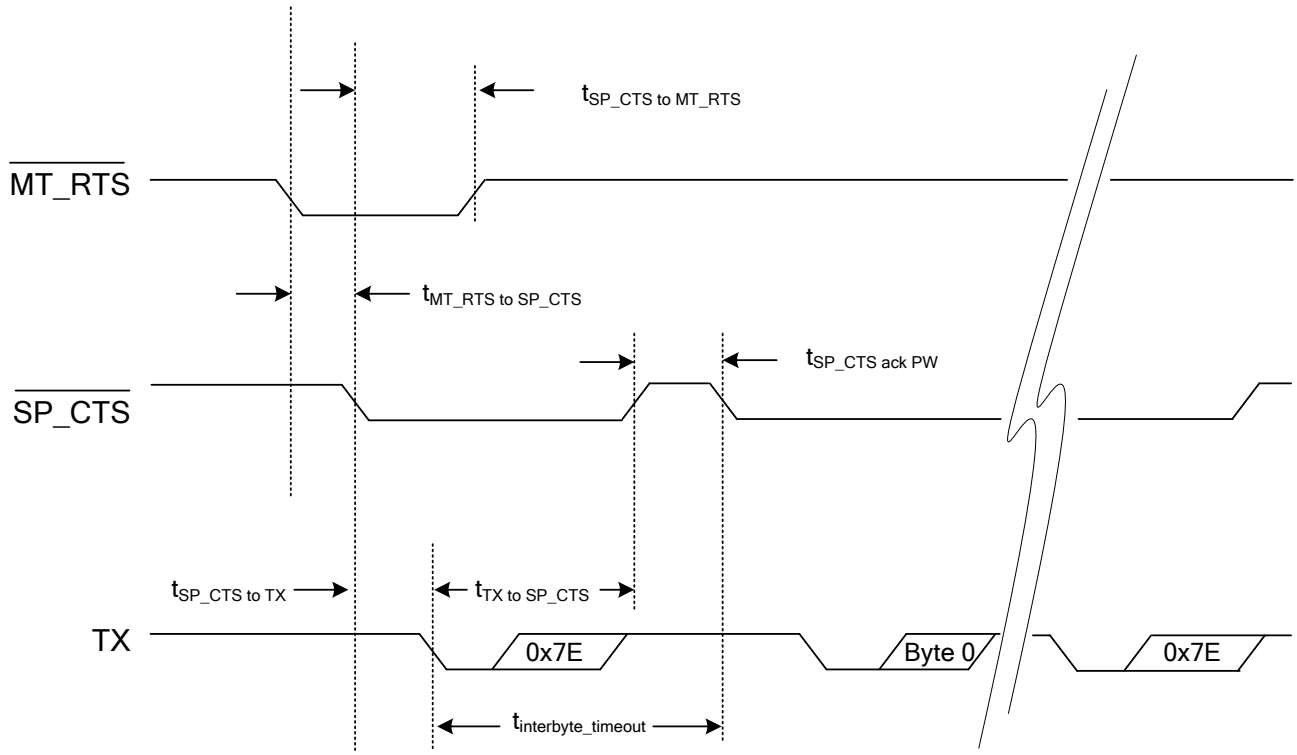

Figure 8 Flow Control Timing

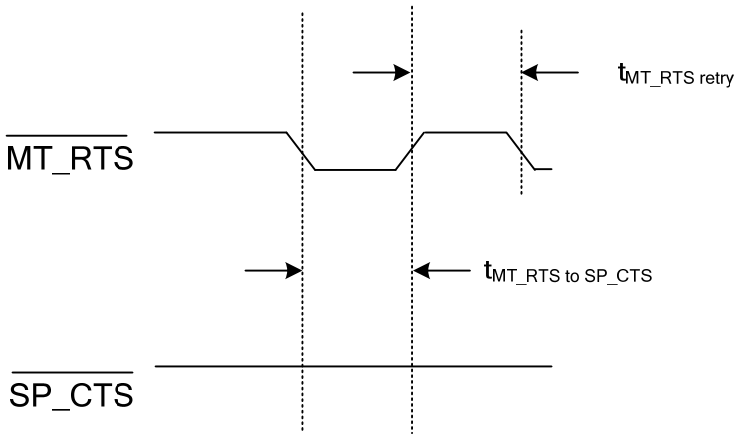

Figure 9 MT_RTS Timeout Behavior

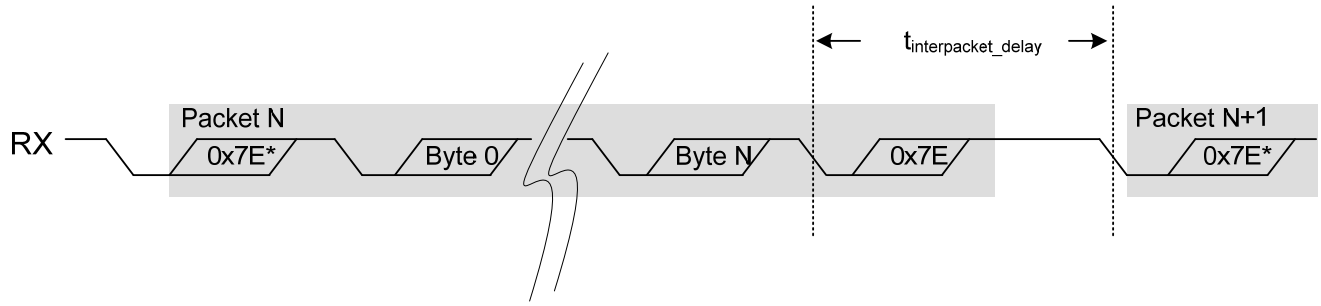

Figure 10 Packet Timing

* The framing byte, 0x7E, must NOT be repeated at the start of each packet sent to the LTP5900.

8.4 Mote Serial API

The LTP5900 offers a comprehensive application programming interface (API) that provides full programmatic access to control the mote, monitor its status (such as battery charge and network status), and provide access to the wireless mesh network. Refer to the *SmartMesh IA-510 Mote Serial API Guide* for more information.

8.5 Temperature Sensor

The LTP5900 has an on-board temperature sensor. The temperature readings are available locally through the mote serial API and through the network at the manager via the XML or serial API. For more information, refer to the *SmartMesh IA-510 Mote Serial API Guide*, *SmartMesh IA-510 Manager Serial API Guide*, or *SmartMesh IA-510 XML API Guide*.

Table 16 Temperature Sensor

Parameter	Min	Typ	Max	Units	Comments
Sensor input range	-40		85	°C	
Accuracy		±7		°C	

9.0 Packaging Description

9.1 Mechanical Drawing

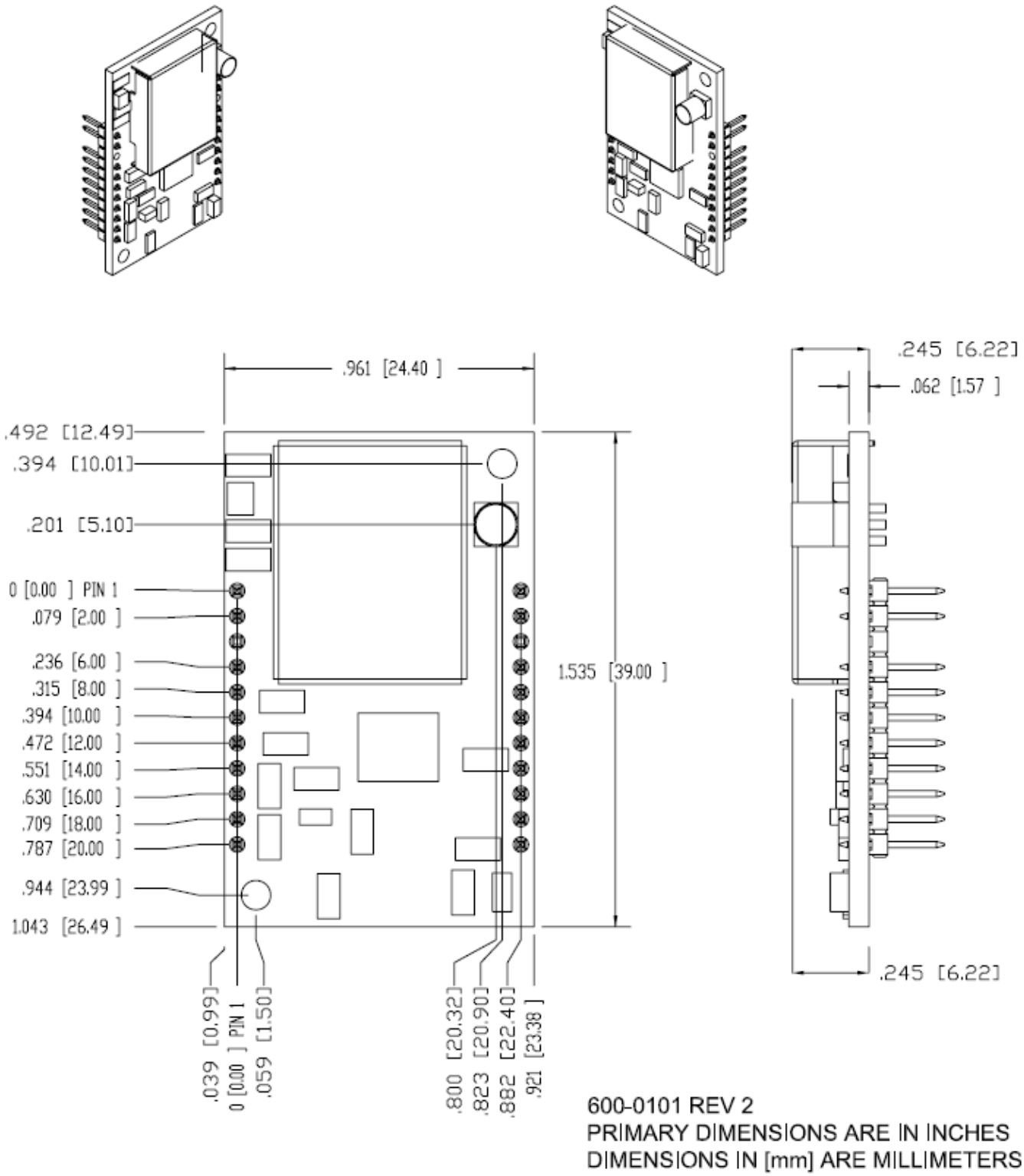

Figure 11 LTP5900 Mote Mechanical Drawing

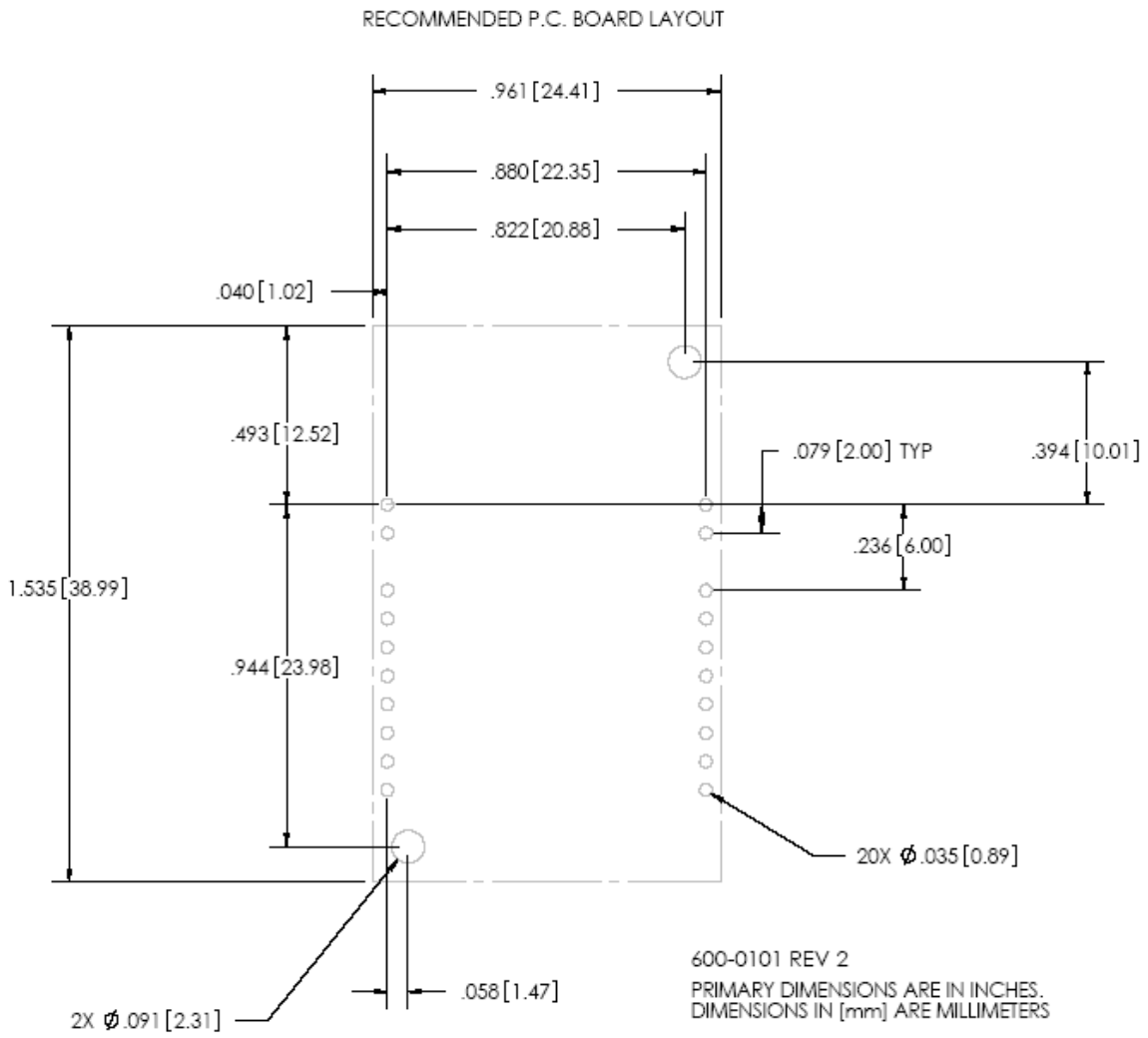

Figure 12 LTP5900 Mote Footprint

9.2 Soldering Information

The LTP5900 can be hand soldered with a soldering iron at 230 °C. The soldering iron should be in contact with the pin for 10 seconds or less.

10.0 Regulatory and Standards Compliance

10.1 FCC Compliance

10.1.1 FCC Testing

The LTP5900 mote complies with Part 15.247 modular (Intentional Radiator) of the FCC rules and regulations. In order to fulfill FCC certification requirements, products incorporating the LTP5900 mote must comply with the following:

1. An external label must be provided on the outside of the final product enclosure specifying the FCC identifier as described in 10.1.3 below.
2. The antenna must be electrically identical to the FCC-approved antenna specifications for the LTP5900 as described in 10.1.2, with the exception that the gain may be lower than specified in Table 17.
3. The device integrating the LTP5900 mote may not cause harmful interference and must accept any interference received, including interference that may cause undesired operation.
4. An unintentional radiator scan must be performed on the device integrating the LTP5900 mote, per FCC rules and regulations, CFR Title 47, Part 15, Subpart B. See FCC rules for specifics on requirements for declaration of conformity.

10.1.2 FCC-approved Antennae

The following are FCC-approved antenna specifications for the LTP5900.

Table 17 FCC-approved Antenna Specifications for the LTP5900

Gain	Type	Pattern	Polarization	Frequency	Connector
+2 dBi maximum	Dipole	Omni-directional	Vertical	2.4-2.4835 GHz	MMCX

10.1.3 OEM Labeling Requirements

The Original Equipment Manufacturer (OEM) must ensure that FCC labeling requirements are met. The outside of the final product enclosure must have a label with the following (or similar) text specifying the FCC identifier. The FCC ID and certification code must be in Latin letters and Arabic numbers and visible without magnification.

Contains transmitter module FCC ID: *SJC-LTP5900*

Or

Contains FCC ID: *SJC-LTP5900*

10.2 Industry Canada (IC) Compliance

10.2.1 IC Testing

The LTP5900 is certified for modular Industry Canada (IC) RSS-210 approval. The OEM is responsible for its product to comply with IC ICES-003 and FCC Part 15, Sub. B - Unintentional Radiators. The requirements of ICES-003 are equivalent to FCC Part 15 Sub. B and Industry Canada accepts FCC test reports or CISPR 22 test reports for compliance with ICES-003.

10.2.2 IC-approved Antennae

The LTP5900 is designed to operate with antennas meeting the specifications shown in Table 18. Antennas not meeting these specifications are strictly prohibited for use with the LTP5900. The required antenna impedance is 50 Ohms. Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Table 18 IC-approved Antenna Specifications for the LTP5900

Gain	Type	Pattern	Polarization	Frequency	Connector
+2 dBi maximum	Dipole	Omni-directional	Vertical	2.4-2.4835 GHz	MMCX

10.2.3 OEM Labeling Requirements

The Original Equipment Manufacturer (OEM) must ensure that IC labeling requirements are met. The outside of the final product enclosure must have a label with the following (or similar) text specifying the IC identifier. The IC ID and certification code must be in Latin letters and Arabic numbers and visible without magnification

Contains IC: *5853A-LTP5900*

10.3 CE Compliance

10.3.1 Declaration of Conformity

We, Dust Networks, of 30695 Huntwood Ave, Hayward, CA 94544 USA, declare under our sole responsibility that our product, SmartMesh IA-510 LTP5900, and in combination with our accessories, to which this declaration relates is in conformity with the appropriate standards ETSI EN 300 328, ETSI EN 301 489-17 and EN 60950, following the provisions of Radio Equipment and Telecommunication Terminal Equipment directive 99/5/EC with requirements covering EMC directive 89/336/EEC, and Low voltage directive 73/23/EEC.

10.3.2 European Compliance

If the LTP5900 mote is incorporated into a product, the manufacturer must ensure compliance of the final product to the European harmonized EMC and low-voltage/safety standards. A Declaration of Conformity must be issued for each of these standards and kept on file as described in Annex II of the R&TTE Directive. Furthermore, the manufacturer must maintain a copy of this LTP5900 user documentation and ensure the final product does not exceed the specified power ratings, antenna specifications, and/or installation requirements as specified in the user manual. If any of these specifications are exceeded in the final product, a submission must be made to a notified body for compliance testing to all required standards.

10.3.3 OEM Labeling Requirements

The 'CE' marking must be affixed to a visible location on the OEM product. The CE mark shall consist of the initials "CE" taking the following form:

If the CE marking is reduced or enlarged, the proportions given in the drawing below must be respected.

The CE marking must have a height of at least 5 mm except where this is not possible on account of the nature of the apparatus.

The CE marking must be affixed visibly, legibly, and indelibly.

Furthermore, since the usage of the 2400 – 2483.5 MHz band is not harmonized throughout Europe, the Restriction sign must be placed to the right of the 'CE' marking as shown below. See the R&TTE Directive, Article 12 and Annex VII for more information.

Figure 13 CE Label Requirements

10.3.4 Restrictions

Norway prohibits operation near Ny-Alesund in Svalbard. More information can be found at the Norway Posts and Telecommunications site (www.npt.no).

10.4 Compliance to Restriction of Hazardous Substances (RoHS)

Restriction of Hazardous Substances (RoHS) is a directive that places maximum concentration limits on the use of cadmium (Cd), lead (Pb), hexavalent chromium(Cr+6), mercury (Hg), Polybrominated Biphenyl(PBB) and Polybrominated Diphenyl Ethers (PBDE). Dust Networks is committed to meeting the requirements of the European Community directive 2002/95/EC.

This product has been specifically designed to utilize RoHS compliant materials and to eliminate, or reduce, the use of restricted materials to comply with 2002/95/EC.

The Dust Networks RoHS compliant design features include:

- RoHS compliant solder for solder joints
- RoHS compliant base metal alloys
- RoHS compliant precious metal plating
- RoHS compliant cable assemblies and connector choices

10.5 Industrial Environment Operation

The LTP5900 is designed to meet the specifications of a harsh industrial environments which includes:

- **Shock and Vibration**—The LTP5900 complies with high vibration pipeline testing, as specified in IEC 60770-1.
- **Temperature Extremes**—The LTP5900 is designed for industrial storage and operational temperature range of –40 °C to +85 °C.

10.6 Encryption Cipher

The LTP5900's 128-bit Advanced Encryption Standard (AES) cipher has been certified compliant to the United States National Institute of Standards and Technology (NIST) FIPS-197 (NIST certificate number, AES: 1437). To view the FIPS-197 validation list, go to: http://csrc.nist.gov/groups/STM/cavp/documents/aes/aesval.html

11.0 Related Documentation

- *SmartMesh LTP5900 Integration Guide*
- *SmartMesh WirelessHART Mote CLI Guide*
- *SmartMesh WirelessHART Mote API Guide*

12.0 Order Information

LEAD FREE FINISH	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE**
LTP5900IPC-WHMA???#PBF	LTP5900	22-Lead (39mm x 24.4mm) PCB	-40 °C to 85 °C

** See http://www.linear.com/ or contact your sales representative to determine the three digit software version field, ???.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/

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