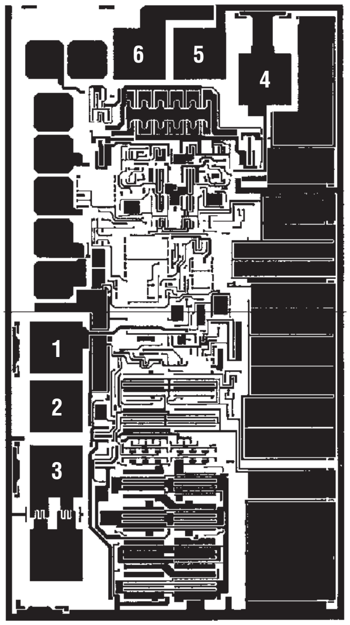
RH6200M
Low Noise, High Speed Rail-to-Rail Op Amp



57mils × 33mils,
12mils thick.
Backside metal: Gold
Backside potential: V^-

PAD FUNCTION

1. $\overline{SHDN}$
2. –IN
3. +IN
4. OUT
5. V^-
6. V^+

DIE CROSS REFERENCE

LTC Finished Part Number	Order DICE Part Number
RH6200MW	RH6200M DICE

DICE/DWF ELECTRICAL TEST LIMITS $T_A = 25°C$

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNITS
V_{OS}	Input Offset Voltage	V_S = 5V, 0V; V_{CM} = V^- to V^+		2	mV
		V_S = ±5V; V_{CM} = V^- to V^+		6	mV
I_B	Input Bias Current	V_S = 5V, 0V; V_{CM} = V^+		18	µA
		V_S = 5V, 0V; V_{CM} = V^-	–50		µA
		V_S = ±5V; V_{CM} = V^+		18	µA
		V_S = ±5V; V_{CM} = V^-	–50		µA
I_{OS}	Input Offset Current	V_S = 5V, 0V; V_{CM} = V^+		4	µA
		V_S = 5V, 0V; V_{CM} = V^-		5	µA
		V_S = ±5V; V_{CM} = V^+		7	µA
		V_S = ±5V; V_{CM} = V^-		12	µA
A_{VOL}	Large Signal	V_S = 5V, 0V; R_L = 1k; V_{OUT} = 0.5V to 4.5V	70		V/mV
	Open-Loop	V_S = 5V, 0V; R_L = 100Ω; V_{OUT} = 1V to 4V	11		V/mV
	Voltage Gain	V_S = ±5V; R_L = 1k; V_{OUT} = ±4.5V	115		V/mV
		V_S = ±5V; R_L = 100Ω; V_{OUT} = ±2V	15		V/mV
CMRR	Common Mode Rejection Ratio	V_S = 5V, 0V; V_{CM} = 0V to 5V	65		dB
		V_S = 5V, 0V; V_{CM} = 1.5V to 3.5V	85		dB
		V_S = ±5V; V_{CM} = ±5V	68		dB
		V_S = ±5V; V_{CM} = ±2V	75		dB

DICE/DWF ELECTRICAL TEST LIMITS $T_A = 25°C$

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNITS
PSRR	Power Supply Rejection Ratio	V_S = ±2.25V to ±5V	60		dB
V_{OL}	Output Voltage Swing Low	V_S = 5V, 0V; I_L = 0 V_S = 5V, 0V; I_L = 5mA V_S = 5V, 0V; I_L = 20mA V_S = ±5V; I_L = 0 V_S = ±5V; I_L = 5mA V_S = ±5V; I_L = 20mA		50 100 290 50 110 290	mV mV mV mV mV mV
V_{OH}	Output Voltage Swing High	V_S = 5V, 0V; I_L = 0 V_S = 5V, 0V; I_L = 5mA V_S = 5V, 0V; I_L = 20mA V_S = ±5V; I_L = 0 V_S = ±5V; I_L = 5mA V_S = ±5V; I_L = 20mA		110 190 400 130 210 420	mV mV mV mV mV mV
I_{SC}	Short-Circuit Current	V_S = 5V, 0V or V_S = ±5V	±60		mA
I_S	Supply Current	V_S = 5V, 0V V_S = ±5V		20 23	mA mA
$I_{S(SHDN)}$	Shutdown Supply Current	V_S = 5V, 0V V_S = ±5V		1.8 2.1	mA mA
I_{SHDN}	Shutdown Pin Current	V_S = 5V, 0V or V_S = ±5V; V_{SHDN} = 0.3V	–280		µA
GBW	Gain Bandwidth Product	V_S = ±5V; at f = 1MHz	110		MHz

Rad Hard die require special handling as compared to standard IC chips.

Rad Hard die are susceptible to surface damage because there is no silicon nitride passivation as on standard die. Silicon nitride protects the die surface from scratches by its hard and dense properties. The passivation on Rad Hard die is silicon dioxide that is much “softer” than silicon nitride.

LTC recommends that die handling be performed with extreme care so as to protect the die surface from scratches. If the need arises to move the die around from the chip tray, use a Teflon-tipped vacuum wand. This wand can be made by pushing a small diameter Teflon tubing onto the tip of a steel-tipped wand. The inside diameter of the Teflon tip should match the die size for efficient pickup. The tip of the Teflon should be cut square and flat to ensure good vacuum to die surface. Ensure the Teflon tip remains clean from debris by inspecting under stereoscope.

During die attach, care must be exercised to ensure no tweezers touch the top of the die.

Wafer level testing is performed per the indicated specifications for dice. Considerable differences in performance can often be observed for dice versus packaged units due to the influences of packaging and assembly on certain devices and/or parameters. Please consult factory for more information on dice performance and lot qualifications via lot sampling test procedures.

Dice data sheet subject to change. Please consult factory for current revision in production.

I.D.No. 66-13-6200M

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