14-Bit DC Accurate Clock-Tunable, 8th Order Elliptic or Linear Phase Lowpass Filter

FEATURES

- **DC Gain Linearity: 14 Bits**
- **Maximum DC Offset: ±1.5mV**
- **DC Offset TempCo: 7μV/°C**
- Device Fully Tested at f_{CUTOFF} = 80kHz
- Maximum Cutoff Frequency: 120kHz (V_S = ±8V)
- Drives 1kΩ Load with 0.02% THD or Better
- Signal-to-Noise Ratio: 90dB
- Input Impedance: 500MΩ
- Selectable Elliptic or Linear Phase Response
- Operates from Single 5V up to ±8V Power Supplies
- Available in an 18-Pin SO Wide Package

APPLICATIONS

- Instrumentation
- Data Acquisition Systems
- Anti-Aliasing Filters
- Smoothing Filters
- Audio Signal Processing

DESCRIPTION

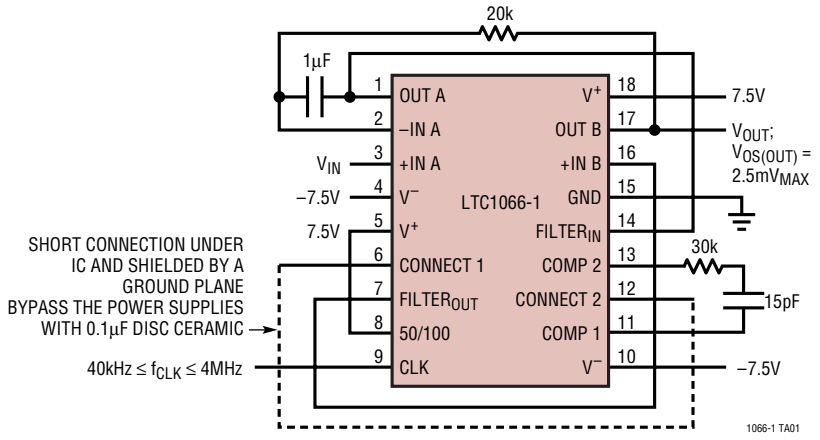
The LTC®1066-1 is an 8th order elliptic lowpass filter which simultaneously provides clock-tunability and DC accuracy. The unique and proprietary architecture of the filter allows 14 bits of DC gain linearity and a maximum of 1.5mV DC offset. An external RC is required for DC accurate operation. With ±7.5V supplies, a 20k resistor and a 1μF capacitor, the cutoff frequency can be tuned from 800Hz to 100kHz. A clock-tunable 10Hz to 100kHz operation can also be achieved (see Typical Application section).

The filter does not require any external active components such as input/output buffers. The input/output impedance is 500MΩ/0.1Ω and the output of the filter can source or sink 40mA. When pin 8 is connected to V^+, the clock-to-cutoff frequency ratio is 50:1 and the input signal is sampled twice per clock cycle to lower the risk of aliasing. For frequencies up to $0.75f_{CUTOFF}$, the passband ripple is ±0.15dB. The gain at f_{CUTOFF} is –1dB and the filter's stopband attenuation is 80dB at $2.3f_{CUTOFF}$. Linear phase operation is also available with a clock-to-cutoff frequency ratio of 100:1 when pin 8 is connected to ground.

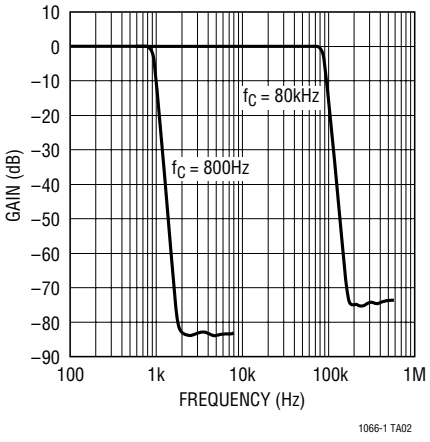
The LTC1066-1 is available in an 18-pin SO Wide package.

TYPICAL APPLICATION

Clock-Tunable, DC Accurate, 800Hz to 80kHz Elliptic Lowpass Filter



Amplitude Response



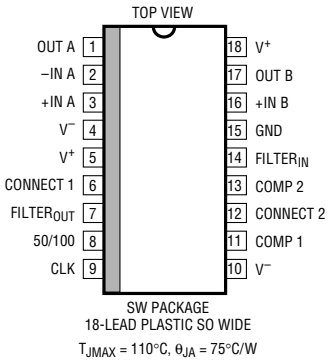
ABSOLUTE MAXIMUM RATINGS

(Note 1)

Total Supply Voltage (V^+ to V^-) 16.5V
Power Dissipation 700mW
Burn-In Voltage 16.5V
Voltage at Any Input ..... $(V^- - 0.3V) \leq V_{IN} \leq (V^+ + 0.3V)$
Maximum Clock Frequency
$V_S = \pm 8V$ 6.1MHz
$V_S = \pm 7.5V$ 5.4MHz
$V_S = \pm 5V$ 4.1MHz
V_S = Single 5V 1.8MHz
Operating Temperature Range* ..... 0°C to 70°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

* For an extended operating temperature range contact LTC Marketing for details.

PACKAGE/ORDER INFORMATION



SW PACKAGE
18-LEAD PLASTIC SO WIDE
T_{JMAX} = 110°C, θ_{JA} = 75°C/W

ORDER PART NUMBER
LTC1066-1CSW

Order Options Tape and Reel: Add #TR
Lead Free: Add #PBF Lead Free Tape and Reel: Add #TRPBF
Lead Free Part Marking: http://www.linear.com/leadfree/

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

(See Test Circuit)

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $V_S = \pm 7.5V$, $R_L = 1k$, $T_A = 25°C$, f_{CLK} signal level is TTL or CMOS (maximum clock rise or fall time ≤ 1μs) unless otherwise specified. All AC gain measurements are referenced to passband gain.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Passband Gain ($0.01f_{CUTOFF}$ to $0.25f_{CUTOFF}$)	f_{CLK} = 400kHz, f_{TEST} = 2kHz	●	–0.18	0.16	0.36	dB
Passband Ripple ($0.01f_{CUTOFF}$ to $0.75f_{CUTOFF}$) for f_{CLK}/f_{CUTOFF} = 50:1	$f_{CUTOFF} \leq$ 50kHz (See Note on Test Circuit)			±0.15		dB
Gain at $0.50f_{CUTOFF}$ for f_{CLK}/f_{CUTOFF} = 50:1	f_{CLK} = 400kHz, f_{TEST} = 4kHz	 ●	–0.09 –0.14	0.02 0.05	0.09 0.14	dB dB
	f_{CLK} = 2MHz, f_{TEST} = 20kHz	 ●	–0.16 –0.22	–0.05 –0.10	0.02 0.02	dB dB
Gain at $0.75f_{CUTOFF}$ for f_{CLK}/f_{CUTOFF} = 50:1	f_{CLK} = 400kHz, f_{TEST} = 6kHz	 ●	–0.18 –0.22	–0.05 –0.10	0.05 0.05	dB dB
	f_{CLK} = 2MHz, f_{TEST} = 30kHz	 ●	–0.36 –0.45	–0.20 –0.30	0.05 0.05	dB dB
	f_{CLK} = 4MHz, f_{TEST} = 60kHz	 ●	–0.65 –0.85	–0.30 –0.40	0.25 0.75	dB dB
Gain at $1.00f_{CUTOFF}$ for f_{CLK}/f_{CUTOFF} = 50:1	f_{CLK} = 400kHz, f_{TEST} = 8kHz	 ●	–1.50 –1.80	–1.10 –1.20	–0.05 –0.05	dB dB
	f_{CLK} = 2MHz, f_{TEST} = 40kHz	 ●	–2.10 –2.30	–1.60 –1.60	–1.20 –1.20	dB dB
	f_{CLK} = 4MHz, f_{TEST} = 80kHz	 ●	–2.20 –2.50	–1.60 –1.60	–0.05 0.25	dB dB
Gain at $2.00f_{CUTOFF}$ for f_{CLK}/f_{CUTOFF} = 50:1	f_{CLK} = 400kHz, f_{TEST} = 16kHz	 ●	–56 –54	–58 –57	–64 –64	dB dB
	f_{CLK} = 2MHz, f_{TEST} = 80kHz	 ●	–53 –51	–56 –55	–62 –62	dB dB
	f_{CLK} = 4MHz, f_{TEST} = 160kHz	 ●	–50 –48	–52 –51	–60 –60	dB dB

ELECTRICAL CHARACTERISTICS (See Test Circuit)

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at V_S = ±7.5V, R_L = 1k, T_A = 25°C, f_{CLK} signal level is TTL or CMOS (maximum clock rise or fall time ≤ 1μs) unless otherwise specified. All AC gain measurements are referenced to passband gain.

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
Gain at f_{CUTOFF} for f_{CLK} = 20kHz, V_S = ±7.5V		f_{CLK}/f_{CUTOFF} = 50:1, f_{TEST} = 400Hz	●	–1.75	–1.25	–0.50	dB
Gain at f_{CUTOFF} for V_S = ±2.375V, f_{CLK}/f_{CUTOFF} = 50:1		f_{CLK} = 1MHz, f_{TEST} = 20kHz	●	–1.75	–0.70	0.10	dB
Gain at 70kHz for V_S = ±5V, f_{CLK}/f_{CUTOFF} = 50:1		f_{CLK} = 4MHz, f_{TEST} = 70kHz	●		1.00	1.40	dB
Linear Phase Response f_{CLK}/f_{CUTOFF} = 100:1, Pin 8 at GND	Phase at 0.25f_{CUTOFF}	f_{CLK} = 400kHz, f_{TEST} = 1kHz	 ●	–48.5 –48.0	–50.0 –50.0	–51.5 –52.0	Deg Deg
	Gain at 0.25f_{CUTOFF}	f_{CLK} = 400kHz, f_{TEST} = 1kHz	●	–0.65	–0.25	0.25	dB
	Phase at 0.50f_{CUTOFF}	f_{CLK} = 400kHz, f_{TEST} = 2kHz	 ●	–97.5 –97.0	–99.5 –99.5	–101.5 –102.0	Deg Deg
	Gain at 0.50f_{CUTOFF}	f_{CLK} = 400kHz, f_{TEST} = 2kHz	●	–0.75	–0.50	–0.10	dB
	Phase at 0.75f_{CUTOFF}	f_{CLK} = 400kHz, f_{TEST} = 3kHz	 ●	–148.0 –147.5	–150.5 –150.5	–152.5 –153.0	Deg Deg
	Gain at 0.75f_{CUTOFF}	f_{CLK} = 400kHz, f_{TEST} = 3kHz	●	–1.40	–1.00	–0.60	dB
	Phase at f_{CUTOFF}	f_{CLK} = 400kHz, f_{TEST} = 4kHz	 ●	–208.0 –207.5	–210.0 –210.0	–212.5 –213.0	Deg Deg
	Gain at f_{CUTOFF}	f_{CLK} = 400kHz, f_{TEST} = 4kHz	●	–2.10	–1.80	–1.60	dB
Input Bias Current		V_S = ±2.375V	 ●		60 70	 135	nA nA
Input Offset Current		V_S = ±2.375V V_S ≥ ±5V (Note 3)	● ●		±10 ±10	±40 ±45	nA nA
Input Offset Current TempCo		±2.375V ≤ V_S ≤ ±7.5V			40		pA/°C
Output Voltage Offset TempCo		±2.375V ≤ V_S ≤ ±7.5V			7		μV/°C
Output Offset Voltage		V_S = ±2.375V, f_{CLK} = 400kHz	 ●		±0.5 ±1.0	 ±1.5	mV mV
		V_S ≥ ±5V (Note 3)	 ●		±0.5 ±1.0	 ±1.5	mV mV
Common Mode Rejection		V_S = ±7.5V V_{CM} = –5V to 5V	 ●	90 84	96 90		dB dB
Power Supply Rejection		V_S = ±2.5V to ±7.5V	 ●	80 78	84 82		dB dB
Input Voltage Range and Output Voltage Swing		V_S = ±2.375V, R_L = 1k	 ●	±1.2 ±1.1	±1.4		V V
		V_S = ±5V, R_L = 1k	 ●	±3.4 ±3.2	±3.6		V V
		V_S = ±7.5V, R_L = 1k	 ●	±5.4 ±5.0	±5.8		V V
Output Short-Circuit Current		±2.375V ≤ V_S ≤ ±7.5V		±20			mA
Power Supply Current (Note 2)		V_S = ±2.375V	 ●		14 16	16 19	mA mA
		V_S = ±5V	 ●		22 23	26 29	mA mA
		V_S = ±7.5V	 ●		25 26	30 33	mA mA
Power Supply Range				±2.375		±8	V

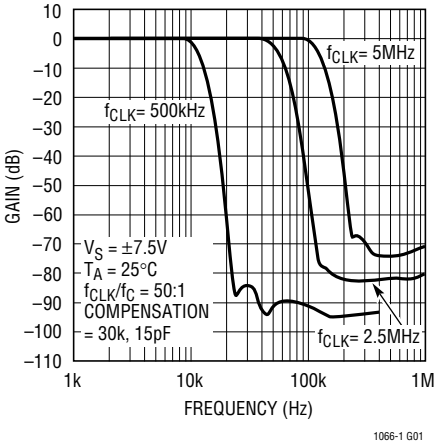
Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: The maximum current over temperature is at 0°C. At 70°C the maximum current is less than its maximum value at 25°C.

Note 3: Guaranteed by design and test correlation.

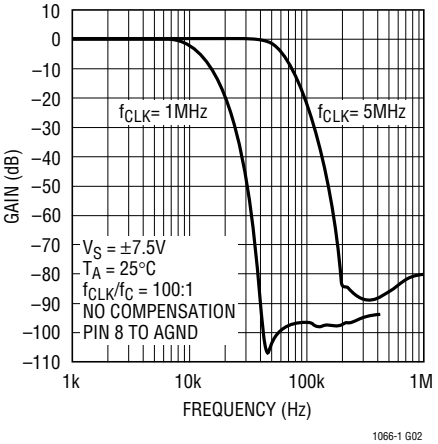
TYPICAL PERFORMANCE CHARACTERISTICS

Gain vs Frequency
$V_S = \pm 7.5V$, $f_{CLK}/f_C = 50:1$



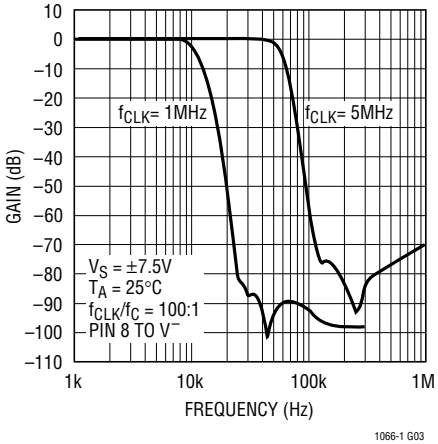
1066-1 G01

Gain vs Frequency
$V_S = \pm 7.5V$, $f_{CLK}/f_C = 100:1$



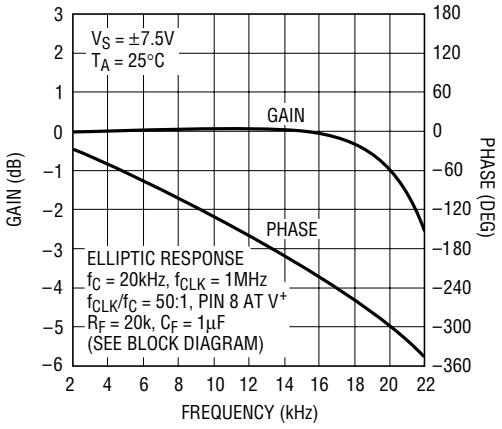
1066-1 G02

Gain vs Frequency
$V_S = \pm 7.5V$, $f_{CLK}/f_C = 100:1$



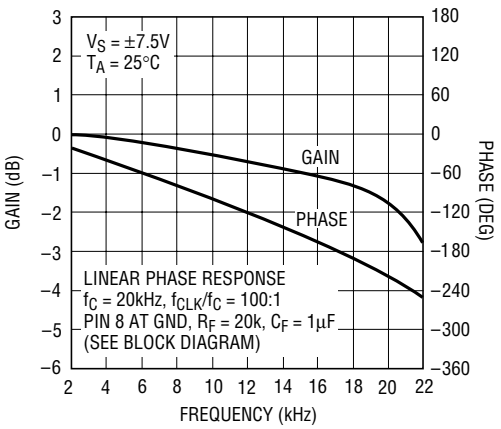
1066-1 G03

Passband Gain and Phase vs Frequency



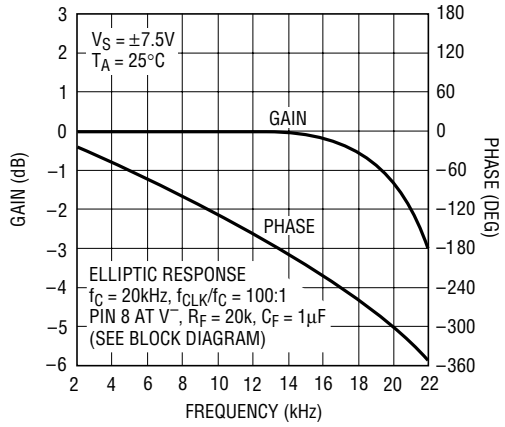
10666-1 G04

Passband Gain and Phase vs Frequency



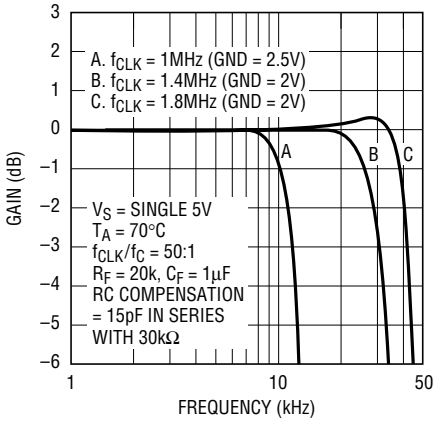
10666-1 G05

Passband Gain and Phase vs Frequency



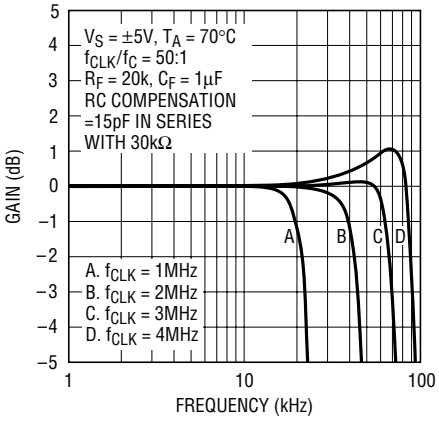
10666-1 G06

Passband Gain vs Frequency and f_{CLK}



1066-1 G07

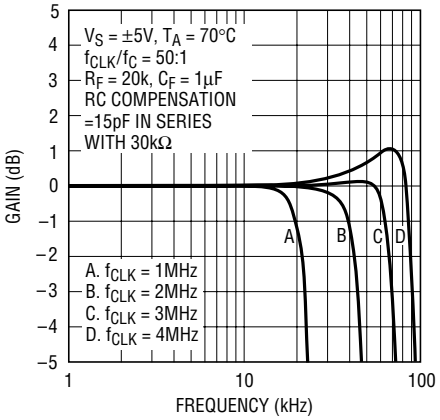
Passband Gain vs Frequency and f_{CLK}



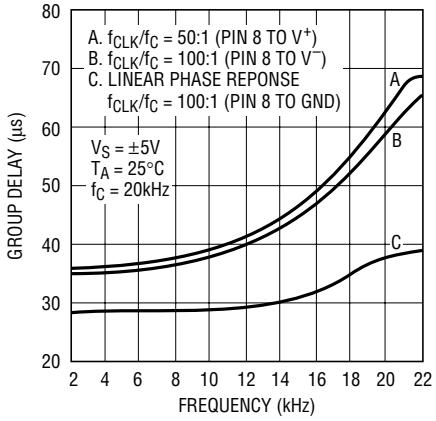
1066-1 G08

TYPICAL PERFORMANCE CHARACTERISTICS

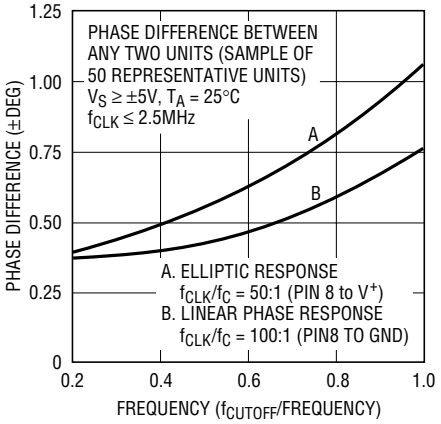
Passband Gain vs Frequency



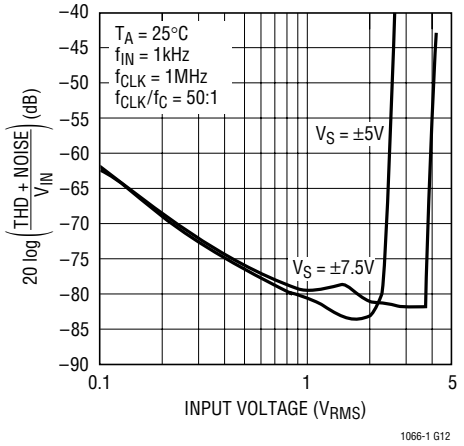
Group Delay vs Frequency



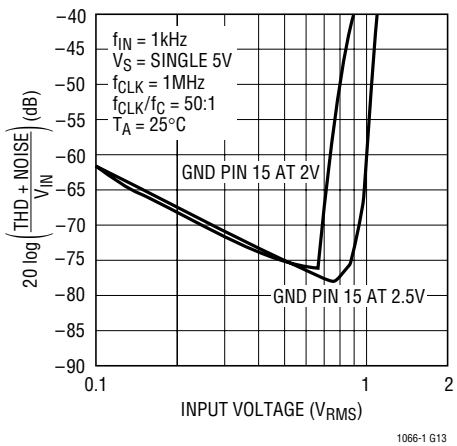
Phase Matching vs Frequency



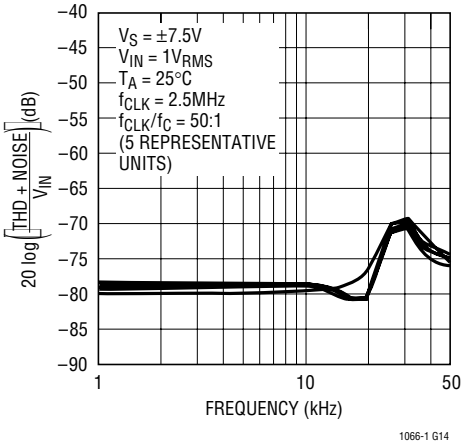
THD + Noise vs Input Voltage



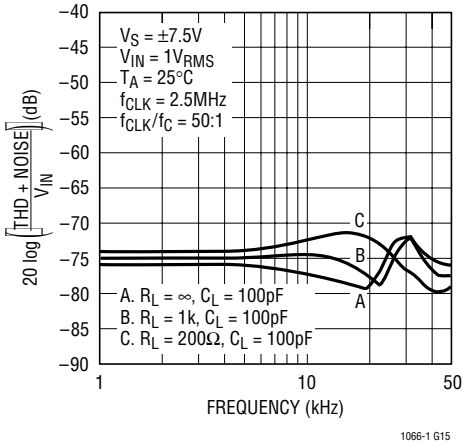
THD + Noise vs Input Voltage



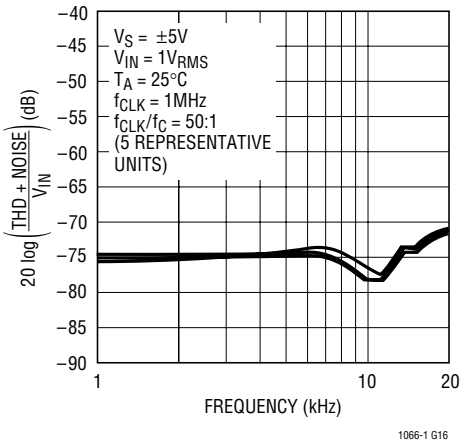
THD + Noise vs Frequency



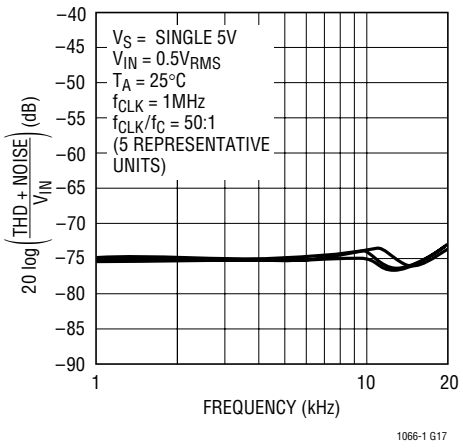
THD + Noise vs Frequency



THD + Noise vs Frequency

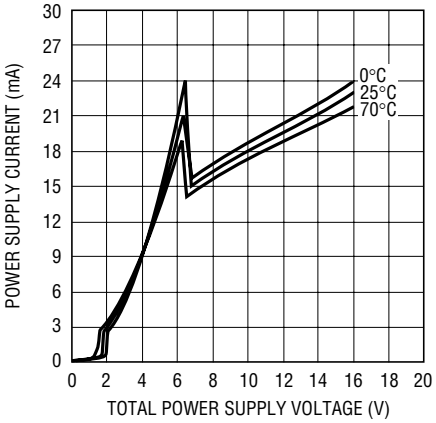


THD + Noise vs Frequency



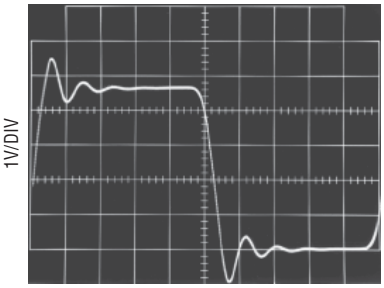
TYPICAL PERFORMANCE CHARACTERISTICS

Power Supply Current vs Power Supply Voltage



1066-1 G18

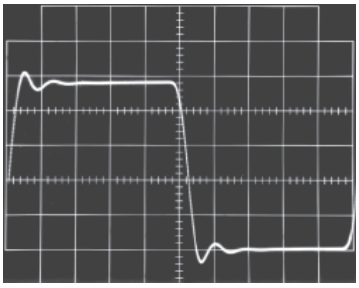
Transient Response



ELLIPTIC RESPONSE (PIN 8 TO V^+)
f_{IN} = 1kHz, f_{CUTOFF} = 10kHz

1066-1 G19

Transient Response



LINEAR PHASE (PIN 8 TO GND)
f_{IN} = 1kHz, f_{CUTOFF} = 10kHz

1066-1 G20

Table 1. Elliptic Response, f_C = 10kHz, f_{CLK}/f_{CUTOFF} = 50:1, V_S = ±7.5V, R_F = 20k, C_F = 1µF, No RC Compensation, T_A = 25°C

FREQUENCY (kHz)	GAIN (dB)	PHASE (DEG)	GROUP DELAY (µs)
2.000	0.117	–50.09	70.52
3.000	0.118	–75.75	72.04
4.000	0.116	–101.96	74.32
5.000	0.112	–129.25	77.59
6.000	0.104	–157.82	82.04
7.000	0.074	171.68	88.56
8.000	–0.014	138.41	97.80
9.000	–0.278	101.26	110.33
10.000	–0.986	58.98	124.91

Table 2. Elliptic Response, f_C = 50kHz, f_{CLK}/f_{CUTOFF} = 50:1, V_S = ±7.5V, R_F = 20k, C_F = 1µF, No RC Compensation, T_A = 25°C

FREQUENCY (kHz)	GAIN (dB)	PHASE (DEG)	GROUP DELAY (µs)
10.000	0.104	–50.91	14.32
15.000	0.105	–76.95	14.61
20.000	0.107	–103.51	15.05
25.000	0.109	–131.13	15.70
30.000	0.107	–160.03	16.57
35.000	0.089	169.22	17.85
40.000	0.014	135.72	19.66
45.000	–0.231	98.44	22.10
50.000	–0.905	56.15	24.93

Table 3. Linear Phase Response, f_C = 10kHz, f_{CLK}/f_{CUTOFF} = 100:1, V_S = ±7.5V, R_F = 20k, C_F = 1µF, No RC Compensation, T_A = 25°C

FREQUENCY (kHz)	GAIN (dB)	PHASE (DEG)	GROUP DELAY (µs)
2.000	–0.020	–39.96	55.25
3.000	–0.181	–59.76	55.03
4.000	–0.383	–79.60	54.98
5.000	–0.601	–99.34	55.28
6.000	–0.811	–119.40	56.34
7.000	–1.004	–139.91	58.56
8.000	–1.196	–161.56	62.34
9.000	–1.451	175.21	67.29
10.000	–1.910	149.99	72.31

Table 4. Linear Phase Response, f_C = 50kHz, f_{CLK}/f_{CUTOFF} = 100:1, V_S = ±7.5V, R_F = 20k, C_F = 1µF, No RC Compensation, T_A = 25°C

FREQUENCY (kHz)	GAIN (dB)	PHASE (DEG)	GROUP DELAY (µs)
10.000	0.039	–40.72	11.30
15.000	–0.068	–61.01	11.31
20.000	–0.202	–81.42	11.36
25.000	–0.345	–101.88	11.48
30.000	–0.479	–122.74	11.73
35.000	–0.594	–144.09	12.20
40.000	–0.701	–166.68	12.99
45.000	–0.860	169.15	14.06
50.000	–1.214	142.72	15.19

PIN FUNCTIONS

Power Supply Pins (5, 18, 4, 10)

The power supply pins should be bypassed with a 0.1µF capacitor to an adequate analog ground. The bypass capacitors should be connected as close as possible to the power supply pins. The V^+ pins (5, 18) and the V^- pins (4, 10) should always be tied to the same positive supply and negative supply value respectively. Low noise linear supplies are recommended. Switching power supplies are not recommended as they will lower the filter dynamic range.

When the LTC1066-1 is powered up with dual supplies and, if V^+ is applied prior to a floating V^-, connect a signal diode (1N4148) between pin 10 and ground to prevent power supply reversal and latch-up. A signal diode (1N4148) is also recommended between pin 5 and ground if the negative supply is applied prior to the positive supply and the positive supply is floating. Note, in most laboratory supplies, reversed biased diodes are always connected between the supply output terminals and ground, and the above precautions are not necessary. However, when the filter is powered up with conventional 3-terminal regulators, the diodes are recommended.

Analog Ground Pin (15)

The filter performance depends on the quality of the analog signal ground. For either dual or single supply operation, an analog ground plane surrounding the package is recommended. The analog ground plane should be connected to any digital ground at a single point. For dual supply operation, pin 15 should be connected to the analog ground plane. For single supply operation pin 15 should be biased at 1/2 supply and should be bypassed to the analog ground plane with at least a 1µF capacitor (see Typical Applications). For single 5V operation and for $f_{CLK} \geq 1.4$MHz, pin 15 should be biased at 2V. This minimizes passband gain and phase variations.

Clock Input Pin (9)

Any TTL or CMOS clock source with a square-wave output and 50% duty cycle (±10%) is an adequate clock source for the device. The power supply for the clock source should not be the filter's power supply. The analog ground for the filter should be connected to clock's ground at a single point only. Table 5 shows the clock's low and high level threshold values for a dual or single supply operation. Sine waves are not recommended for clock input frequencies less than 100kHz, since excessively slow clock rise or fall times generate internal clock jitter (maximum clock rise or fall time ≤ 1µs). The clock signal should be routed from the left side of the IC package and perpendicular to it to avoid coupling to any input or output analog signal path. A 200Ω resistor between clock source and pin 9 will slow down the rise and fall times of the clock to further reduce charge coupling.

Table 5. Clock Source High and Low Threshold Levels

POWER SUPPLY	HIGH LEVEL	LOW LEVEL
Dual Supply = ±7.5V	≥ 2.18V	≤ 0.5V
Dual Supply = ±5V	≥ 1.45V	≤ 0.5V
Dual Supply = ±2.5V	≥ 0.73V	≤ –2.0V
Single Supply = 12V	≥ 7.80V	≤ 6.5V
Single Supply = 5V	≥ 1.45V	≤ 0.5V

50:1/100:1 Pin (8)

The DC level at pin 8 determines the ratio of the clock to the filter cutoff frequency. When pin 8 is connected to V^+ the clock-to-cutoff frequency ratio (f_{CLK}/f_{CUTOFF}) is 50:1 and the filter response is elliptic. The design of the internal switched-capacitor filter was optimized for a 50:1 operation.

When pin 8 is connected to ground (or 1/2 supply for single supply operation), the f_{CLK}/f_{CUTOFF} ratio is equal to 100:1 and the filter response is pseudolinear phase (see Group Delay vs Frequency in Typical Performance Characteristic section).

When pin 8 is connected to V^- (or ground for single supply operation), the f_{CLK}/f_{CUTOFF} ratio is 100:1 and the filter response is transitional Butterworth elliptic. The Typical Performance Characteristics provide all the necessary information.

If the DC level at pin 8 is mechanically switched, a 10k resistor should be connected between pin 8 and the DC source.

Input Pins (2, 3, 14, 16)

Pin 3 (+IN A) and pin 2 (–IN A) are the positive and negative inputs of an internal high performance op amp A

PIN FUNCTIONS

(see Block Diagram). Input bias current flows out of pins 2 and 3. Pin 16 (+IN B) is the positive input of a high performance op amp B which is internally connected as a unity-gain follower. Op amp B buffers the switched-capacitor network output. The input capacitance of both op amps is 10pF.

Pin 14 ($FILTER_{IN}$) is the input of a switched-capacitor network. The input impedance of pin 14 is typically 11k.

Output Pins (1, 7, 17)

Pins 1 and 17 are the outputs of the internal high performance op amps A and B. Pin 1 is usually connected to the internal switched-capacitor filter network input pin 14. Pin 17 is the buffered output of the filter and it can drive loads as heavy as 200Ω (see THD + Noise curves under Typical Performance Characteristics). Pin 7 is the internal switched-capacitor network output and it can typically sink or source 1mA.

Compensation Pins (11, 13)

Pins 11 and 13 are the AC compensation pins. If compensation is needed, an external 30k resistor in series with a 15pF capacitor should be connected between pins 11 and 13. Compensation is recommended for the following cases shown in Table 6.

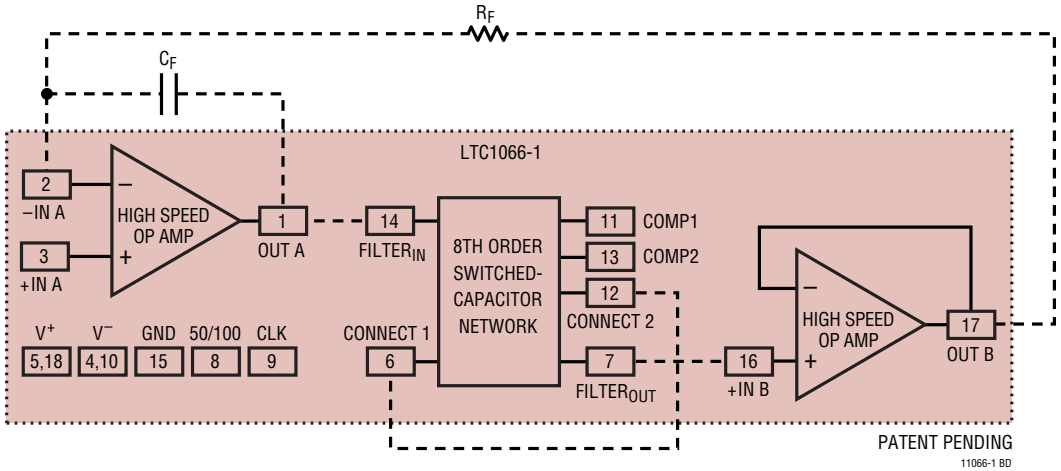
Table 6. Cases Where an RC Compensation (15pF in Series with 30kΩ pins 11, 13) is Recommended, f_{CLK}/f_{CUTOFF} = 50:1

V_S = Single 5V (AGND = 2V)	T_A = 25°C T_A = 70°C	$f_{CUTOFF} \geq$ 28kHz $f_{CUTOFF} \geq$ 24kHz
V_S = ±5V	T_A = 25°C T_A = 70°C	$f_{CUTOFF} \geq$ 60kHz $f_{CUTOFF} \geq$ 50kHz
V_S = ±7.5V	T_A = 25°C T_A = 70°C	$f_{CUTOFF} \geq$ 70kHz $f_{CUTOFF} \geq$ 60kHz

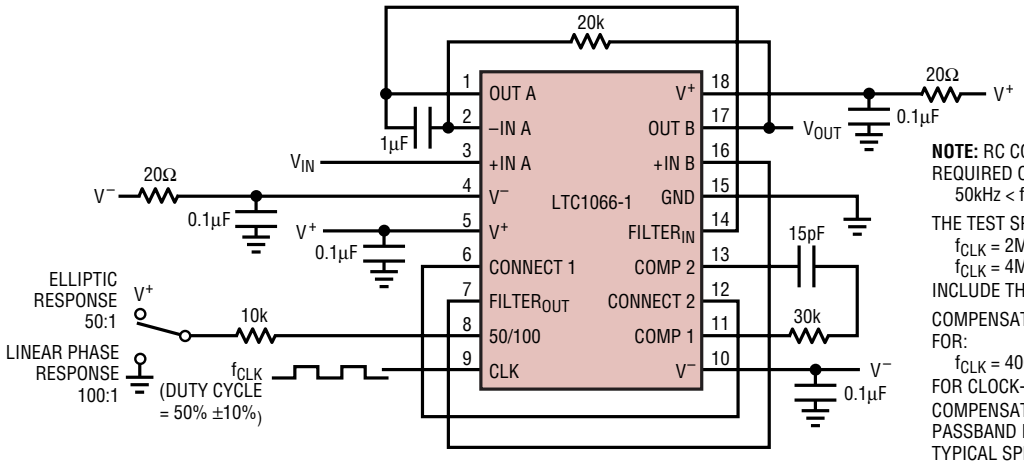
Connect Pins (6, 12)

Pin 6 (CONNECT 1) and pin 12 (CONNECT 2) should be shorted. In a printed circuit board the connection should be done under the IC package through a short trace surrounded by the analog ground plane. Pin 6 should be 0.2 inches away from any other circuit trace.

BLOCK DIAGRAM



TEST CIRCUIT



NOTE: RC COMPENSATION BETWEEN PINS 11 AND 13 IS REQUIRED ONLY FOR CLOCK-TUNABLE OPERATION FOR:
$50kHz < f_{CUTOFFs} \leq 100kHz$.

THE TEST SPECIFICATIONS FOR:
$f_{CLK} = 2MHz$, $f_{CUTOFF} = 40kHz$, AND
$f_{CLK} = 4MHz$, $f_{CUTOFF} = 80kHz$
INCLUDE THE EFFECTS OF RC COMPENSATION.

COMPENSATION DOES NOT INFLUECE THE SPECIFICATIONS FOR:
$f_{CLK} = 400kHz$, $f_{CUTOFF} = 8kHz$.
FOR CLOCK-TUNABLE $f_{CUTOFFs}$ FROM 2kHz TO 50kHz COMPENSATION IS NOT REQUIRED AND THE FILTER'S PASSBAND PERFORMANCE IS REPRESENTED BY THE TYPICAL SPECIFICATIONS AT:
$f_{CLK} = 400kHz$, $f_{CUTOFF} = 8kHz$.

1066-1 TC01

APPLICATIONS INFORMATION

DC PERFORMANCE

The DC performance of the LTC1066-1 is dictated by the DC characteristics of the input precision op amp.

1. DC input voltages in the vicinity of the filter's half of the total power supply are processed with exactly 0dB (or 1V/V) of gain.

2. The typical DC input voltage ranges are equal to:

   $V_{IN} = \pm 5.8V$, $V_S = \pm 7.5V$
   $V_{IN} = \pm 3.6V$, $V_S = \pm 5V$
   $V_{IN} = \pm 1.4V$, $V_S = \pm 2.5V$

   With an input DC voltage range of $V_{IN} = \pm 5V$, ($V_S = \pm 7.5V$), the measured CMRR was 100dB. Figure 1 shows the DC gain linearity of the filter exceeding the requirements of a 14-bit, 10V full scale system.

3. The filter output DC offset $V_{OS(OUT)}$ is measured with the input grounded and with dual power supplies. The $V_{OS(OUT)}$ is typically ±0.1mV and it is optimized for the filter connection shown in the test circuit figure. The filter output offset is equal to:

   $$V_{OS(OUT)} = V_{OS}\,(\text{op amp A}) - I_{BIAS} \times R_F = 0.1mV\,(\text{Typ})$$

4. The $V_{OS(OUT)}$ temperature drift is typically 7µV/°C ($T_A > 25°C$), and –7µV/°C ($T_A < 25°C$).

5. The $V_{OS(OUT)}$ temperature drift can be improved by using an input resistor R_{IN} equal to the feedback resistor R_F, however, the absolute value of $V_{OS(OUT)}$ will increase. For instance, if a 20k resistor is added in series with pin 3 (see Test Circuit), the output V_{OS} drift will be improved by 2µV/°C to 3µV/°C, however, the $V_{OS(OUT)}$ may increase by $1mV_{(MAX)}$.

6. The filter DC output offset voltage $V_{OS(OUT)}$ is independent from the filter clock frequency ($f_{CLK} \leq 250kHz$).

   Figures 2 and 3 show the $V_{OS(OUT)}$ variation for three different power supplies and for clock frequencies up to 5MHz. Both figures were traced with the LTC1066-1 soldered into the PC board. Power supply decoupling is very important, especially with ±7.5V supplies. If necessary connect a small resistor (20Ω) between pins 5 and 18, and between pins 10 and 4, to isolate the precision op amp supply pin from the switched capacitor network supply (see the Test Circuit).

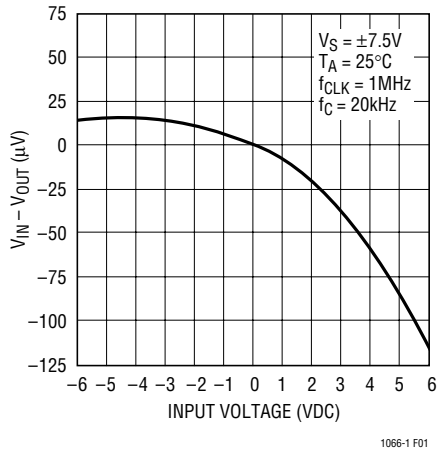


Figure 1. DC Gain Linearity

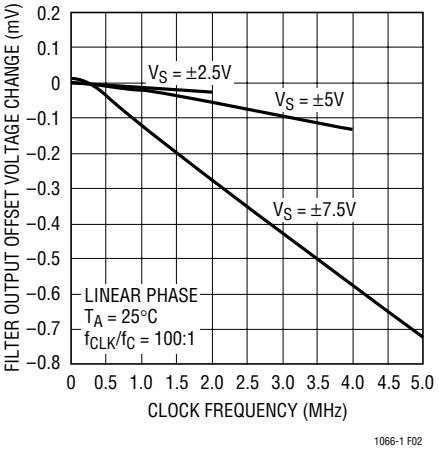


Figure 2. Output Offset Change vs Clock (Relative to Offset for f_{CLK} = 250kHz)

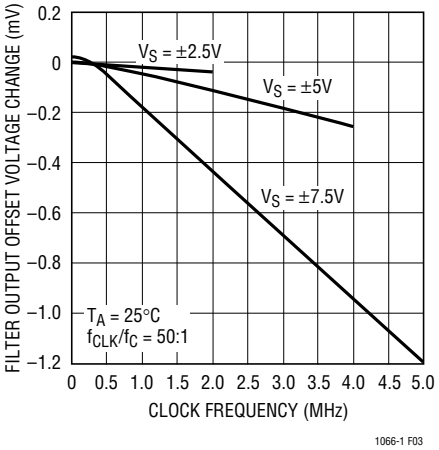


Figure 3. Output Offset Change vs Clock (Relative to Offset for f_{CLK} = 250kHz)

APPLICATIONS INFORMATION

AC PERFORMANCE

AC (Passband) Gain

The passband gain of the LTC1066-1 is equal to the passband gain of the internal switched-capacitor lowpass filter, and it is measured at $f = 0.25f_{CUTOFF}$. Unlike conventional monolithic filters, the LTC1066-1 starts with an absolutely perfect 0dB DC gain and phases into an "imperfect" AC passband gain, typically ±0.1dB.

The filter's low passband ripple, typically 0.05dB, is measured with respect to the AC passband gain.

The LTC1066-1 DC stabilizing loop slightly warps the filter's passband performance if the –3dB frequency of the feedback passive elements ($1/2\pi R_F C_F$) is more than the cutoff frequency of the internal switched-capacitor filter divided by 250. The LTC1066-1 clock tunability directly relates to the above constraint. Figure 4 illustrates the passband behavior of the LTC1066-1 and it demonstrates the clock tunability of the device. A typical LTC1066-1 device was used to trace all four curves of Figure 4. Curve D, for instance, has nearly zero ripple and 0.04dB passband gain. Curve D's 20kHz cutoff is much higher than the 8Hz cutoff frequency of the R_FC_F feedback network, so its passband is free from any additional error due to R_FC_F feedback elements. Curve B illustrates the passband error when the 1MHz clock of curve D is lowered to 100kHz. A 0.1dB error is added to the filter's original AC gain of 0.04dB.

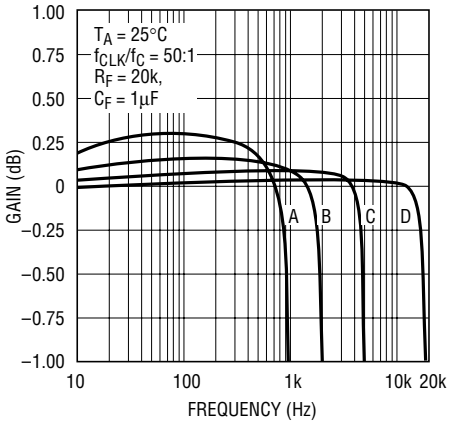


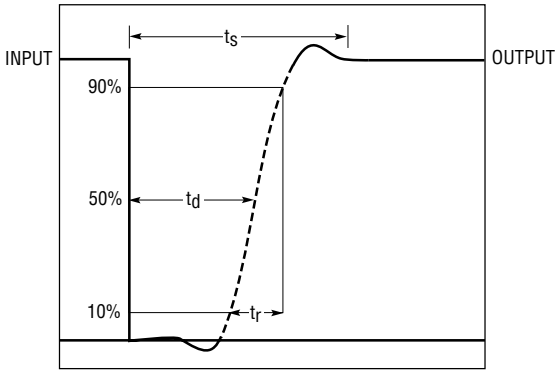
Figure 4. Passband Behavior

APPLICATIONS INFORMATION

Transient Response and Settling Time

The LTC1066-1 exhibits two different transient behaviors. First, during power-up the DC correcting loop will settle after the voltage offset of the internal switched-capacitor network is stored across the feedback capacitor C_F (see Block Diagram). It takes approximately five time constants ($5R_FC_F$) for settling to 1%. Second, following DC loop settling, the filter reaches steady state. The filter transient response is then defined by the frequency characteristics of the internal switched-capacitor lowpass filter. Figure 5 shows details.

DC loop settling is also observed if, at steady state, the DC offset of the internal switched-capacitor network suddenly changes. A sudden change may occur if the clock frequency is instantaneously stepped to a value above 1MHz.



	50:1 ELLIPTIC	100:1 LINEAR PHASE
RISE TIME (t_r)	$\frac{0.43}{f_{CUTOFF}}$ ±5%	$\frac{0.43}{f_{CUTOFF}}$ ±5%
SETTLING TIME (t_s)	$\frac{3.4}{f_{CUTOFF}}$ ±5%	$\frac{2.05}{f_{CUTOFF}}$ ±5%
DELAY TIME (t_d)	$\frac{0.709}{f_{CUTOFF}}$ ±5%	$\frac{0.556}{f_{CUTOFF}}$ ±5%

1066-1 F05

Figure 5. Transient Response

Clock Feedthrough

Clock feedthrough is defined as the RMS value of the clock frequency and its harmonics that are present at the filter's output pin (9). The clock feedthrough is tested with the input pin (2) grounded and depends on PC board layout and on the value of the power supplies. With proper layout techniques the values of the clock feedthrough are shown on Table 7.

Table 7. Clock Feedthrough

POWER SUPPLY	50:1	100:1
Single 5V	$70\mu V_{RMS}$	$90\mu V_{RMS}$
±5V	$100\mu V_{RMS}$	$200\mu V_{RMS}$
±7.5V	$160\mu V_{RMS}$	$650\mu V_{RMS}$

Wideband Noise

The wideband noise of the filter is the total RMS value of the device's noise spectral density and is used to determine the operating signal-to-noise ratio. Most of its frequency contents lie within the filter passband and cannot be reduced with post filtering. For instance, the LTC1066-1 wideband noise at ±5V supply is $100\mu V_{RMS}$, $95\mu V_{RMS}$ of which have frequency contents from DC up to the filter's cutoff frequency. The total wideband noise (μV_{RMS}) is nearly independent of the value of the clock. The clock feedthrough specifications are not part of the wideband noise. Table 8 lists the typical wideband noise for each supply.

Table 8. Wideband Noise

POWER SUPPLY	50:1	100:1 (Pin 8 to GND)
Single 5V	$90\mu V_{RMS}$	$80\mu V_{RMS}$
±5V	$100\mu V_{RMS}$	$85\mu V_{RMS}$
±7.5V	$106\mu V_{RMS}$	$90\mu V_{RMS}$

Speed Limitations

To avoid op amp slew rate limiting at maximum clock frequencies, the signal amplitude should be kept below a specified level as shown in Table 9.

Table 9. Maximum V_{IN}

INPUT FREQUENCY	MAXIMUM V_{IN}
≥250kHz	$0.50V_{RMS}$
≥700kHz	$0.25V_{RMS}$

APPLICATIONS INFORMATION

Aliasing

In a sampled-data system the sampling theorem says that if an input signal has any frequency components greater than one half the sampling frequency, aliasing errors will appear at the output. In practice, aliasing is not always a serious problem. High order switched-capacitor lowpass filters are inherently band limited and significant aliasing occurs only for input signals centered around the clock frequency and its multiples.

Figure 6 shows the LTC1066-1 aliasing response when operated with a clock-to-cutoff frequency ratio of 50:1. With a 50:1 ratio LTC1066-1 samples its input twice during one clock period and the sampling frequency is equal to two times the clock frequency.

The figure also shows the maximum aliased output generated for inputs in the range of $2f_{CLK} \pm f_C$. For instance, if the LTC1066-1 is programmed to produce a cutoff frequency of 20kHz with 1MHz clock, a 10mV, 1.02MHz input signal will cause a 10μV aliased signal at 20kHz. This signal will be buried in the noise. Maximum aliasing will occur only for input signals in the narrow range of 2MHz ±20kHz or multiples of 2MHz.

Figure 7 shows the LTC1066-1 aliased response when operated with a clock-to-cutoff frequency ratio of 100:1 (linear phase response with pin 8 to ground).

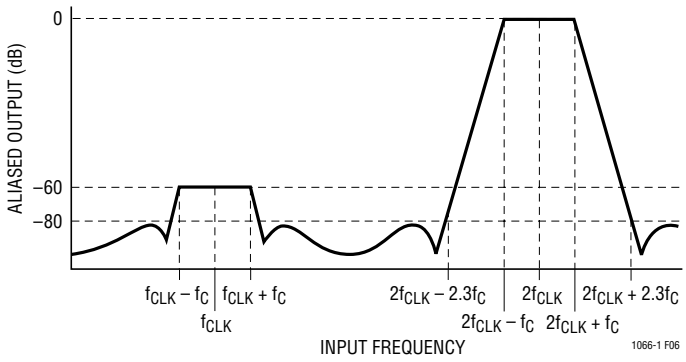


Figure 6. Aliasing vs Frequency f_{CLK}/f_C = 50:1 (Pin 8 to V^+) Clock is a 50% Duty Cycle Square Wave

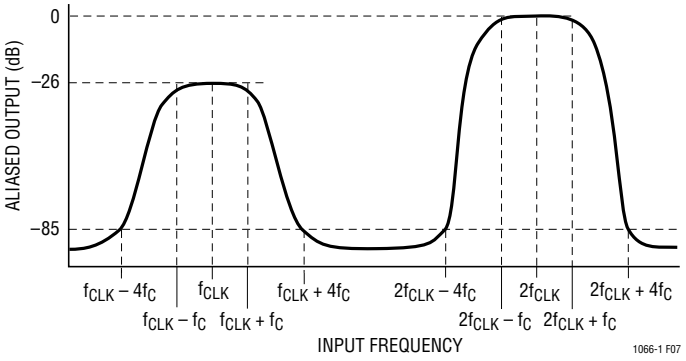
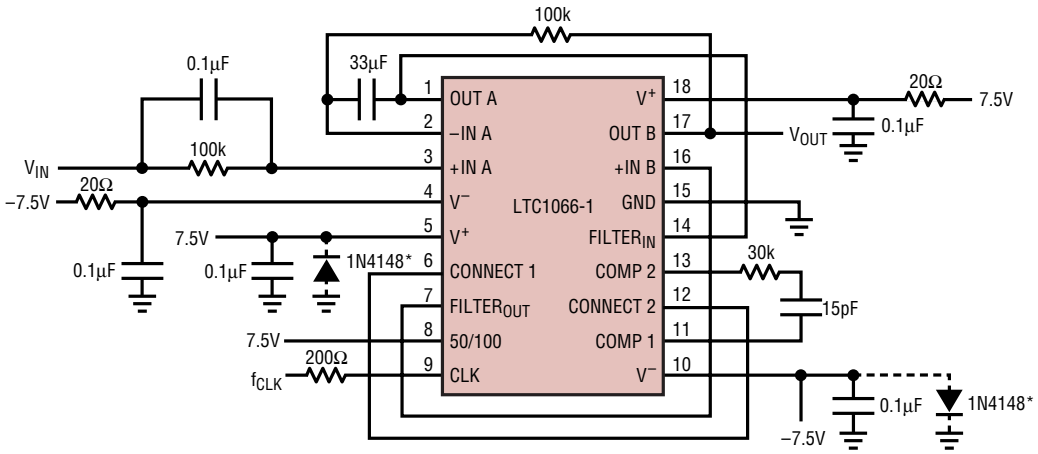


Figure 7. Aliasing vs Frequency f_{CLK}/f_C = 100:1 (Pin 8 to Ground) Clock is a 50% Duty Cycle Square Wave

TYPICAL APPLICATION

Dual Supply Operation
DC Accurate, *10Hz to 100kHz*, Clock-Tunable, 8th Order Elliptic Lowpass Filter
f_{CLK}/f_C = 50:1



MAXIMUM OUTPUT VOLTAGE OFFSET = ±5.5mV, DC LINEARITY = ±0.0063%, T_A = 25°C.

THE PINS 6 TO 12 CONNECTION SHOULD BE UNDER THE IC AND SHIELDED BY AN ANALOG SYSTEM GROUND PLANE.

RC COMPENSATION BETWEEN PINS 11 AND 13 REQUIRED ONLY FOR $f_{CUTOFF} \geq$ 60kHz.

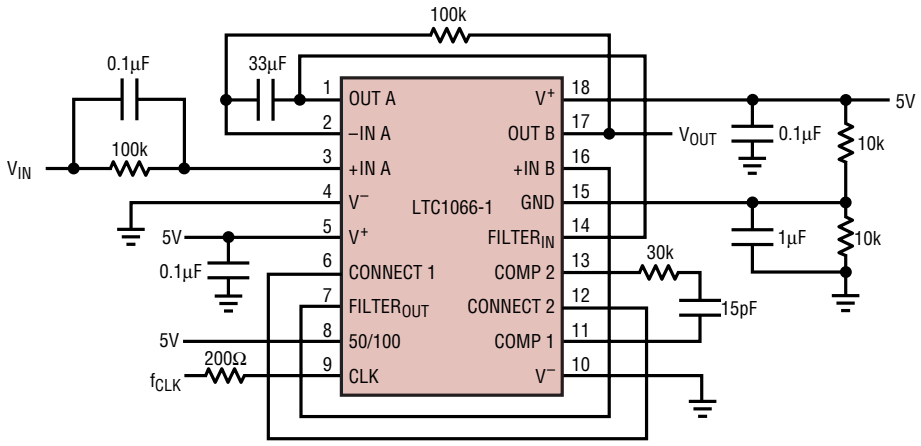
THE 33µF CAPACITOR IS A NONPOLARIZED, ALUMINUM ELECTROLYTIC, ±20%, 16V (NICHICON UUPIC 330MCRIGS OR NIC NACEN 33M16V 6.3 × 5.5 OR EQUIVALENT).

* PROTECTION DIODES, 1N4148 ARE OPTIONAL. SEE PIN DESCRIPTIONS.

1066-1 TA03

TYPICAL APPLICATION

Single 5V Supply Operation
DC Accurate, *10Hz to 36kHz*, Clock-Tunable, 8th Order Elliptic Lowpass Filter
f_{CLK}/f_C = 50:1



INPUT LINEAR RANGE = 1.4V to 3.6V. DC LINEARITY = ±0.0063%.

THE PINS 6 TO 12 CONNECTION SHOULD BE UNDER THE IC AND SHIELDED BY AN ANALOG SYSTEM GROUND PLANE.

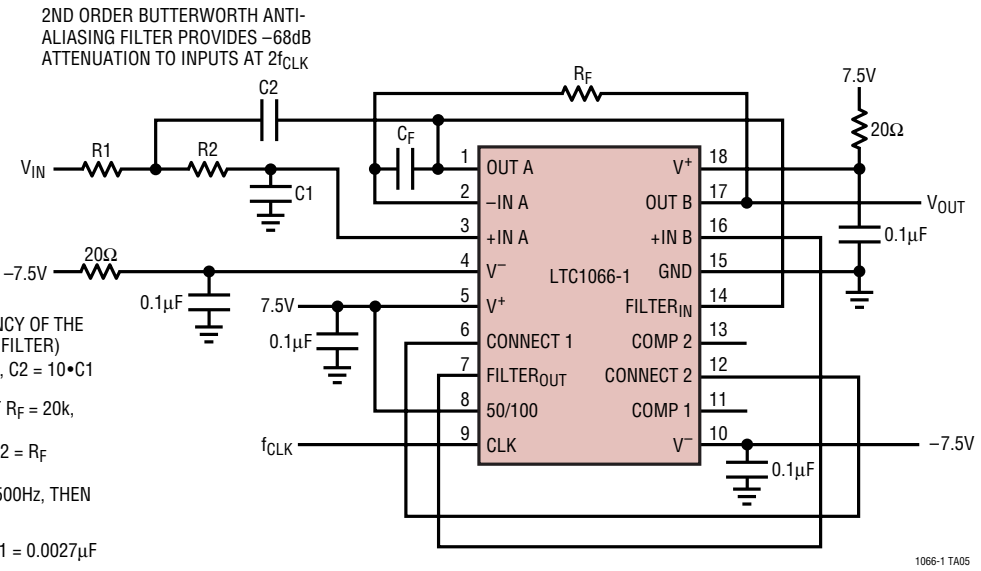
RC COMPENSATION BETWEEN PINS 11 AND 13 REQUIRED ONLY FOR $f_{CUTOFF} \geq 24$kHz.

THE 33µF CAPACITOR IS A NONPOLARIZED, ALUMINUM ELECTROLYTIC, ±20%, 16V (NICHICON UUPIC 330MCRIGS OR NIC NACEN 33M16V 6.3 × 5.5)

1066-1 TA04

TYPICAL APPLICATION

DC Accurate Lowpass Filter with Input Anti-Aliasing
($f_{CLK} \leq 250kHz$)



$f_{CUTOFF} = \frac{f_{CLK}}{50}$, $\frac{1}{2\pi R_F C_F} = \frac{f_{CUTOFF}}{250}$

$f_{-3dB} = 2 \bullet f_{CUTOFF}$ (f_{-3dB} IS THE –3dB FREQUENCY OF THE 2ND ORDER ANTI-ALIASING FILTER)

$\frac{1}{2\pi(R1 + R2)C1} = 0.707 \bullet f_{-3dB}$, R2 = 17.946•R1, C2 = 10•C1

FOR CUTOFF FREQUENCIES 2kHz TO 5kHz, SET R_F = 20k, C_F = 1µF AND R1 + R2 ≤ 2k

FOR CUTOFF FREQUENCIES <2kHz, SET R1 + R2 = R_F

FOR EXAMPLE:

IF THE CUTOFF FREQUENCY OF LTC1066-1 IS 500Hz, THEN f_{-3dB} = 1000Hz

$\frac{1}{2\pi R_F C_F}$ = 2Hz, SET R_F = 80.6k, C_F = 1µF AND C1 = 0.0027µF

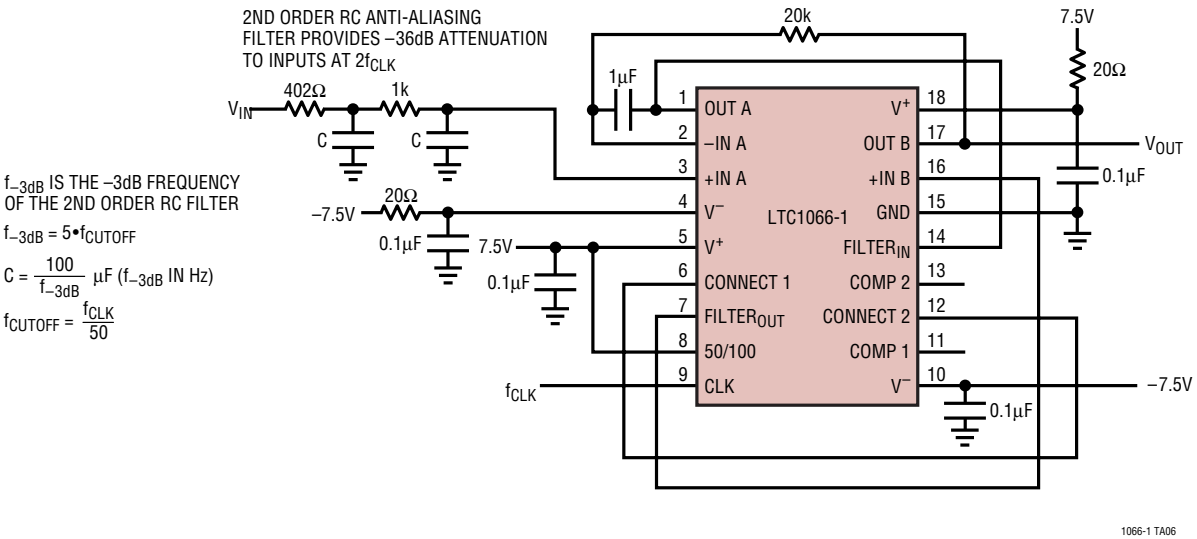
R1 + R2 = 80.6k, R1 = 4.22k AND R2 = 76.8k ROUNDED TO NEAREST 1% VALUE.

C2 = 0.027µF ROUNDED TO NEAREST STANDARD VALUE.

NOTE: R_F SHOULD BE ≤100k TO MINIMIZE DC OFFSET TO ±5.5mV

TYPICAL APPLICATION

DC Accurate Lowpass Filter with Input Anti-Aliasing (f_{CLK} > 250kHz)



f_{-3dB} IS THE –3dB FREQUENCY OF THE 2ND ORDER RC FILTER

$f_{-3dB} = 5 \bullet f_{CUTOFF}$

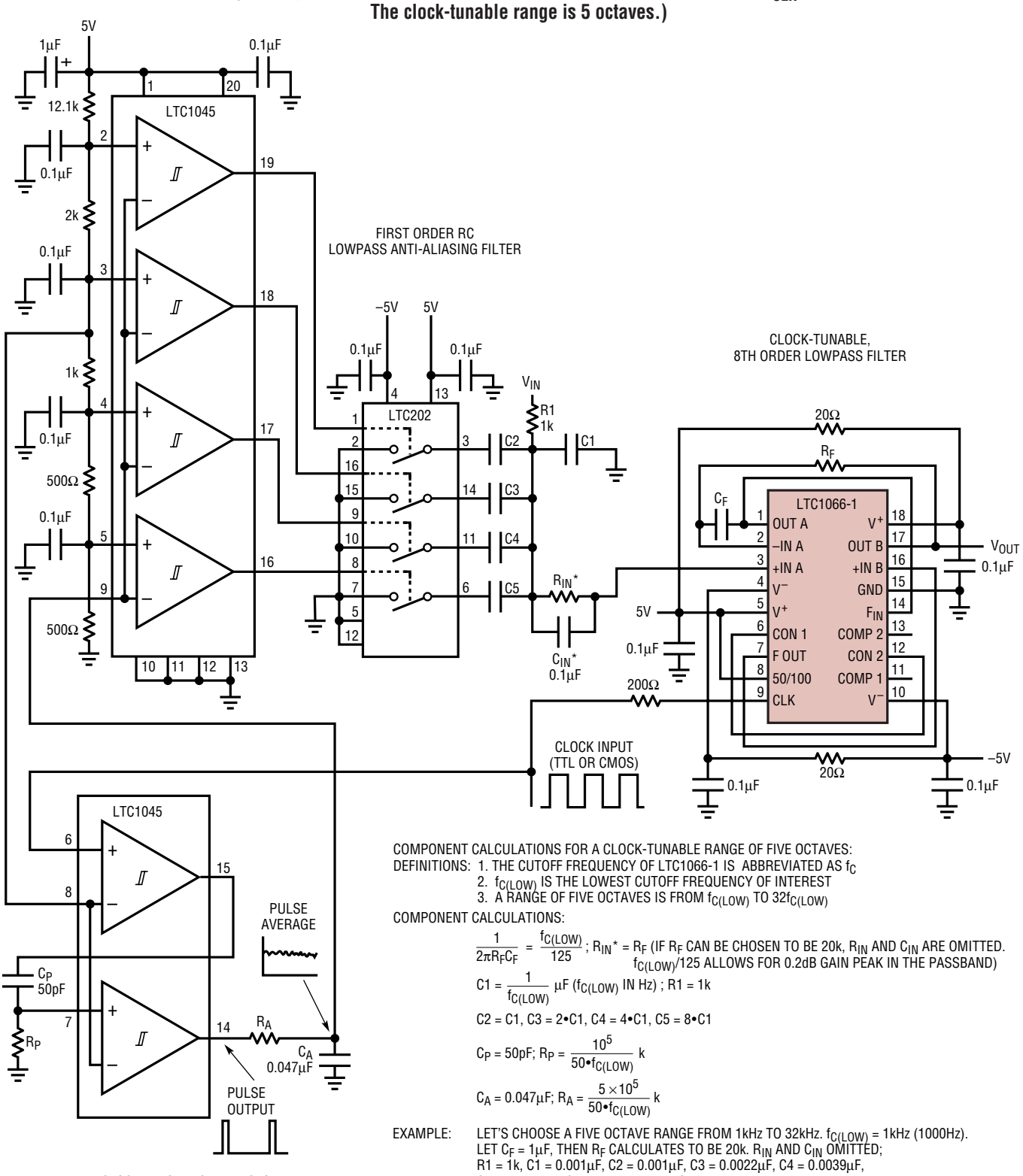
$C = \frac{100}{f_{-3dB}}$ µF (f_{-3dB} IN Hz)

$f_{CUTOFF} = \frac{f_{CLK}}{50}$

1066-1 TA06

TYPICAL APPLICATION

DC Accurate Clock-Tunable Lowpass Filter with Tunable Input Anti-Aliasing Filter
(Circuit provides at least –20dB attenuation to input frequencies at $2f_{CLK}$.
The clock-tunable range is 5 octaves.)



COMPONENT CALCULATIONS FOR A CLOCK-TUNABLE RANGE OF FIVE OCTAVES:

DEFINITIONS:
1. THE CUTOFF FREQUENCY OF LTC1066-1 IS ABBREVIATED AS f_C
2. $f_{C(LOW)}$ IS THE LOWEST CUTOFF FREQUENCY OF INTEREST
3. A RANGE OF FIVE OCTAVES IS FROM $f_{C(LOW)}$ TO $32f_{C(LOW)}$

COMPONENT CALCULATIONS:

$$\frac{1}{2\pi R_F C_F} = \frac{f_{C(LOW)}}{125};\ R_{IN}{}^* = R_F$$ (IF R_F CAN BE CHOSEN TO BE 20k, R_{IN} AND C_{IN} ARE OMITTED. $f_{C(LOW)}/125$ ALLOWS FOR 0.2dB GAIN PEAK IN THE PASSBAND)

$$C1 = \frac{1}{f_{C(LOW)}}\ \mu F\ (f_{C(LOW)}\ \text{IN Hz});\ R1 = 1k$$

$C2 = C1,\ C3 = 2 \bullet C1,\ C4 = 4 \bullet C1,\ C5 = 8 \bullet C1$

$$C_P = 50pF;\ R_P = \frac{10^5}{50 \bullet f_{C(LOW)}}\ k$$

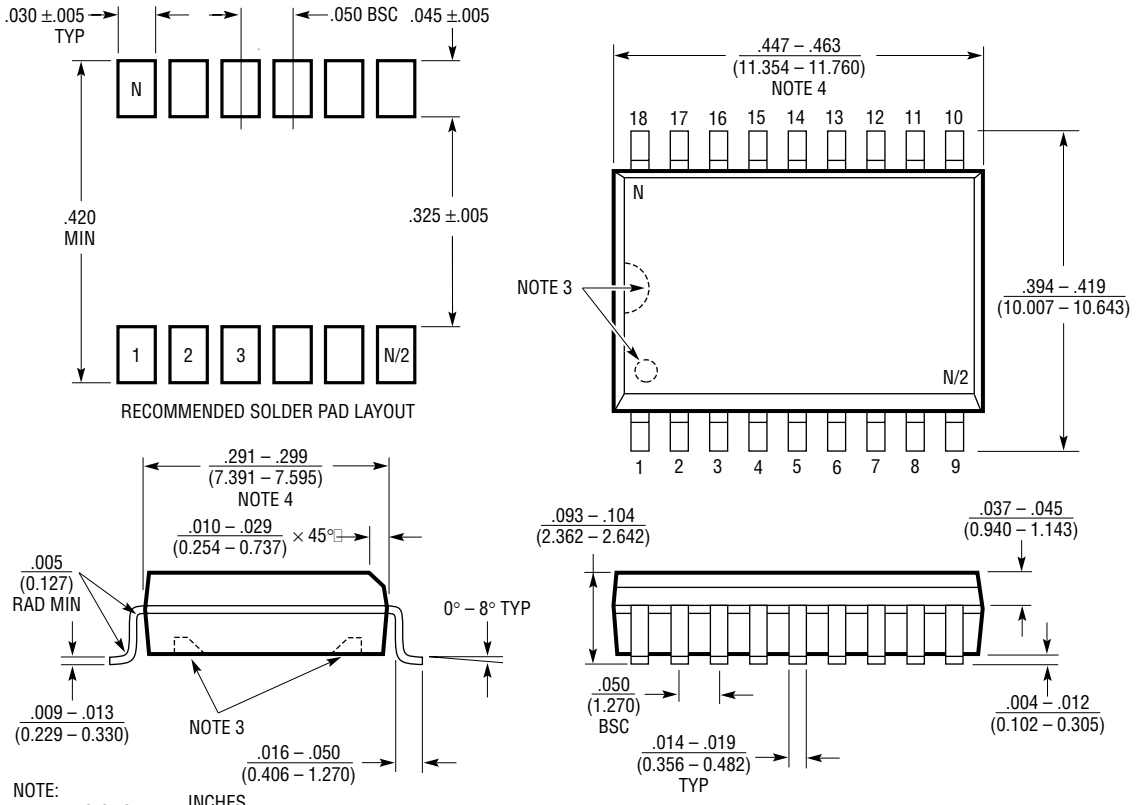
$$C_A = 0.047\mu F;\ R_A = \frac{5 \times 10^5}{50 \bullet f_{C(LOW)}}\ k$$

EXAMPLE: LET'S CHOOSE A FIVE OCTAVE RANGE FROM 1kHz TO 32kHz. $f_{C(LOW)}$ = 1kHz (1000Hz). LET C_F = 1µF, THEN R_F CALCULATES TO BE 20k. R_{IN} AND C_{IN} OMITTED; R1 = 1k, C1 = 0.001µF, C2 = 0.001µF, C3 = 0.0022µF, C4 = 0.0039µF, C5 = 0.0082µF. C_P = 50pF, R_P = 2k, C_A = 0.047µF, R_A = 10k

1066-1 TA07

PACKAGE DESCRIPTION

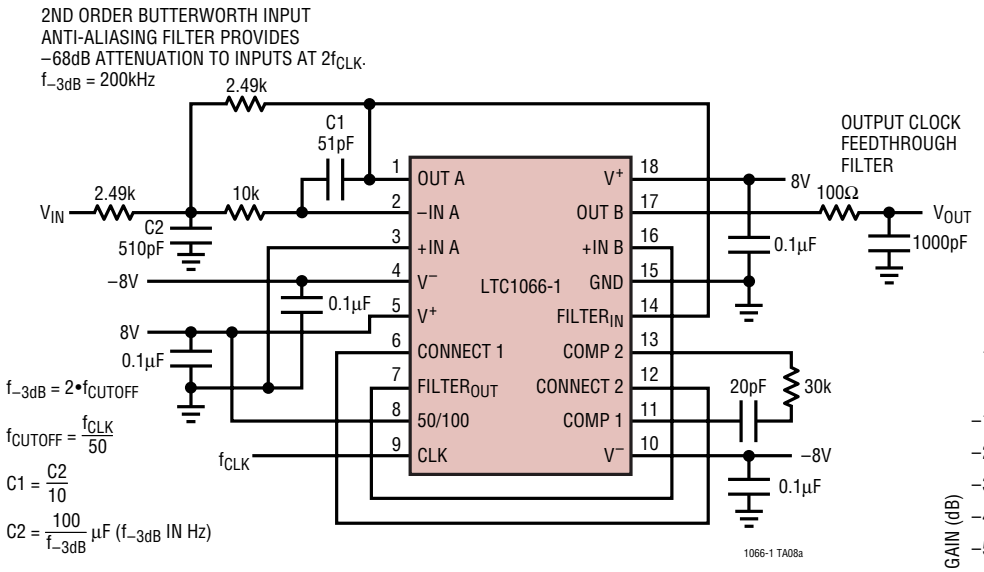
SW Package
18-Lead Plastic Small Outline (Wide .300 Inch)
(Reference LTC DWG # 05-08-1620)



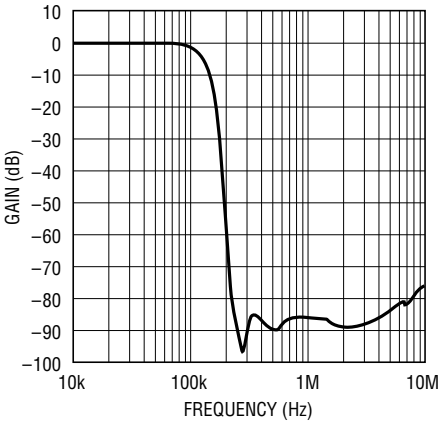
NOTE:
1. DIMENSIONS IN $\frac{\text{INCHES}}{(\text{MILLIMETERS})}$
2. DRAWING NOT TO SCALE
3. PIN 1 IDENT, NOTCH ON TOP AND CAVITIES ON THE BOTTOM OF PACKAGES ARE THE MANUFACTURING OPTIONS. THE PART MAY BE SUPPLIED WITH OR WITHOUT ANY OF THE OPTIONS
4. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .006" (0.15mm)

TYPICAL APPLICATIONS

100kHz Elliptic Lowpass Filter with Input Anti-Aliasing and Output Clock Feedthrough Filters (Not DC Accurate)



Gain vs Frequency



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1063	Clock-Tunable 5th Order Butterworth Lowpass	1mV Offset, 80dB CMR
LTC1065	Clock-Tunable 5th Order Bessel Lowpass Filter	1mV Offset, 80dB CMR
LTC1565-31	650kHz Linear Phase Lowpass Filter	Continuous Time, Fully Diff In/Out
LTC1566-1	Low Noise, 2.3MHz Lowpass Filter	Continuous Time, Fully Diff In/Out
LT1567	Low Noise Op Amp and Inverter Building Block	Single Ended to Differential Conv
LT1568	Low Noise, 10MHz 4th Order Building Block	Lowpass or Bandpass, Diff Outputs
LT6600-2.5	Low Noise Differential Amp and 10MHz Lowpass	55µV_{RMS} Noise 100kHz to 10MHz, 3V Supply
LT6600-10	Low Noise Differential Amp and 20MHz	Lowpass 86µV_{RMS} Noise 100kHz to 20MHz, 3V Supply

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