

Low Voltage Ideal Diode Controller with Monitoring

FEATURES

- **Low Loss Replacement for Power Diode**
- **Controls N-Channel MOSFET**
- **0V to 18V Supply ORing or Holdup**
- **0.5 μ s Turn-On and Turn-Off Time**
- Undervoltage and Overvoltage Protection
- Open MOSFET Detect
- Status and Fault Outputs
- Hot Swappable
- Reverse Current Enable Input
- 12-Pin MSOP and DFN (3mm \times 3mm) Packages

APPLICATIONS

- Redundant Power Supplies
- Supply Holdup
- Telecom Infrastructure
- Computer Systems and Servers

DESCRIPTION

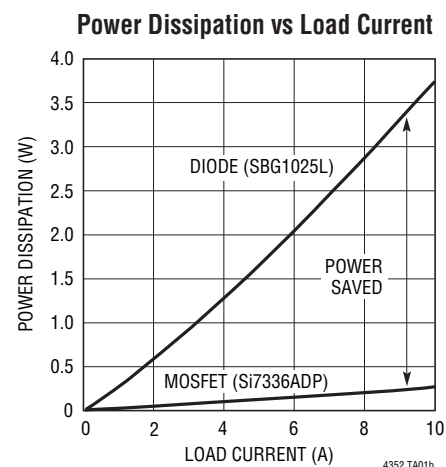
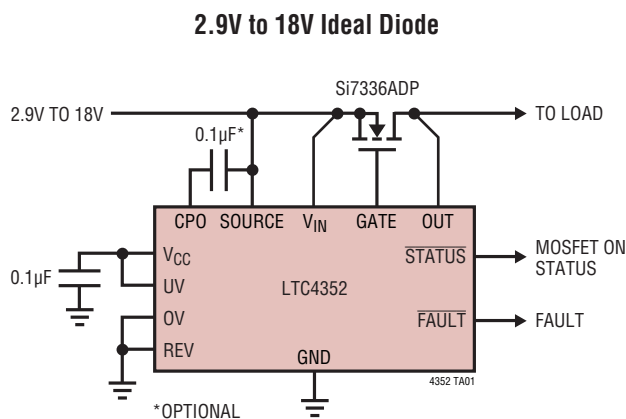
The LTC®4352 creates a near-ideal diode using an external N-channel MOSFET. It replaces a high power Schottky diode and the associated heat sink, saving power and board area. The ideal diode function permits low loss power ORing and supply holdup applications.

The LTC4352 regulates the forward voltage drop across the MOSFET to ensure smooth current transfer in diode-OR applications. A fast turn-on reduces the load voltage droop during supply switch-over. If the input supply fails or is shorted, a fast turn-off minimizes reverse currents.

The controller operates with supplies from 2.9V to 18V. For lower voltages, an external supply is needed at the V_{CC} pin. Power passage is disabled during undervoltage or overvoltage conditions. The controller also features an open MOSFET detect circuit that flags excessive voltage drop across the pass transistor in the on state. A REV pin enables reverse current, overriding the diode behavior when desired.

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TYPICAL APPLICATION



LTC4352

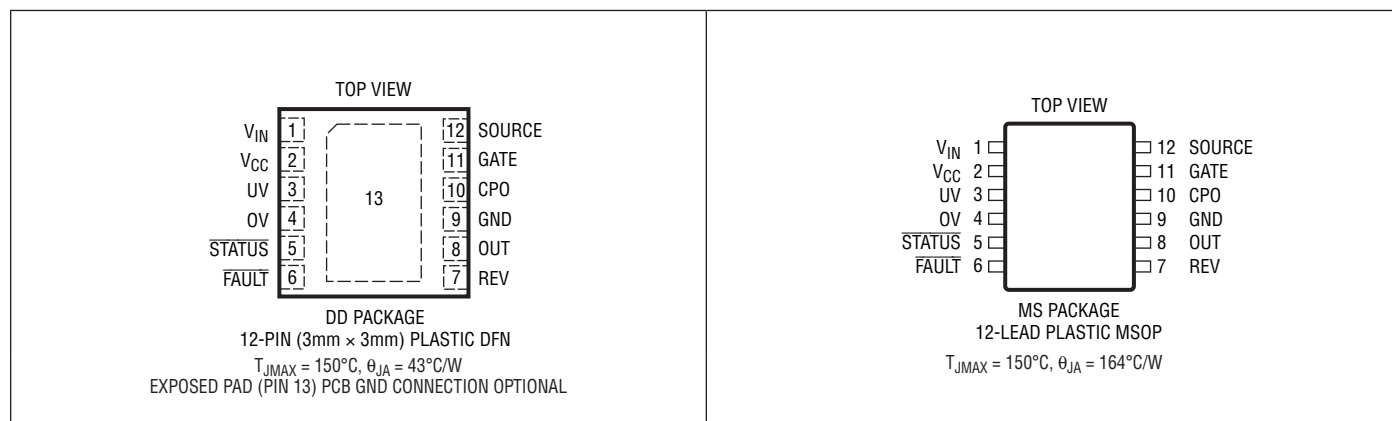
ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2)

| | |
|--|--------------|
| V_{IN} , SOURCE Voltages | –2V to 24V |
| V_{CC} Voltage | –0.3V to 7V |
| OUT Voltage | –2V to 24V |
| CPO, GATE Voltages (Note 3) | –0.3V to 30V |
| CPO D.C. Current | 10mA |
| UV, OV, REV Voltages | –0.3V to 24V |
| \overline{FAULT} , STATUS Voltages | –0.3V to 24V |

| | |
|--|----------------|
| \overline{FAULT} , STATUS Currents | 5mA |
| Operating Ambient Temperature Range | |
| LTC4352C | 0°C to 70°C |
| LTC4352I | –40°C to 85°C |
| LTC4352H | –40°C to 150°C |
| Storage Temperature Range | –65°C to 150°C |
| Lead Temperature (Soldering, 10 sec) | |
| MS Package | 300°C |

PIN CONFIGURATION



ORDER INFORMATION

| LEAD FREE FINISH | TAPE AND REEL | PART MARKING* | PACKAGE DESCRIPTION | TEMPERATURE RANGE |
|------------------|------------------|---------------|--------------------------------|-------------------|
| LTC4352CDD#PBF | LTC4352CDD#TRPBF | LDPJ | 12-Pin (3mm × 3mm) Plastic DFN | 0°C to 70°C |
| LTC4352IDD#PBF | LTC4352IDD#TRPBF | LDPJ | 12-Pin (3mm × 3mm) Plastic DFN | –40°C to 85°C |
| LTC4352HDD#PBF | LTC4352HDD#TRPBF | LDPJ | 12-Pin (3mm × 3mm) Plastic DFN | –40°C to 150°C |
| LTC4352CMS#PBF | LTC4352CMS#TRPBF | 4352 | 12-Lead Plastic MSOP | 0°C to 70°C |
| LTC4352IMS#PBF | LTC4352IMS#TRPBF | 4352 | 12-Lead Plastic MSOP | –40°C to 85°C |
| LTC4352HMS#PBF | LTC4352HMS#TRPBF | 4352 | 12-Lead Plastic MSOP | –40°C to 150°C |

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: <http://www.linear.com/leadfree/>

For more information on tape and reel specifications, go to: <http://www.linear.com/tapeandree/>

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$. $V_{IN} = 12\text{V}$, $V_{SOURCE} = V_{IN}$, $V_{OUT} = V_{IN}$, V_{CC} Open, unless otherwise noted.

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|----------------------------|---|--|---|--------------|----------------|----------|---------------|
| Supplies | | | | | | | |
| V_{IN} | Input Operating Range | | ● | 2.9 | | 18 | V |
| | | With External 2.9V to 4.7V V_{CC} Supply | ● | 0 | | V_{CC} | V |
| | | With External 4.7V to 6V V_{CC} Supply | ● | 0 | | 18 | V |
| $V_{CC(EXT)}$ | V_{CC} External Supply Range | | ● | 2.9 | | 6 | V |
| $V_{CC(INT)}$ | V_{CC} Internal Regulator Voltage | | ● | 3.5 | 4.1 | 4.7 | V |
| I_{IN} | V_{IN} Supply Current | | ● | | 1.4 | 3 | mA |
| | | $V_{IN} = 0\text{V}$, $V_{CC} = 5\text{V}$, $V_{OUT} = 18\text{V}$ | ● | | -10 | -13 | μA |
| | | $V_{IN} = 0\text{V}$, $V_{CC} = 5\text{V}$, $V_{OUT} = 18\text{V}$ (LTC4352H) | ● | | -10 | -25 | μA |
| I_{CC} | External V_{CC} Supply Current | $V_{CC} = 5\text{V}$, $V_{IN} = 0\text{V}$ | ● | | 1.25 | 2.5 | mA |
| $V_{CC(UVLO)}$ | V_{CC} Undervoltage Lockout Threshold | V_{CC} Rising | ● | 2.45 | 2.57 | 2.7 | V |
| $\Delta V_{CC(HYST)}$ | V_{CC} Undervoltage Lockout Hysteresis | | ● | 50 | 70 | 90 | mV |
| Ideal Diode Control | | | | | | | |
| $V_{FWD(REG)}$ | Forward Regulation Voltage ($V_{IN} - V_{OUT}$) | | ● | 10 | 25 | 40 | mV |
| ΔV_{GATE} | MOSFET Gate Drive ($V_{GATE} - V_{SOURCE}$) | $V_{FWD} = 0.1\text{V}$, $I = 0$ and $-1\mu\text{A}$ | ● | 5 | 6.1 | 7.5 | V |
| $t_{ON(GATE)}$ | GATE Turn-On Delay | $C_{GATE} = 10\text{nF}$, $V_{FWD} = 0.2\text{V}$ | ● | | 0.25 | 0.5 | μs |
| $t_{OFF(GATE)}$ | GATE Turn-Off Delay | $C_{GATE} = 10\text{nF}$, $V_{FWD} = -0.2\text{V}$ | ● | | 0.2 | 0.5 | μs |
| Input/Output Pins | | | | | | | |
| $V_{UV,OV(TH)}$ | UV, OV Threshold Voltage | V_{UV} Falling, V_{OV} Rising | ● | 490 | 500 | 510 | mV |
| $\Delta V_{UV,OV(HYST)}$ | UV, OV Threshold Hysteresis | | ● | 2.5 | 5 | 8.5 | mV |
| $V_{REV(TH)}$ | REV Threshold Voltage | | ● | 0.8 | 1.0 | 1.2 | V |
| | | (LTC4352H) | ● | 0.8 | 1.0 | 1.25 | V |
| $I_{UV,OV}$ | UV, OV Current | $V = 0.5\text{V}$ | ● | | 0 | ± 1 | μA |
| I_{REV} | REV Current | $V_{REV} = 1\text{V}$ | ● | 7 | 10 | 13 | μA |
| I_{OUT} | OUT Current | $V_{OUT} = 0\text{V}$, 12V | ● | -13 | | 200 | μA |
| I_{SOURCE} | SOURCE Current | $V_{SOURCE} = 0\text{V}$ | ● | | -85 | -130 | μA |
| $I_{CPO(UP)}$ | CPO Pull-Up Current | $V_{CPO} = V_{IN} = 2.9\text{V}$ | ● | -60 | -90 | -115 | μA |
| | | $V_{CPO} = V_{IN} = 18\text{V}$ | ● | -50 | -75 | -100 | μA |
| I_{GATE} | GATE Fast Pull-Up Current | $V_{FWD} = 0.2\text{V}$, $\Delta V_{GATE} = 0\text{V}$, $V_{CPO} = 17\text{V}$ | | | -1.5 | | A |
| | GATE Fast Pull-Down Current | $V_{FWD} = -0.2\text{V}$, $\Delta V_{GATE} = 5\text{V}$ | | | 1.5 | | A |
| | GATE Off Pull-Down Current | $V_{UV} = 0\text{V}$, $\Delta V_{GATE} = 2.5\text{V}$ | ● | 60 | 100 | 145 | μA |
| $I_{FLT,STAT(IN)}$ | STATUS, FAULT Leakage Current | $V = 18\text{V}$ | ● | | 0 | ± 1 | μA |
| $I_{FLT,STAT(UP)}$ | STATUS, FAULT Pull-Up Current | $V = 0\text{V}$ | ● | -8 | -10 | -12 | μA |
| V_{OL} | STATUS, FAULT Output Low Voltage | $I = 1.25\text{mA}$ | ● | | 0.2 | 0.4 | V |
| V_{OH} | STATUS, FAULT Output High Voltage | $I = -1\mu\text{A}$ | ● | $V_{CC} - 1$ | $V_{CC} - 0.5$ | | V |
| $\Delta V_{GATE(ST)}$ | MOSFET On Detect Threshold | STATUS Pulls Low, $V_{FWD} = 50\text{mV}$ | ● | 0.3 | 0.7 | 1.1 | V |
| | | STATUS Pulls Low, $V_{FWD} = 50\text{mV}$ (LTC4352H) | ● | 0.28 | 0.7 | 1.1 | V |
| $V_{FWD(FLT)}$ | Open MOSFET Threshold ($V_{IN} - V_{OUT}$) | FAULT Pulls Low | ● | 200 | 250 | 300 | mV |

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating for extended periods may affect device reliability and lifetime.

Note 2: All currents into device pins are positive; all currents out of device

pins are negative. All voltages are referenced to GND unless otherwise specified.

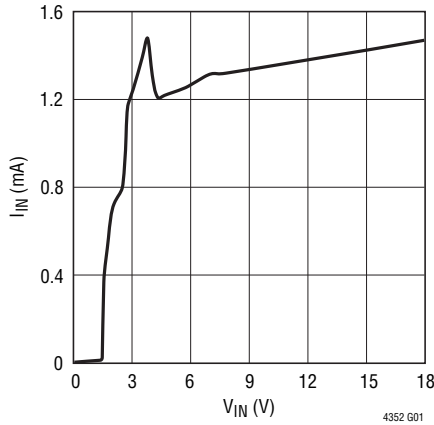
Note 3: Internal clamps limit the GATE and CPO pins to a minimum of 5V above, and a diode below SOURCE. Driving these pins to voltages beyond the clamp may damage the device.

TYPICAL PERFORMANCE CHARACTERISTICS

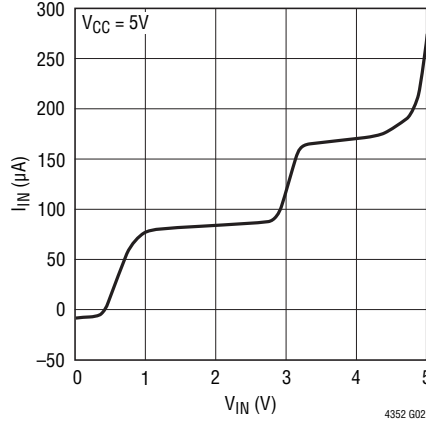
V_{CC} Open, unless otherwise noted.

$T_A = 25^\circ\text{C}$, $V_{IN} = 12\text{V}$, $V_{SOURCE} = V_{IN}$, $V_{OUT} = V_{IN}$,

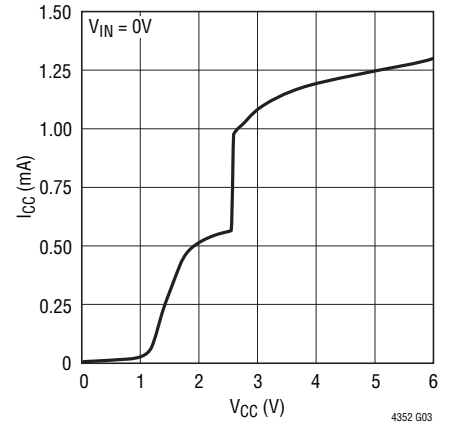
V_{IN} Current vs Voltage



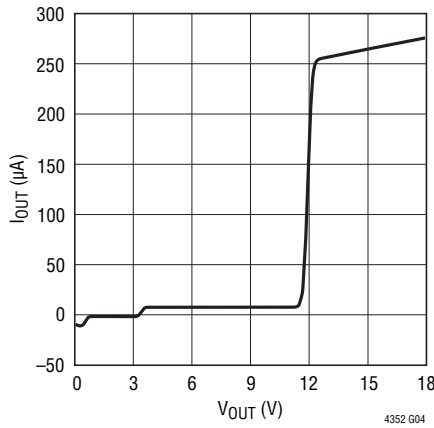
V_{IN} Current vs Voltage with External V_{CC}



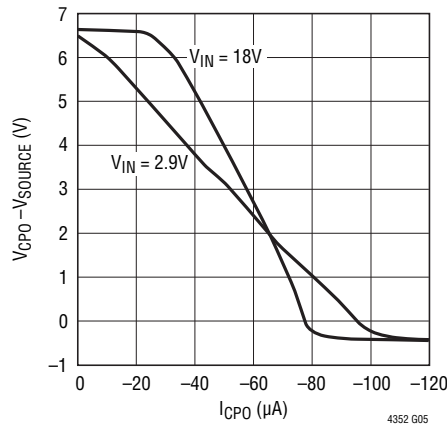
V_{CC} Current vs Voltage



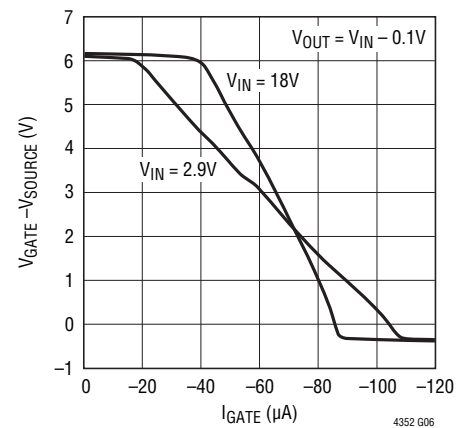
OUT Current vs Voltage



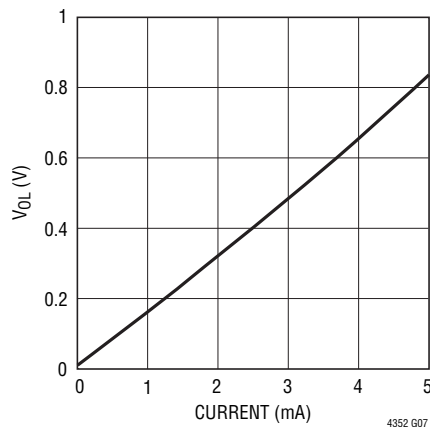
CPO Voltage vs Current



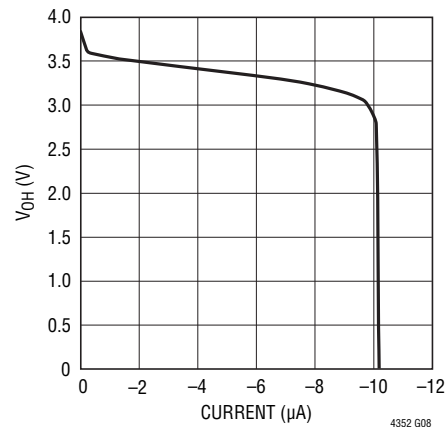
GATE Voltage vs Current



STATUS, FAULT Output Low Voltage vs Current



STATUS, FAULT Output High Voltage vs Current



PIN FUNCTIONS

V_{IN} (Pin 1): Voltage Sense and Supply Input. Connect this pin to the power input side of the MOSFET. The low voltage supply V_{CC} is generated from V_{IN}. The voltage sensed at this pin is used to control the MOSFET gate.

V_{CC} (Pin 2): Low Voltage Supply. Connect a 0.1μF capacitor from this pin to ground. When V_{IN} ≥ 2.9V, this pin provides decoupling for an internal regulator that generates a 4.1V supply. For applications where V_{IN} < 2.9V, connect an external supply voltage in the range 2.9V to 6V to this pin.

UV (Pin 3): Undervoltage Comparator Input. Connect this pin to an external resistive divider from V_{IN}. If the voltage at this pin falls below 0.5V, an undervoltage fault is detected and the MOSFET is turned off. The comparator has a built-in hysteresis of 5mV. Tie to V_{CC} if unused.

OV (Pin 4): Overvoltage Comparator Input. Connect this pin to an external resistive divider from V_{IN}. If the voltage at this pin rises above 0.5V, an overvoltage fault is detected and the MOSFET is turned off. The comparator has a built-in hysteresis of 5mV. Tie to GND if unused.

STATUS (Pin 5): MOSFET Status Output. This pin is pulled low by an open-drain output when the external MOSFET is on. An internal 10μA current source pulls this pin up to a diode below V_{CC}. It may be pulled above V_{CC} using an external pull-up. Tie to GND or leave open if unused.

FAULT (Pin 6): Fault Output. This pin is pulled low by an open-drain output when a fault occurs. This fault could either be an undervoltage fault, an overvoltage fault, or an open MOSFET fault. The external MOSFET is turned off for undervoltage and overvoltage faults, while it is left on for open MOSFET fault. An internal 10μA current source

pulls this pin up to a diode below V_{CC}. It may be pulled above V_{CC} using an external pull-up. Tie to GND or leave open if unused.

REV (Pin 7): Reverse Current Enable Input. Connect this pin to GND for normal diode operation that blocks reverse current. Driving this pin above 1V fully turns on the MOSFET gate to allow reverse current. An internal 10μA current source pulls this pin to GND.

OUT (Pin 8): Output Voltage Sense Input. Connect this pin to the output side of the MOSFET. The voltage sensed at this pin is used to control the MOSFET gate.

GND (Pin 9): Device Ground.

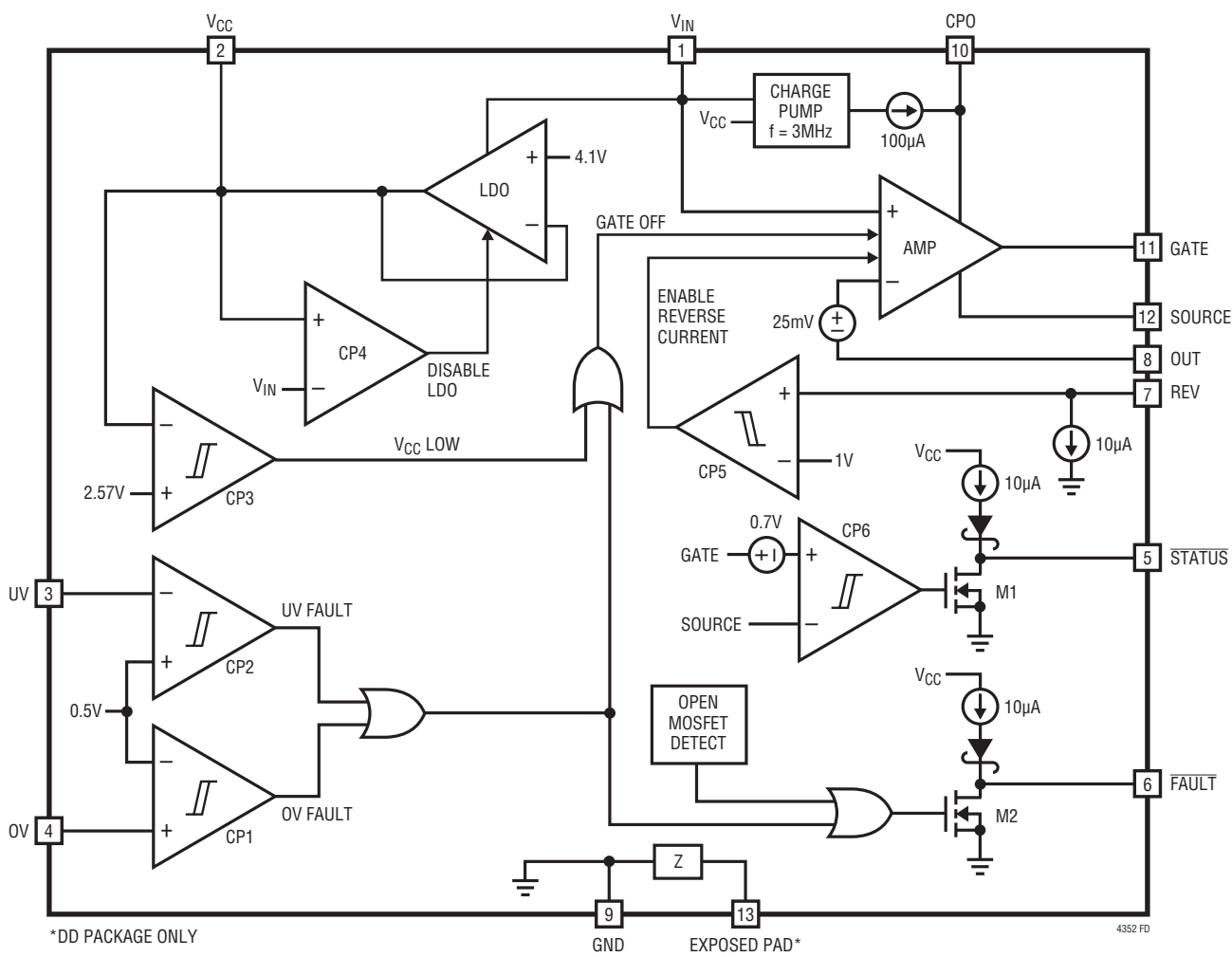
CPO (Pin 10): Charge Pump Output. Connect a capacitor from this pin to the SOURCE pin. The value of this capacitor is approximately 10x the gate capacitance (C_{ISS}) of the MOSFET switch. The charge stored on this capacitor is used to pull-up the gate during a fast turn-on. Leave this pin open if fast turn-on is not needed.

GATE (Pin 11): MOSFET Gate Drive Output. Connect this pin to the gate of the external N-channel MOSFET switch. An internal clamp limits the gate voltage to 6.1V above, and a diode below SOURCE. During fast turn-on a 1.5A pull-up charges GATE to CPO. During fast turn-off a 1.5A pull-down discharges GATE to SOURCE.

SOURCE (Pin 12): MOSFET Gate Drive Return. Connect this pin to the source of the external N-channel MOSFET switch.

EXPOSED PAD (Pin 13, DD Package Only): Exposed pad may be left open or connected to device ground.

FUNCTIONAL DIAGRAM



OPERATION

The LTC4352 controls either single or back-to-back N-channel MOSFETs in order to emulate an ideal diode. Dual MOSFETs eliminate current flow from the input to the output in an input undervoltage or overvoltage condition.

When enabled, an amplifier (AMP) monitors the voltage between the V_{IN} and OUT pins, and drives the GATE pin. The amplifier controls the gate of the external MOSFET to servo its forward voltage drop ($V_{IN} - OUT$) to 25mV. The gate voltage rises to enhance the MOSFET if the load current causes more than 25mV of drop. For large output currents the MOSFET gate is driven fully on and the voltage drop is equal to $I_{LOAD} \cdot R_{DS(ON)}$.

In the case of an input supply short-circuit, when the MOSFET is conducting, a large reverse current starts flowing from the load towards the input. The AMP detects this failure condition as soon as it appears, and turns off the MOSFET by pulling down the GATE pin. The REV pin can be used to allow reverse current, overriding the diode behavior.

The AMP quickly pulls-up the GATE pin whenever it senses a large forward voltage drop. An external capacitor between the CPO and SOURCE pins is needed for fast gate pull-up. This capacitor is charged up, at device power-up, by the internal charge-pump. This stored charge is used for the fast gate pull-up.

The GATE pin sources current from the CPO pin, and sinks current to the SOURCE and GND pins. Internal clamps

limit the GATE to SOURCE voltage to 6.1V, and the CPO to SOURCE voltage to 6.7V. The same clamps also limit the CPO and GATE pins to a diode voltage below the SOURCE pin.

OV, UV, and V_{CC} comparators, CP1 to CP3, control power passage. The MOSFET is held off whenever the OV pin is above 0.5V, the UV pin is below 0.5V, or the V_{CC} pin is below 2.57V. There is a 40 μ s delay from all three conditions becoming good to GATE being allowed to turn on. Overvoltage causes a fast turn-off, while undervoltage activates a 100 μ A pull-down on GATE after a 7 μ s delay.

Open-drain pull-down, M1, pulls the \overline{STATUS} pin low when the GATE to SOURCE voltage exceeds 0.7V, to indicate that power is passing through the MOSFET. The \overline{FAULT} output, M2, pulls low during an undervoltage or overvoltage fault condition. It also pulls low when GATE is fully on and the forward voltage drop exceeds 250mV, indicating the MOSFET has too much current or has failed open circuit. Note that this open MOSFET fault does not turn off the MOSFET unlike the undervoltage and overvoltage faults.

LDO is a low dropout regulator that generates a 4.1V supply at the V_{CC} pin from the V_{IN} input. When a supply below 2.9V is being ORed, an external supply in the 2.9V to 6V range is required at the V_{CC} pin. Comparator CP4 will disable LDO when V_{IN} is below V_{CC} .

APPLICATIONS INFORMATION

High availability systems often employ parallel-connected power supplies or battery feeds to achieve redundancy and enhance system reliability. ORing diodes have been a popular means of connecting these supplies at the point of load. Diodes with storage capacitors also hold up supply voltages when an input voltage sags or has a brownout. The disadvantage of these approaches is the diode's significant forward voltage drop and the resulting power loss. Additionally, diodes provide no information concerning the status of the sourcing supply. Separate control must therefore be added to ensure that a supply that is out of range is not allowed to affect the load.

The LTC4352 solves these problems by using an external N-channel MOSFET as the pass element (see Figure 1). The MOSFET is turned on when power is being passed, allowing for a low voltage drop from the supply to the load. When the input source voltage drops below the output

common supply voltage it turns off the MOSFET, thereby matching the function and performance of an ideal diode.

Power Supply Configuration

The LTC4352 can operate with supplies down to 0V. This requires powering the V_{CC} pin with an always present external supply in the 2.9V to 6V range. If not always present, a series 470 Ω resistor or Schottky diode limits device power dissipation and backfeeding of low V_{CC} supply when V_{IN} is high. For a 2.9V to 4.7V V_{CC} supply, V_{IN} should be lower than V_{CC} . A 0.1 μ F bypass capacitor should also be connected between the V_{CC} and GND pins, close to the device. Figure 2 illustrates this.

If V_{IN} operates above 2.9V then the external supply at V_{CC} is not needed. The 0.1 μ F capacitor is still required for bypassing.

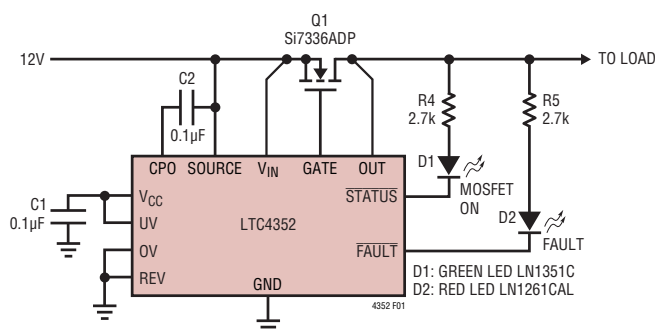


Figure 1. 12V Ideal Diode with Status and Fault Indicators

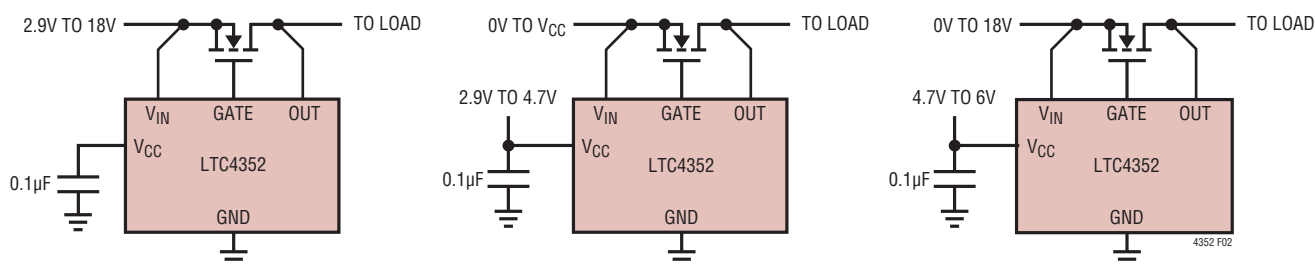


Figure 2. Power Supply Configurations

APPLICATIONS INFORMATION

CPO and GATE Start-Up

In single MOSFET applications, CPO is initially pulled up to a diode below the SOURCE pin (Figure 3). In back-to-back MOSFET applications, CPO starts off at 0V, since SOURCE is near ground (Figure 4). CPO starts ramping up 10 μ s after V_{CC} clears its undervoltage lockout level. Another 40 μ s later, GATE will also start ramping up with CPO if UV, OV and V_{IN} – OUT conditions allow it to. The ramp rate is decided by the CPO pull-up current into the combined CPO and GATE pin capacitances. An internal clamp limits the CPO voltage to 6.7V above SOURCE, while the final GATE voltage is determined by the forward drop servo amplifier.

MOSFET Selection

The LTC4352 drives N-channel MOSFETs to conduct the load current. The important features of the MOSFET are its threshold voltage, the maximum drain-source voltage BV_{DSS} , and the on-resistance $R_{DS(ON)}$.

The gate drive for the MOSFET is guaranteed to be between 5V and 7.5V. This allows the use of logic level threshold

N-channel MOSFETs. The maximum allowable drain-source voltage, BV_{DSS} , must be higher than the supply voltages as the full supply voltage can appear across the MOSFET when the input falls to 0V.

The \overline{FAULT} pin pulls low to signal an open MOSFET fault whenever the forward voltage drop across the enhanced MOSFET exceeds 250mV. The $R_{DS(ON)}$ should be small enough to conduct the maximum load current while not triggering such a fault (when using \overline{FAULT}), and to stay within the MOSFET's power rating at the maximum load current.

CPO Capacitor Selection

The recommended value of the capacitor between the CPO and SOURCE pins is approximately 10x the input capacitance, C_{ISS} , of the MOSFET. A larger capacitor takes a correspondingly longer time to charge up by the internal charge pump. A smaller capacitor suffers more voltage drop during a fast gate turn-on event as it shares charge with the MOSFET gate capacitance.

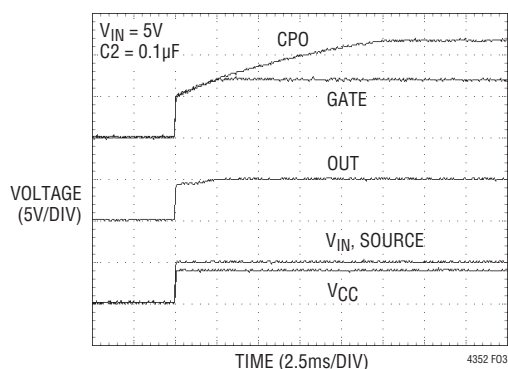


Figure 3. Start-up Waveform for Single MOSFET Application

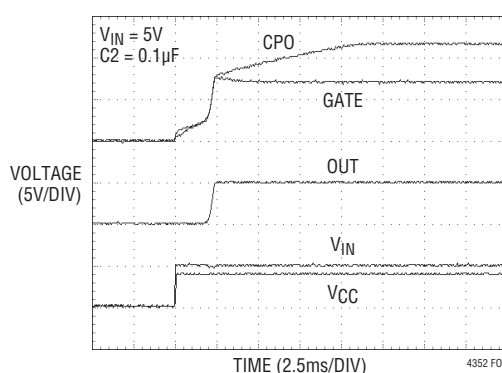


Figure 4. Start-up Waveform for Back-to-Back MOSFET Application

APPLICATIONS INFORMATION

External CPO Supply

The internal charge pump takes milliseconds to charge up the CPO pin capacitor especially during device power up. This time can be shortened by connecting an external supply to the CPO pin. A series resistor is needed to limit the current into the internal clamp between the CPO and SOURCE pins. The CPO supply should also be higher than the main input supply to meet the gate drive requirements of the MOSFET. Figure 7 shows such a 5V ideal diode application, where a 12V supply is connected to the CPO pin through a 1k resistor. The 1k limits the current into the CPO pin to 5.3mA, when the SOURCE pin is grounded.

Input Transient Protection

When the capacitances at the input and output are very small, rapid changes in current can cause transients that exceed the 24V Absolute Maximum Rating of the V_{IN} and OUT pins. In ORing applications using a single MOSFET, one surge suppressor connected from OUT to ground clamps all the inputs. In the absence of a surge suppressor, an output capacitance of 10 μ F is sufficient in most applications to prevent the transient from exceeding 24V. Back-to-back MOSFET applications, depending on voltage levels, may require a surge suppressor on each supply input.

Design Example

The following design example demonstrates the calculations involved for selecting components in a 12V system with 10A maximum load current (see Figure 1).

First, calculate the $R_{DS(ON)}$ of the MOSFET to achieve the desired forward drop at full load. Assuming a V_{FWD} of 50mV (which is comfortably below the 200mV minimum open MOSFET fault threshold):

$$R_{DS(ON)} \leq \frac{V_{FWD}}{I_{LOAD}} = \frac{50mV}{10A} = 5m\Omega$$

The Si7336ADP offers a good solution, in a SO-8 sized package, with a maximum $R_{DS(ON)}$ of 4m Ω and BV_{DSS} of 30V. The maximum power dissipation in the MOSFET is:

$$P = I_{LOAD}^2 \cdot R_{DS(ON)} = (10A)^2 \cdot 4m\Omega = 0.4W$$

With a maximum steady-state thermal resistance, θ_{JA} , of 65°C/W, 0.4W causes a modest 26°C rise in junction temperature of the Si7336ADP above the ambient.

The input capacitance, C_{ISS} , of the Si7336ADP is about 6500pF. Slightly exceeding the 10x recommendation, a 0.1 μ F capacitor is selected for C2.

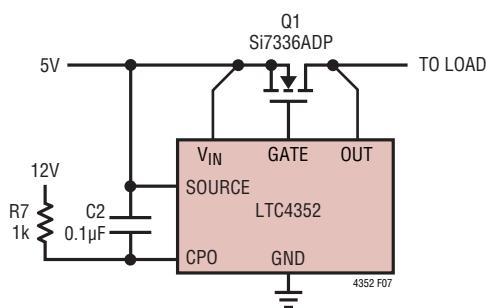


Figure 7. 5V Ideal Diode with External 12V Powering CPO for Faster Start-up and Refresh

APPLICATIONS INFORMATION

LEDs, D1 and D2, require around 3mA for good luminous intensity. Accounting for a 2V diode drop and 0.5V V_{OL} , R1 and R2 are set to 2.7k.

PCB Layout Considerations

Connect the V_{IN} and OUT pin traces as close as possible to the MOSFET's terminals. Keep the traces to the MOSFET wide and short to minimize resistive losses. The PCB traces

associated with the power path through the MOSFET should have low resistance. See Figure 8.

It is also important to put C1, the bypass capacitor for the V_{CC} pin, as close as possible between V_{CC} and GND. Also place C2 near the CPO and SOURCE pins. Surge suppressors, when used, should be mounted close to the LTC4352 using short lead lengths.

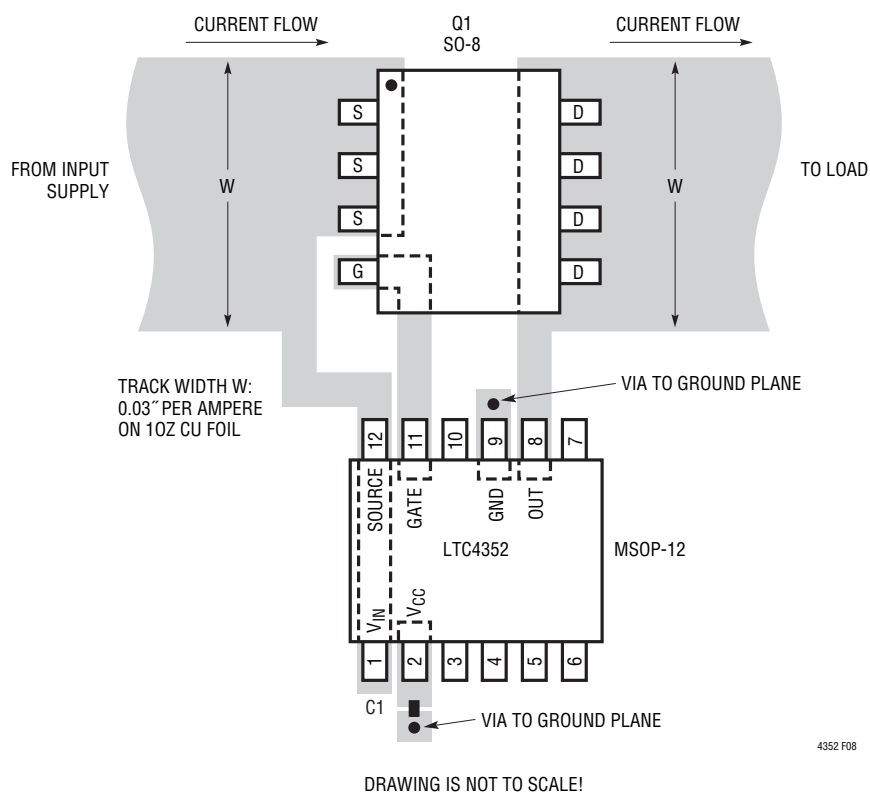
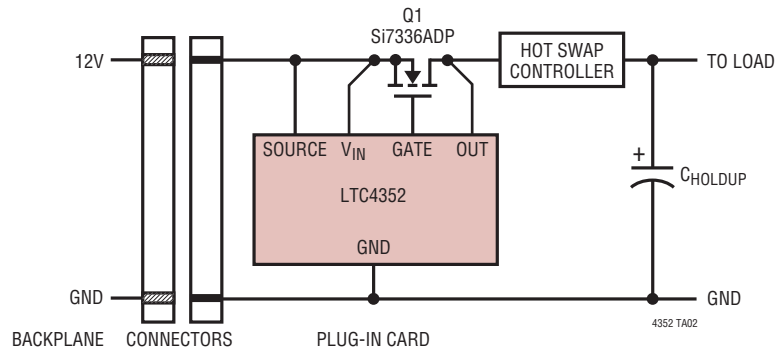


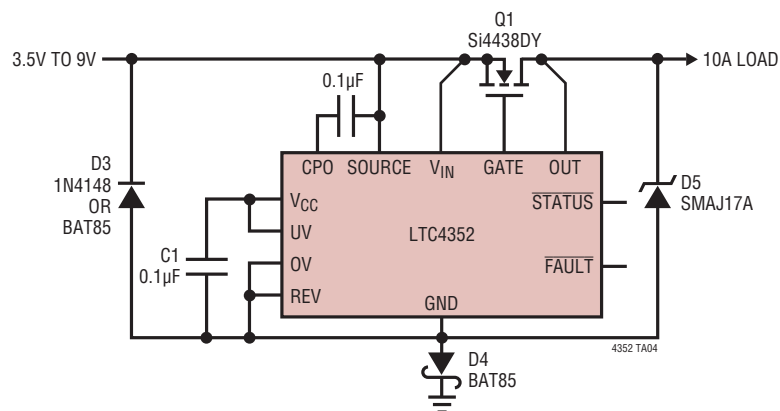
Figure 8. Recommended PCB Layout for Power MOSFET

TYPICAL APPLICATIONS

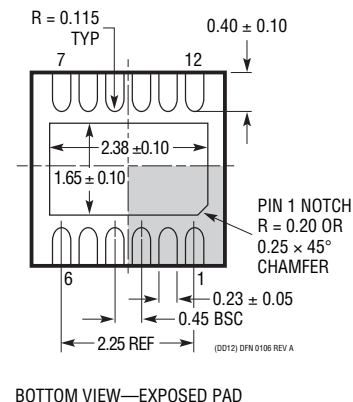
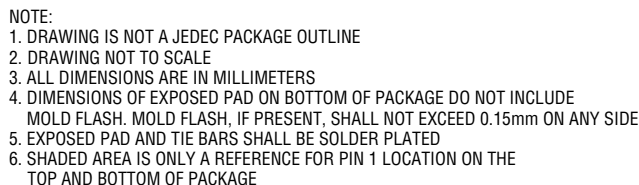
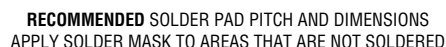
Plug-in Card Supply Holdup Using Ideal Diode at Input



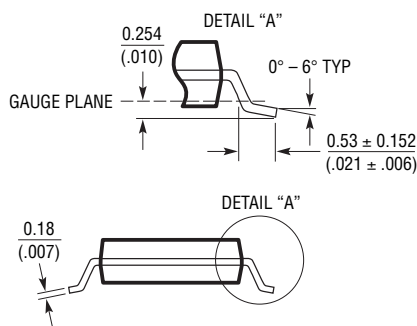
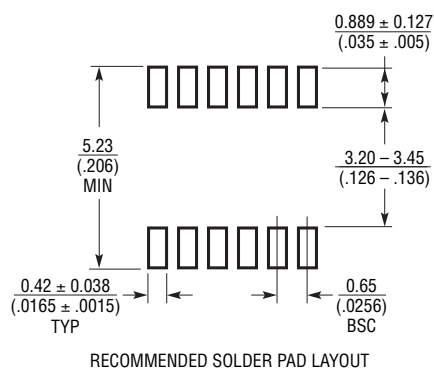
Ideal Diode with Reverse Input Protection



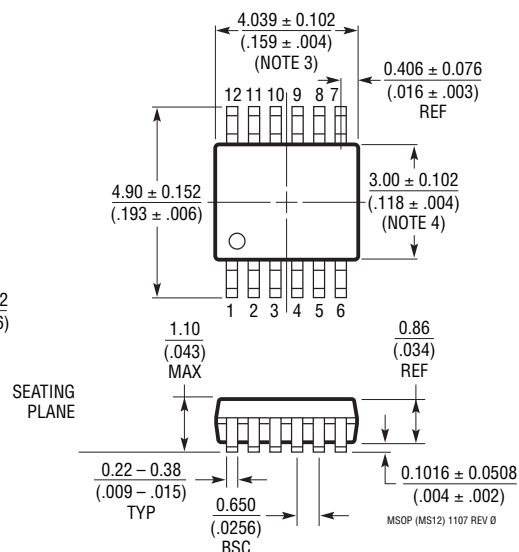
(Reference LTC DWG # 05-08-1725 Rev A)



(Reference LTC DWG # 05-08-1668 Rev Ø)



- NOTE: 1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX



REVISION HISTORY

| REV | DATE | DESCRIPTION | PAGE NUMBER |
|-----|-------|--|-------------|
| A | 12/10 | Added H-grade information | 2,3 |
| | | Revised $\overline{\text{FAULT}}$ pin description in Pin Functions | 5 |
| | | Revised Functional Diagram | 6 |
| | | Added text to Operation section | 7 |
| | | Revised Figures 2, 5, 6 in Applications Information | 8, 10 |
| | | Added new Typical Application | 13 |
| | | Revised Typical Application and Related Parts list | 16 |

RELATED PARTS

| PART NUMBER | DESCRIPTION | COMMENTS |
|-------------------|--|--|
| LTC1473/LTC1473L | Dual PowerPath™ Switch Driver | N-Channel, 4.75V to 30V/3.3V to 10V, SSOP-16 |
| LTC1479 | PowerPath Controller for Dual Battery Systems | Three N-Channel Drivers, 6V to 28V, SSOP-36 |
| LTC4350 | Hot Swappable Load Share Controller | N-Channel, 1.5V to 12V, Share Bus, SSOP-16 |
| LTC4354 | Negative Voltage Diode-OR Controller and Monitor | Dual N-Channel, –4.5V to –80V, SO-8, DFN-8 |
| LTC4355 | Positive High Voltage Ideal Diode-OR and Monitor | Dual N-Channel, 9V to 80V, SO-16, DFN-14 |
| LTC4357 | Positive High Voltage Ideal Diode Controller | N-Channel, 9V to 80V, MSOP-8, DFN-6 |
| LTC4358 | 5A Ideal Diode | Internal N-Channel, 9V to 26.5V, TSSOP-16, DFN-14 |
| LTC4411 | 2.6A Low Loss Ideal Diode in ThinSOT™ | Internal P-Channel, 2.6V to 5.5V, 40μA I _Q , SOT-23 |
| LTC4412/LTC4412HV | Low Loss PowerPath Controller in ThinSOT | P-Channel, 2.5V to 28V/36V, 11μA I _Q , TSOT-23 |
| LTC4413/LTC4413-1 | Dual 2.6A, 2.5V to 5.5V, Ideal Diodes in DFN-10 | Dual Internal P-Channel, 2.5V to 5.5V, DFN-10 |
| LTC4414 | 36V Low Loss PowerPath Controller for Large PFETs | P-Channel, 3V to 36V, 30μA I _Q , MSOP-8 |
| LTC4416/LTC4416-1 | 36V Low Loss Dual PowerPath Controller for Large PFETs | Dual P-Channel, 3.6V to 36V, 70μA I _Q , MSOP-10 |